

Quad 2-input NAND Gate

CD4011

Logic

1 Introduction

The CD4011 is a quad 2-input NAND gate. The outputs are fully buffered for the highest noise immunity and pattern insensitivity to output impedance.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

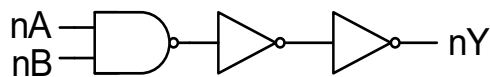
3 Features

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40°C to $+125^{\circ}\text{C}$

2 Available Packages

PART NUMBER	PACKAGE
CD4011	SOP14
	TSSOP14

Note: For all available packages, please refer to the part Orderable Information.



Logic diagram

4 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4011ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CD4011BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

5 Pin Configuration and Marking Information

5.1 Pin Configuration

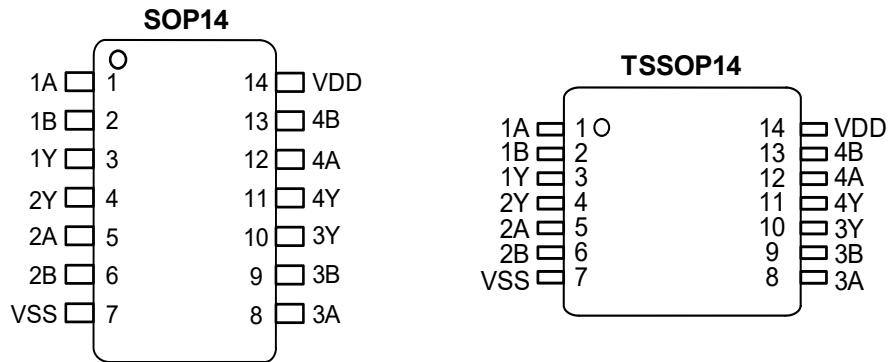


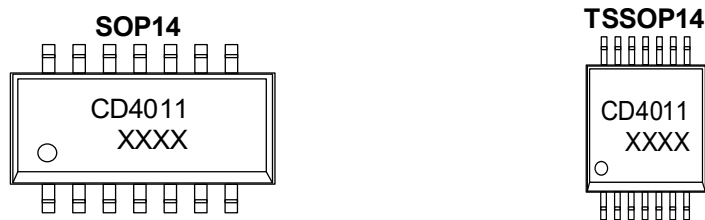
Figure 5-1 Pin configuration

5.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	1A	I	Data input
2	1B	I	Data input
3	1Y	O	Data output
4	2Y	O	Data output
5	2A	I	Data input
6	2B	I	Data input
7	VSS	G	Ground (0V)
8	3A	I	Data input
9	3B	I	Data input
10	3Y	O	Data output
11	4Y	O	Data output
12	4A	I	Data input
13	4B	I	Data input
14	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

5.3 Marking Information



XXXX: Code, indicates weekly record information.

6 Specifications

6.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+18	V
I_{IK}	DC input current	Any one input		-	± 10	mA
V_I	Input voltage	All inputs		-0.5	$V_{DD}+0.5$	V
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

6.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	15	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C

6.3 Electrical Characteristics

6.3.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			T _{amb} =25°C			UNIT
		V _O	V _{IN}	V _{DD}	MIN.	TYP.	MAX.	
I _{DD}	Supply current	-	0/5	5	-	-	1	uA
		-	0/10	10	-	-	1	uA
		-	0/15	15	-	-	1	uA
I _{OL}	LOW-level output current	0.4	0/5	5	0.51	1	-	mA
		0.5	0/10	10	1.3	2.6	-	mA
		1.5	0/15	15	3.4	6.8	-	mA
I _{OH}	HIGH-level output current	4.6	0/5	5	-0.51	-	-	mA
		2.5	0/5	5	-1.6	-	-	mA
		9.5	0/10	10	-1.3	-	-	mA
		13.5	0/15	15	-3.4	-	-	mA
V _{OL}	LOW-level output voltage	-	0/5	5	-	0	0.05	V
		-	0/10	10	-	0	0.05	V
		-	0/15	15	-	0	0.05	V
V _{OH}	HIGH-level output voltage	-	0/5	5	4.95	5	-	V
		-	0/10	10	9.95	10	-	V
		-	0/15	15	14.95	15	-	V
V _{IL}	LOW-level input voltage	4.5	-	5	-	-	1.5	V
		9	-	10	-	-	3	V
		13.5	-	15	-	-	4	V
V _{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	-	V
		1/9	-	10	7	-	-	V
		1.5/13.5	-	15	11	-	-	V
I _I	Input leakage current	-	0/15	15	-	-	±1	uA

6.3.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			T _{amb} =-40°C		T _{amb} =+85°C		T _{amb} =+125°C		UNIT
		V _O	V _{IN}	V _{DD}	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
I _{DD}	Supply current	-	0/5	5	-	1	-	7.5	-	7.5	uA
		-	0/10	10	-	1	-	15	-	15	uA
		-	0/15	15	-	1	-	30	-	30	uA
I _{OL}	LOW-level output current	0.4	0/5	5	0.61	-	0.42	-	0.36	-	mA
		0.5	0/10	10	1.5	-	1.1	-	0.9	-	mA
		1.5	0/15	15	4	-	2.8	-	2.4	-	mA
I _{OH}	HIGH-level output current	4.6	0/5	5	-0.61	-	-0.42	-	-0.36	-	mA
		2.5	0/5	5	-1.8	-	-1.3	-	-1.15	-	mA
		9.5	0/10	10	-1.5	-	-1.1	-	-0.9	-	mA
		13.5	0/15	15	-4	-	-2.8	-	-2.4	-	mA
V _{OL}	LOW-level output voltage	-	0/5	5	-	0.05	-	0.05	-	0.05	V
		-	0/10	10	-	0.05	-	0.05	-	0.05	V
		-	0/15	15	-	0.05	-	0.05	-	0.05	V
V _{OH}	HIGH-level output voltage	-	0/5	5	4.95	-	4.95	-	4.95	-	V
		-	0/10	10	9.95	-	9.95	-	9.95	-	V
		-	0/15	15	14.95	-	14.95	-	14.95	-	V
V _{IL}	LOW-level input voltage	4.5	-	5	-	1.5	-	1.5	-	1.5	V
		9	-	10	-	3	-	3	-	3	V
		13.5	-	15	-	4	-	4	-	4	V
V _{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1/9	-	10	7	-	7	-	7	-	V
		1.5/13.5	-	15	11	-	11	-	11	-	V
I _I	Input leakage current	-	0/15	15	-	±1	-	±1	-	±1	uA

6.3.3 AC Characteristics

T_{amb}=25°C, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200kΩ, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
t _{PHL} , t _{PLH}	Propagation delay time	See Figure 7-4	V _{DD} =5V	-	125	250	ns
		V _{DD} =10V	-	60	120	ns	
		V _{DD} =15V	-	45	90	ns	
t _{THL} , t _{TLH}	Transition time	See Figure 7-4	V _{DD} =5V	-	100	200	ns
		V _{DD} =10V	-	50	100	ns	
		V _{DD} =15V	-	40	80	ns	
C _I	Input capacitance	Any input	-	5	7.5	pF	

7 Detailed Description

7.1 Overview

The CD4011 is a quad 2-input NAND gate. The outputs are fully buffered for the highest noise immunity and pattern insensitivity to output impedance.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

7.2 Functional Block Diagram

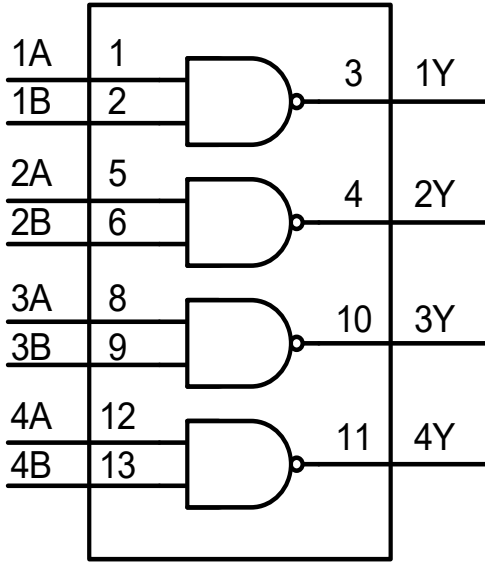


Figure 7-1 Functional diagram

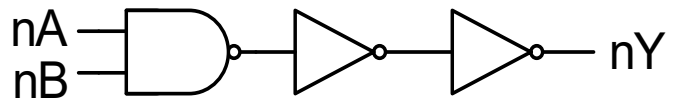


Figure 7-2 Logic diagram (one gate)

7.3 Function Table

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

Note: H=HIGH voltage level; L=LOW voltage level.

7.4 Testing Circuit

7.4.1 AC Testing Circuit

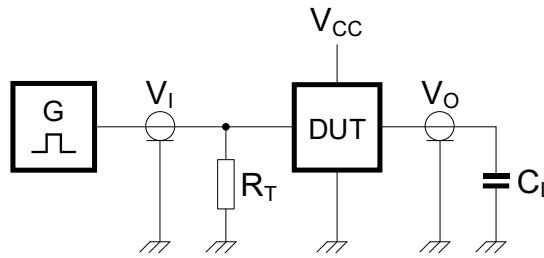


Figure 7-3 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

CL=Load capacitance including jig and probe capacitance.

RT=Termination resistance should be equal to the output impedance Zo of the pulse generator.

7.4.2 AC Testing Waveforms

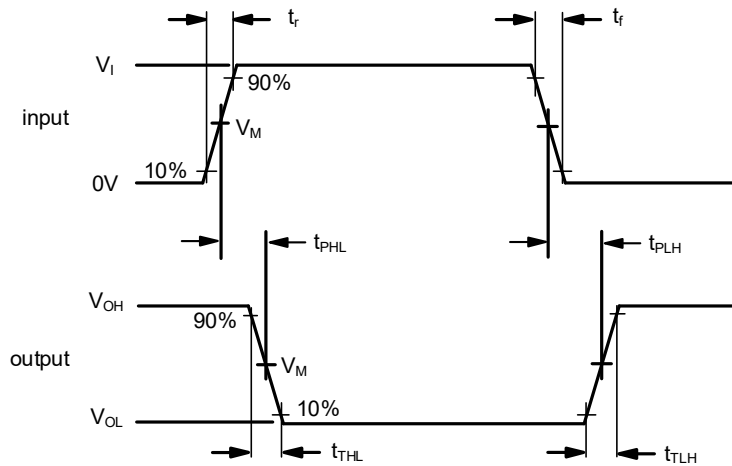


Figure 7-4 Propagation delay, output transition time

7.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V _{DD}	V _M	V _M
5V to 15V	0.5xV _{DD}	0.5xV _{DD}

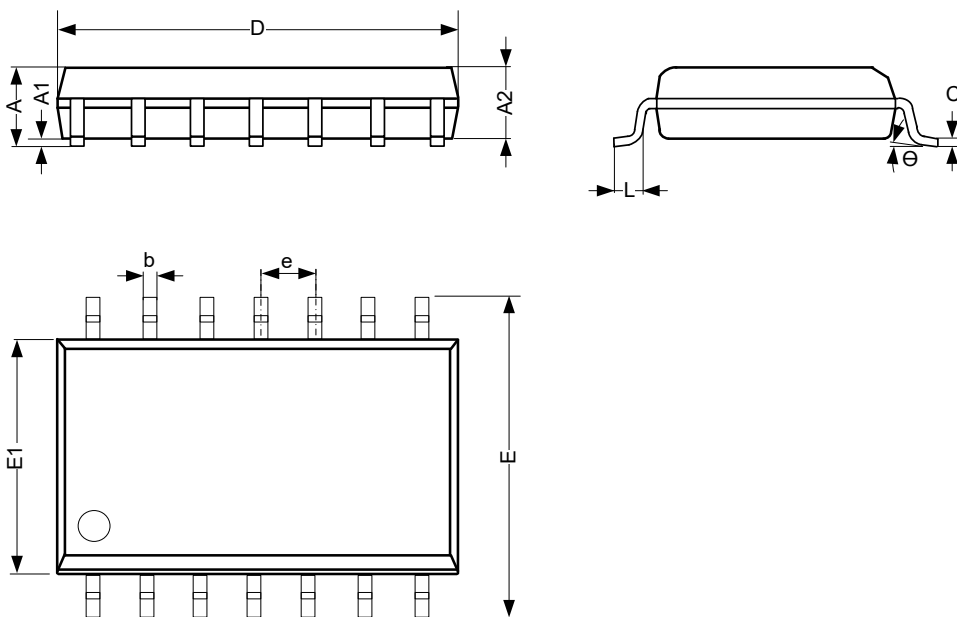
7.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD
V _{DD}	V _I	t _r , t _f	C _L
5V to 15V	V _{SS} or V _{DD}	≤ 20ns	50pF

8 Mechanical Information

8.1 SOP14 Mechanical Information

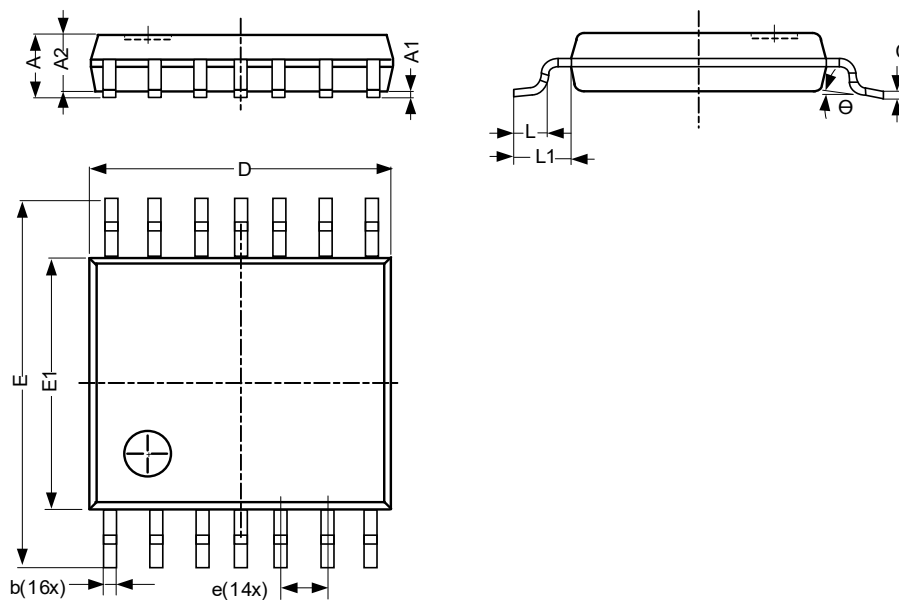
8.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
Θ	0°	-	8°
Unit: mm			

8.2 TSSOP14 Mechanical Information

8.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

9 Notes and Revision History

9.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

9.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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