Dual D-type Flip-flop

CD4013 Logic

1 Introduction

The CD4013 is a dual D-type flip-flop that features independent set-direct input (SD), clear-direct input (CD), clock input (CP) and outputs (Q, /Q). Data is accepted when CP is LOW and is transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous CD and SD inputs are independent and override the D or CP inputs. The outputs are buffered for best system performance. The clock input's Schmitt-trigger action makes the circuit highly tolerant of slower clock rise and fall times.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2 Available Packages

PART NUMBER	PACKAGE
CD4013	SOP14
	TSSOP14

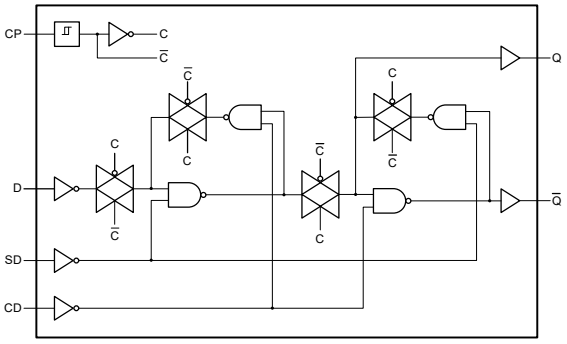
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Tolerant of slow clock rise and fall times
- Specified from -40°C to +125°C

4 Applications

- Power Delivery
- Grid Infrastructure
- Medical, Healthcare, and Fitness
- BodyElectronics and Lighting
- Building Automation
- Telecom Infrastructure
- Test and Measurement



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4013ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CD4013BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

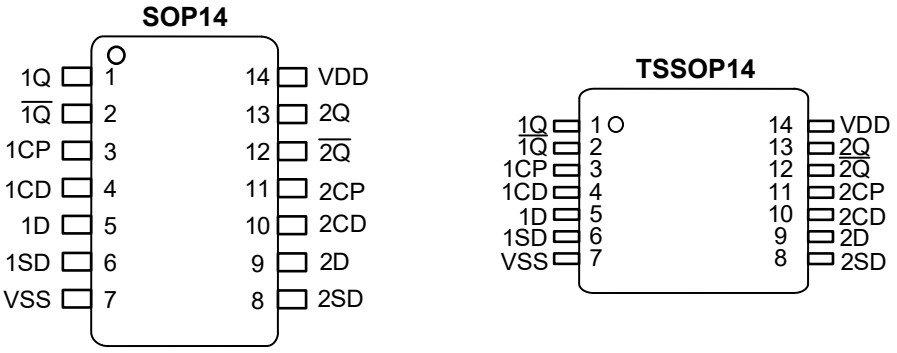


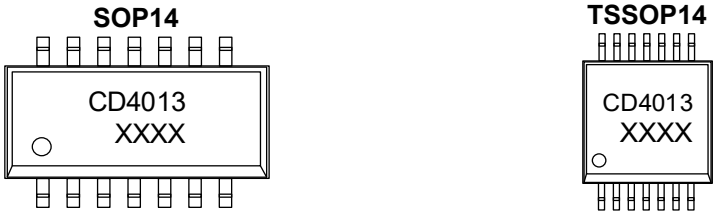
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	1Q	O	True output
2	$\overline{1Q}$	O	Complement output
3	1CP	I	Cock input (LOW to HIGH edge-triggered)
4	1CD	I	Asynchronous clear-direct input (active HIGH)
5	1D	I	Data input
6	1SD	I	Asynchronous set-direct input (active HIGH)
7	VSS	G	Ground (0V)
8	2SD	I	Asynchronous set-direct input (active HIGH)
9	2D	I	Data input
10	2CD	I	Asynchronous clear-direct input (active HIGH)
11	2CP	I	Clock input (LOW to HIGH edge-triggered)
12	$\overline{2Q}$	O	Complement output
13	2Q	O	True output
14	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+18	V
I_{IK}	DC input current	Any one input		-	±10	mA
V_I	Input voltage	All inputs		-0.5	V_{DD}+0.5	V
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	15	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C
t_{su}	Set-up time	V_{DD}=5V	40	-	-	ns
		V_{DD}=10V	20	-	-	ns
		V_{DD}=15V	15	-	-	ns
t_{wCL}	Clock pulse width	V_{DD}=5V	140	-	-	ns
		V_{DD}=10V	60	-	-	ns
		V_{DD}=15V	40	-	-	ns
f_{CL}	Clock input frequency	V_{DD}=5V	3.5	7	-	MHz
		V_{DD}=10V	8	16	-	MHz
		V_{DD}=15V	12	24	-	MHz
t_{rCL}, t_{fCL}	Clock rise and fall time	V_{DD}=5V	-	-	15	us
		V_{DD}=10V	-	-	10	us
		V_{DD}=15V	-	-	5	us
$t_{wS/R}$	Set or reset pulse width	V_{DD}=5V	180	-	-	ns
		V_{DD}=10V	80	-	-	ns
		V_{DD}=15V	50	-	-	ns

Note: If more than one unit is cascaded in a parallel clocked operation, t_{rCL} must be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transistion time of the output driving stage for the estimated capacitive load.

7.3 Electrical Characteristics

7.3.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			T_{amb}=25°C			UNIT
		V_O	V_{IN}	V_{DD}	MIN.	TYP.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	-	1	uA
		-	0/10	10	-	-	2	uA
		-	0/15	15	-	-	4	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.51	1	-	mA
		0.5	0/10	10	1.3	2.6	-	mA
		1.5	0/15	15	3.4	6.8	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.51	-	-	mA
		2.5	0/5	5	-1.6	-	-	mA
		9.5	0/10	10	-1.3	-	-	mA
		13.5	0/15	15	-3.4	-	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0	0.05	V
		-	0/10	10	-	0	0.05	V
		-	0/15	15	-	0	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	5	-	V
		-	0/10	10	9.95	10	-	V
		-	0/15	15	14.95	15	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	-	1.5	V
		1/9	-	10	-	-	3	V
		1.5/13.5	-	15	-	-	4	V
V_{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	-	V
		1/9	-	10	7	-	-	V
		1.5/13.5	-	15	11	-	-	V
I_I	Input leakage current	-	0/15	15	-	-	±1	uA

7.3.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			T_{amb}=-40°C		T_{amb}=+85°C		T_{amb}=+125°C		UNIT
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	Min.	Max.	
I_{DD}	Supply current	-	0/5	5	-	1	-	30	-	30	uA
		-	0/10	10	-	2	-	60	-	60	uA
		-	0/15	15	-	4	-	120	-	120	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.61	-	0.42	-	0.36	-	mA
		0.5	0/10	10	1.5	-	1.1	-	0.9	-	mA
		1.5	0/15	15	4	-	2.8	-	2.4	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.61	-	-0.42	-	-0.36	-	mA
		2.5	0/5	5	-1.8	-	-1.3	-	-1.15	-	mA
		9.5	0/10	10	-1.5	-	-1.1	-	-0.9	-	mA
		13.5	0/15	15	-4	-	-2.8	-	-2.4	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0.05	-	0.05	-	0.05	V
		-	0/10	10	-	0.05	-	0.05	-	0.05	V
		-	0/15	15	-	0.05	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	-	4.95	-	4.95	-	V
		-	0/10	10	9.95	-	9.95	-	9.95	-	V
		-	0/15	15	14.95	-	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	1.5	-	1.5	-	1.5	V
		1/9	-	10	-	3	-	3	-	3	V
		1.5/13.5	-	15	-	4	-	4	-	4	V
V_{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1/9	-	10	7	-	7	-	7	-	V
		1.5/13.5	-	15	11	-	11	-	11	-	V
I_I	Input leakage current	-	0/15	15	-	±1	-	±1	-	±1	uA

7.3.3 AC Characteristics

T_{amb}=25°C, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=20kΩ, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}	HIGH to LOW propagation delay	nCP to nQ, $n\overline{Q}$; See Figure 8-4	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=15V	-	45	90	ns
		nSD to $n\overline{Q}$ or nCD to nQ	V_{DD}=5V	-	200	400	ns
			V_{DD}=10V	-	85	170	ns
			V_{DD}=15V	-	60	120	ns
t_{PLH}	LOW to HIGH propagation delay	nCP to nQ, $n\overline{Q}$; See Figure 8-4	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=15V	-	45	90	ns
		nSD to nQ or nCD to $n\overline{Q}$	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=15V	-	45	90	ns
t_t	Transition time	See Figure 8-4	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	80	ns
$f_{clk(max)}$	Maximum clock frequency	See Figure 8-4	V_{DD}=5V	3.5	7	-	MHz
			V_{DD}=10V	8	16	-	MHz
			V_{DD}=15V	12	24	-	MHz
t_W	Pulse width	nCP input LOW; See Figure 8-4	V_{DD}=5V	-	70	140	ns
			V_{DD}=10V	-	30	60	ns
			V_{DD}=15V	-	20	40	ns
		nSD input HIGH or nCD input HIGH; See Figure 8-5	V_{DD}=5V	-	90	180	ns
			V_{DD}=10V	-	40	80	ns
			V_{DD}=15V	-	25	50	ns
t_{su}	Set-up time	nD to nCP; See Figure 8-4	V_{DD}=5V	-	20	40	ns
			V_{DD}=10V	-	10	20	ns
			V_{DD}=15V	-	7	15	ns
t_h	Hold time	nD to nCP; See Figure 8-4	V_{DD}=5V	-	2	5	ns
			V_{DD}=10V	-	2	5	ns
			V_{DD}=15V	-	2	5	ns
t_{rCL}, t_{fCL}	Clock input rise or fall time	-	V_{DD}=5V	-	-	15	us
			V_{DD}=10V	-	-	10	us
			V_{DD}=15V	-	-	5	us
C_I	Input capacitance	Any input		-	5	7.5	pF

Note: t_t is the same as t_{TLH} and t_{THL}.

8 Detailed Description

8.1 Overview

The CD4013 is a dual D-type flip-flop that features independent set-direct input (SD), clear-direct input (CD), clock input (CP) and outputs (Q, /Q). Data is accepted when CP is LOW and is transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous CD and SD inputs are independent and override the D or CP inputs. The outputs are buffered for best system performance. The clock input's Schmitt-trigger action makes the circuit highly tolerant of slower clock rise and fall times.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

8.2 Functional Block Diagram

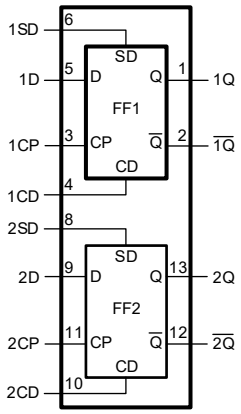


Figure 8-1 Functional diagram

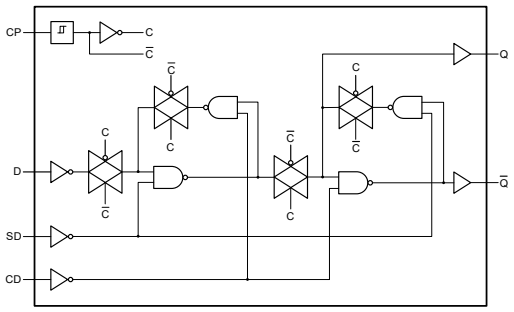


Figure 8-2 Logic diagram (one flip-flop)

8.3 Function Table

INPUT				OUTPUT	
nSD	**nCD**	**nCP**	**nD**	**nQ**	**$\overline{nQ}$**
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	↑	L	L	H
L	L	↑	H	H	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑ =LOW-to-HIGH clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

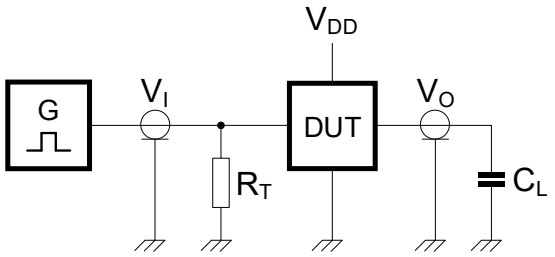


Figure 8-3 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

8.4.2 AC Testing Waveforms

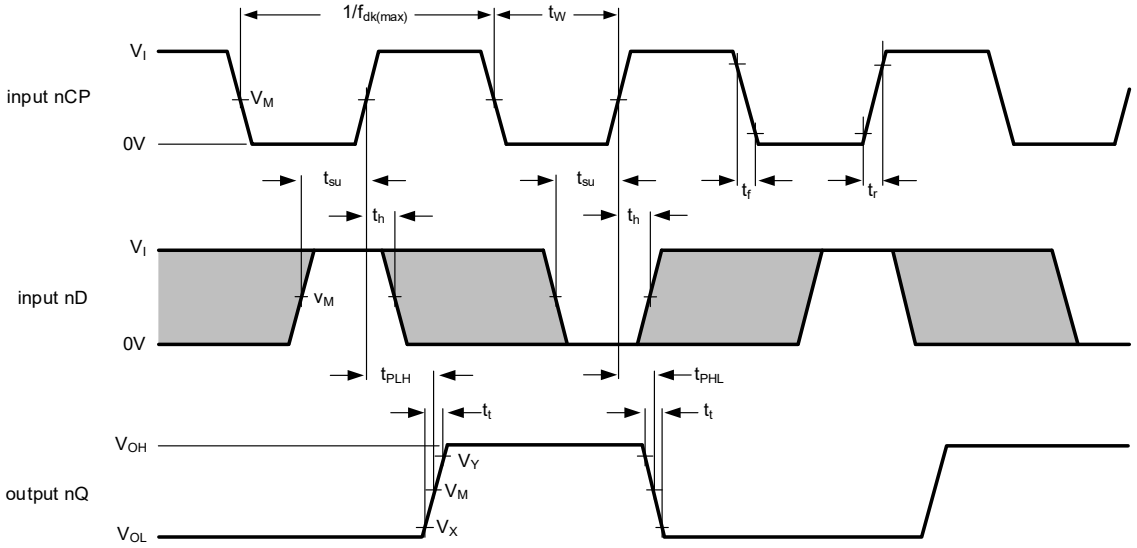


Figure 8-4 Set-up time, hold time, minimum clock pulse width, propagation delays and transition times

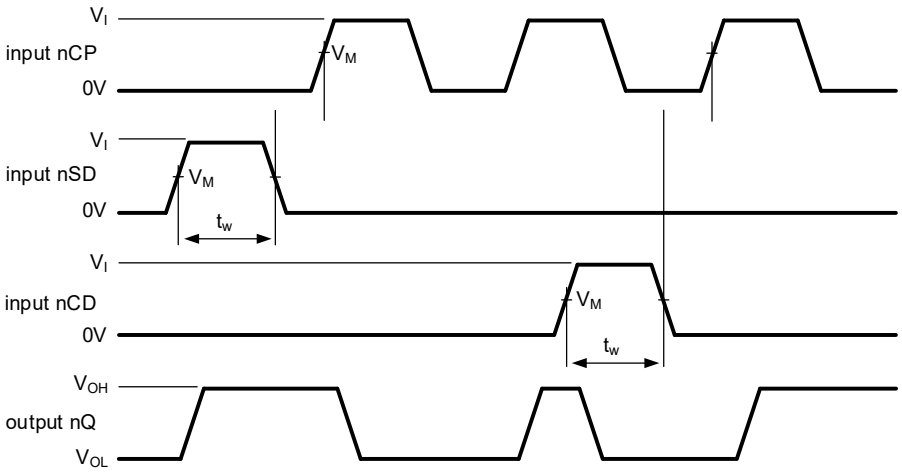


Figure 8-5 nSD, nCD pulse width

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT		
V_{DD}	V_M	V_M	V_X	V_Y
5V to 15V	0.5xV_{DD}	0.5xV_{DD}	0.1xV_{DD}	0.9xV_{DD}

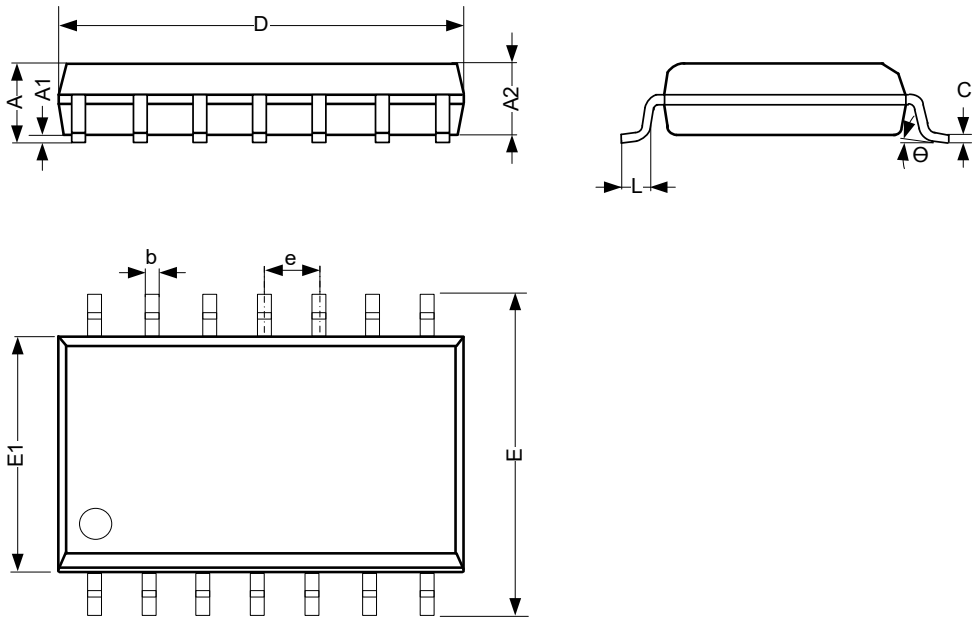
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD
V_{DD}	V_I	t_r , t_f	C_L
5V to 15V	V_{SS} or V_{DD}	≤20ns	50pF

9 Mechanical Information

9.1 SOP14 Mechanical Information

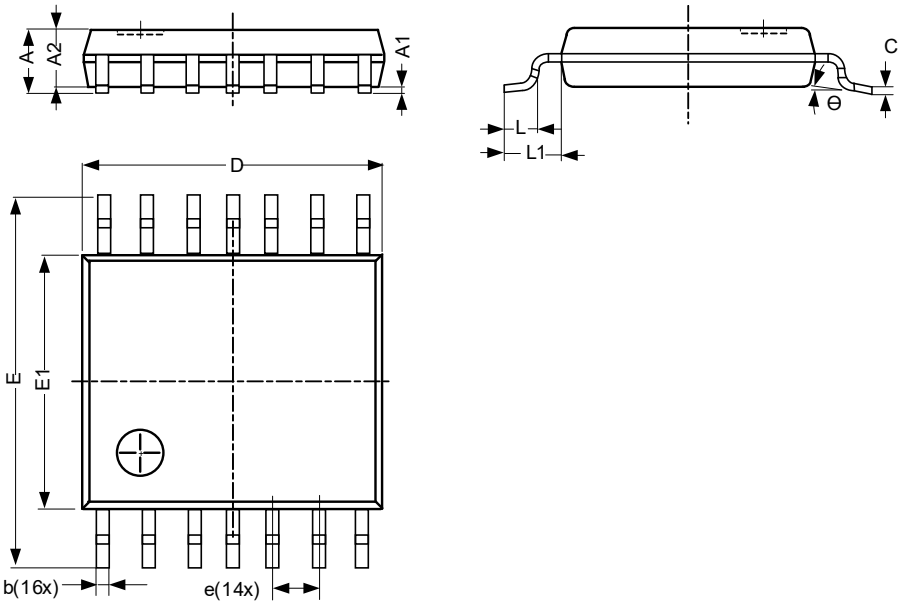
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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