14-stage Ripple-carry Binary Counter/Divider and Oscillator

CD4060 Logic

1 Introduction

CD4060 is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, REXT and CEXT), ten buffered outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset input (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q3 to Q9 and Q11 to Q13=LOW), independent of other input conditions.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2 Available Packages

PART NUMBER	PACKAGE
CD4060	SOP16
	TSSOP16

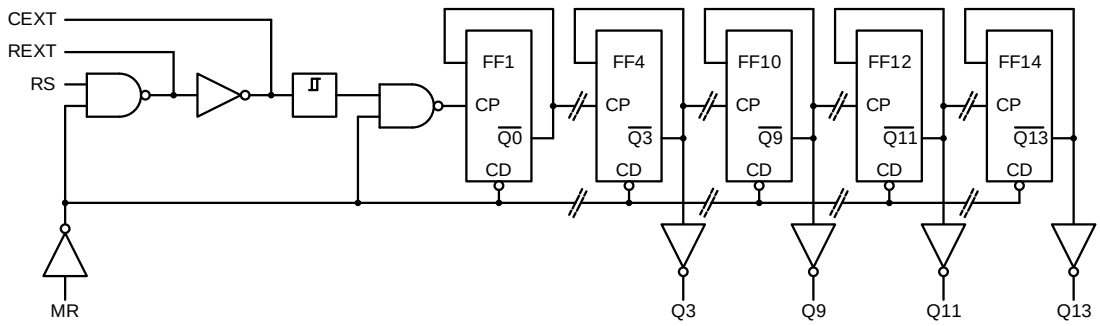
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 15V
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40°C to +125°C

4 Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4060AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CD4060BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

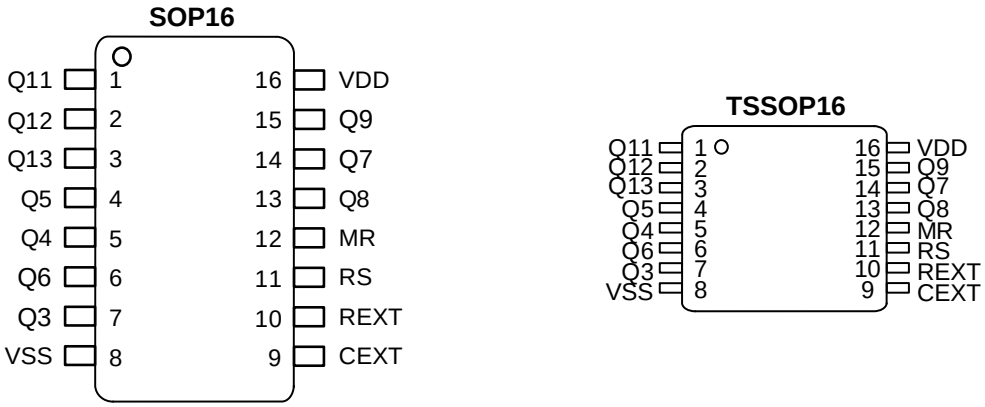


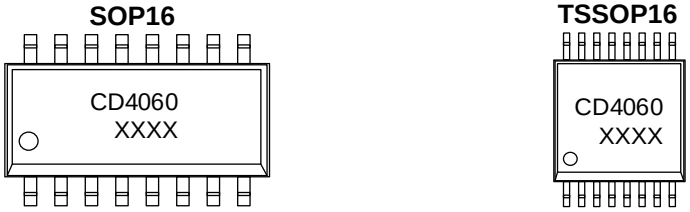
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	Q11	O	Counter output
2	Q12	O	Counter output
3	Q13	O	Counter output
4	Q5	O	Counter output
5	Q4	O	Counter output
6	Q6	O	Counter output
7	Q3	O	Counter output
8	VSS	G	Ground (0V)
9	CEXT	-	External capacitor connection
10	REXT	O	Oscillator pin
11	RS	I	Clock input/oscillator pin
12	MR	I	Master reset
13	Q8	O	Counter output
14	Q7	O	Counter output
15	Q9	O	Counter output
16	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+18	V
I_{IK}	DC input current	Any one input		-	±10	mA
V_I	Input voltage	All inputs		-0.5	V_{DD}+0.5	V
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-		3	-	15	V
T_{amb}	Ambient temperature	In free air		-40	-	+125	°C
t_w	Input pulse width	f=100kHz	V_{DD}=5V	100	-	-	ns
			V_{DD}=10V	40	-	-	ns
			V_{DD}=15V	30	-	-	ns
t_{rIN}, t_{fIN}	Input pulse rise and fall time	V_{DD}=5V		Unlimited			-
		V_{DD}=10V					-
		V_{DD}=15V					-
f_{RS}	Input pulse frequency	External pulse source	V_{DD}=5V	-	-	3.5	MHz
			V_{DD}=10V	-	-	8	MHz
			V_{DD}=15V	-	-	12	MHz
t_{wR}	Reset pulse width	V_{DD}=5V		120	-	-	ns
		V_{DD}=10V		60	-	-	ns
		V_{DD}=15V		40	-	-	ns

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	1500	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			T_{amb}=25°C			UNIT
		V_O	V_{IN}	V_{DD}	MIN.	TYP.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	-	5	uA
		-	0/10	10	-	-	10	uA
		-	0/15	15	-	-	20	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.51	1	-	mA
		0.5	0/10	10	1.3	2.6	-	mA
		1.5	0/15	15	3.4	6.8	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.51	-	-	mA
		2.5	0/5	5	-1.6	-	-	mA
		9.5	0/10	10	-1.3	-	-	mA
		13.5	0/15	15	-3.4	-	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0	0.05	V
		-	0/10	10	-	0	0.05	V
		-	0/15	15	-	0	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	5	-	V
		-	0/10	10	9.95	10	-	V
		-	0/15	15	14.95	15	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	-	1.5	V
		1/9	-	10	-	-	3	V
		1.5/13.5	-	15	-	-	4	V
V_{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	-	V
		1/9	-	10	7	-	-	V
		1.5/13.5	-	15	11	-	-	V
I_I	Input leakage current	-	0/15	15	-	-	±1	uA

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			T_{amb}=-40°C		T_{amb}=+85°C		UNIT
		V_O	V_{IN}	V_{DD}	MIN.	MAX.	MIN.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	5	-	150	uA
		-	0/10	10	-	10	-	300	uA
		-	0/15	15	-	20	-	600	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.61	-	0.42	-	mA
		0.5	0/10	10	1.5	-	1.1	-	mA

		1.5	0/15	15	4	-	2.8	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.61	-	-0.42	-	mA
		2.5	0/5	5	-1.8	-	-1.3	-	mA
		9.5	0/10	10	-1.5	-	-1.1	-	mA
		13.5	0/15	15	-4	-	-2.8	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0.05	-	0.05	V
		-	0/10	10	-	0.05	-	0.05	V
		-	0/15	15	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	-	4.95	-	V
		-	0/10	10	9.95	-	9.95	-	V
		-	0/15	15	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	1.5	-	1.5	V
		1/9	-	10	-	3	-	3	V
		1.5/13.5	-	15	-	4	-	4	V
V_{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	3.5	-	V
		1/9	-	10	7	-	7	-	V
		1.5/13.5	-	15	11	-	11	-	V
I_I	Input leakage current	-	0/15	15	-	±1	-	±1	uA

7.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			T_{amb}=-40°C		T_{amb}=+125°C		UNIT
		V_O	V_{IN}	V_{DD}	MIN.	MAX.	MIN.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	5	-	150	uA
		-	0/10	10	-	10	-	300	uA
		-	0/15	15	-	20	-	600	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.61	-	0.36	-	mA
		0.5	0/10	10	1.5	-	0.9	-	mA
		1.5	0/15	15	4	-	2.4	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.61	-	-0.36	-	mA
		2.5	0/5	5	-1.8	-	-1.15	-	mA
		9.5	0/10	10	-1.5	-	-0.9	-	mA
		13.5	0/15	15	-4	-	-2.4	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0.05	-	0.05	V
		-	0/10	10	-	0.05	-	0.05	V
		-	0/15	15	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	-	4.95	-	V
		-	0/10	10	9.95	-	9.95	-	V

		-	0/15	15	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	1.5	-	1.5	V
		1/9	-	10	-	3	-	3	V
		1.5/13.5	-	15	-	4	-	4	V
V_{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	3.5	-	V
		1/9	-	10	7	-	7	-	V
		1.5/13.5	-	15	11	-	11	-	V
I_I	Input leakage current	-	0/15	15	-	±1	-	±1	uA

7.4.4 AC Characteristics 1

T_{amb}=25°C, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200kΩ, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time	RS to Q3 out; See Figure 8-4	V_{DD}=5V	-	370	740	ns
			V_{DD}=10V	-	150	300	ns
			V_{DD}=15V	-	100	200	ns
		Q_n to Q_{n+1}; See Figure 8-4	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	80	ns
		MR to Qn; See Figure 8-4	V_{DD}=5V	-	180	360	ns
			V_{DD}=10V	-	80	160	ns
			V_{DD}=15V	-	50	100	ns
t_t	Transition time	See Figure 8-4	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	80	ns
t_W	Pulse width	Minimum width; f=100kHz; RS HIGH;	V_{DD}=5V	-	50	100	ns
			V_{DD}=10V	-	20	40	ns
			V_{DD}=15V	-	15	30	ns
		Minimum width; MR HIGH; See Figure 8-4	V_{DD}=5V	-	60	120	ns
			V_{DD}=10V	-	30	60	ns
			V_{DD}=15V	-	20	40	ns
t_{rIN}, t_{fIN}	Input pulse rise and fall time	-	V_{DD}=5V	Unlimited			-
			V_{DD}=10V				-
			V_{DD}=15V				-
f_{max}	Maximum clock frequency	Input RS; see Figure 4	V_{DD}=5V	3.5	7	-	MHz
			V_{DD}=10V	8	16	-	MHz
			V_{DD}=15V	12	24	-	MHz
C_I	Input capacitance	Any input		-	5	7.5	pF

Note: t_t is the same as t_{TLH} and t_{THL}.

7.4.5 AC Characteristics 2

RC Operation, T_{amb}=25°C, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200kΩ, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
-	Variation of frequency (unit to unit)	C_X=200pF R_S=560kΩ R_X=50kΩ	V_{DD}=5V	-	23±10%	-	kHz
			V_{DD}=10V	-	24±10%	-	kHz
			V_{DD}=15V	-	25±10%	-	kHz
-	Variation of frequency with voltage change (same unit)	C_X=200pF R_S=560kΩ R_X=50kΩ	5V to 10V	-	1.5	-	kHz
			10V to 15V	-	0.5	-	kHz
-	R_X max	C_X=10uF, V_{DD}=5V		-	-	20	MΩ
		C_X=50uF, V_{DD}=10V		-	-	20	MΩ
		C_X=10uF, V_{DD}=15V		-	-	10	MΩ
-	C_X max	R_X=500kΩ, V_{DD}=5V		-	-	1000	uF
		R_X=300kΩ, V_{DD}=10V		-	-	50	uF
		R_X=300kΩ, V_{DD}=15V		-	-	50	uF
-	Maximum oscillator frequency	C_X=15pF R_S=30kΩ R_X=15kΩ	V_{DD}=10V	530	650	810	kHz
			V_{DD}=15V	690	800	940	kHz
I_{OL}	Drive current at CEXT (for oscillator design)	V_O=0.4V, V_{DD}=5V		0.16	0.35	-	mA
		V_O=0.5V, V_{DD}=10V		0.42	0.8	-	mA
		V_O=1.5V, V_{DD}=15V		1	2	-	mA
I_{OH}		V_O=4.6V, V_{DD}=5V		-0.16	-	-	mA
		V_O=9.5V, V_{DD}=10V		-0.42	-	-	mA
		V_O=13.5V, V_{DD}=15V		-1	-	-	mA

Note: RC oscillator applications are not recommended at supply voltages below 7V for R_X<50kΩ.

8 Detailed Description

8.1 Overview

CD4060 is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, REXT and CEXT), ten buffered outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset input (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q3 to Q9 and Q11 to Q13=LOW), independent of other input conditions.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

8.2 Functional Block Diagram

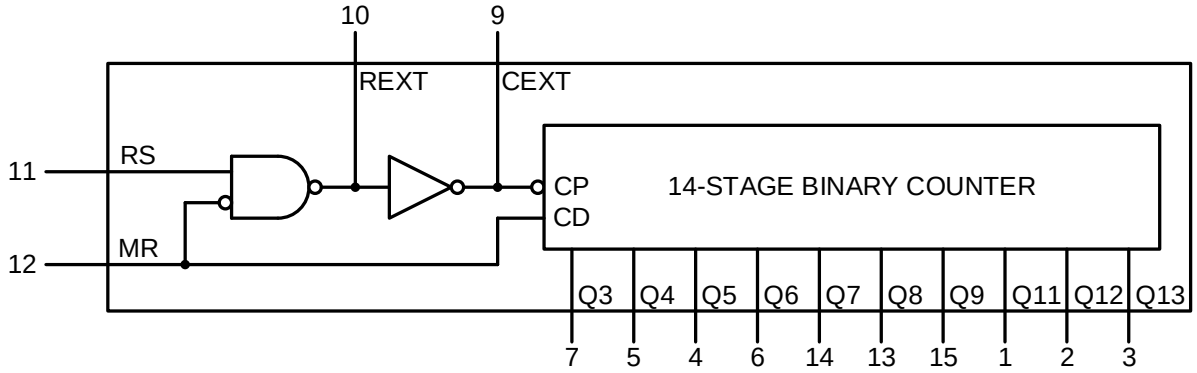


Figure 8-1 Functional diagram

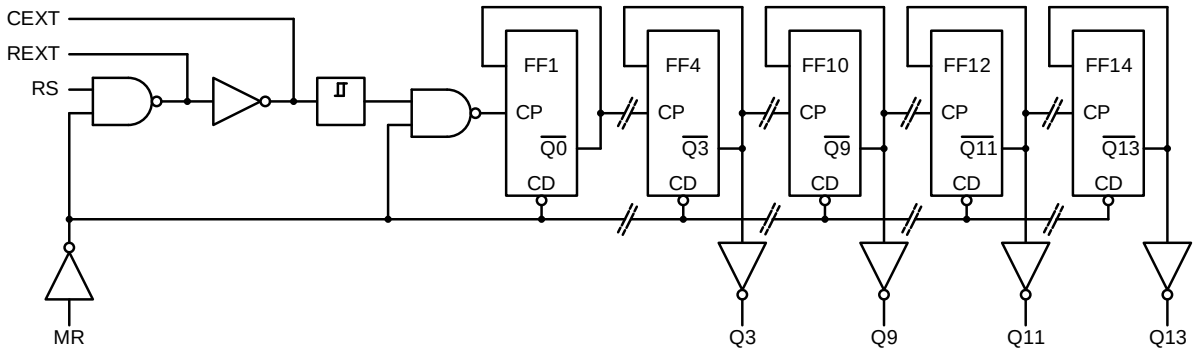


Figure 8-2 Logic diagram

8.3 Function Table

INPUT		OUTPUT
RS	**MR**	**Q3 to Q9 and Q11 to Q13**
↑	L	No change
↓	L	Count
X	H	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

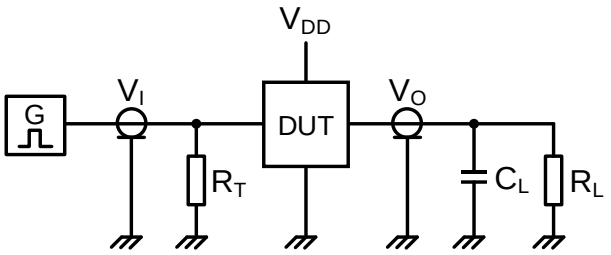


Figure 8-3 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L= Load resistance.

8.4.2 AC Testing Waveforms

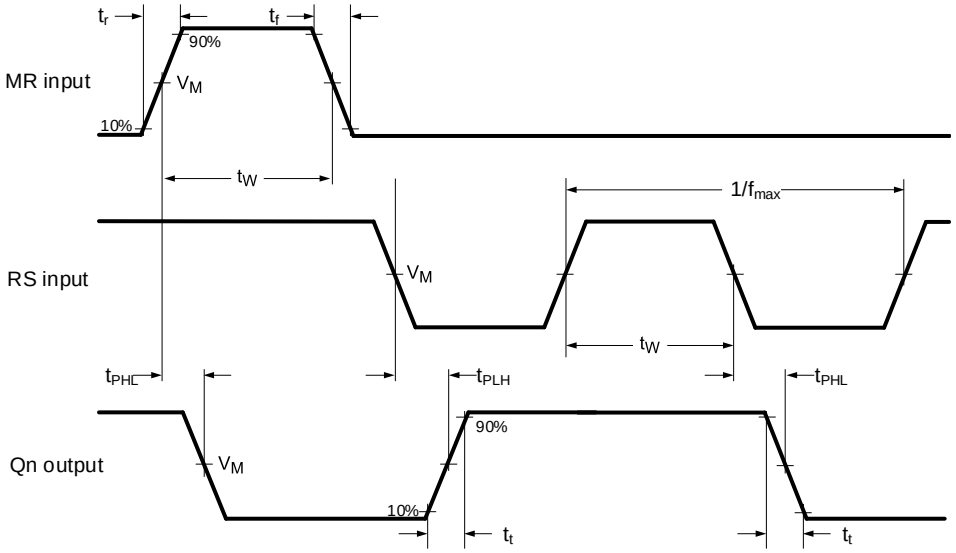


Figure 8-4 Waveforms showing propagation delays

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{DD}	V_M	V_M
5V to 15V	0.5xV_{DD}	0.5xV_{DD}

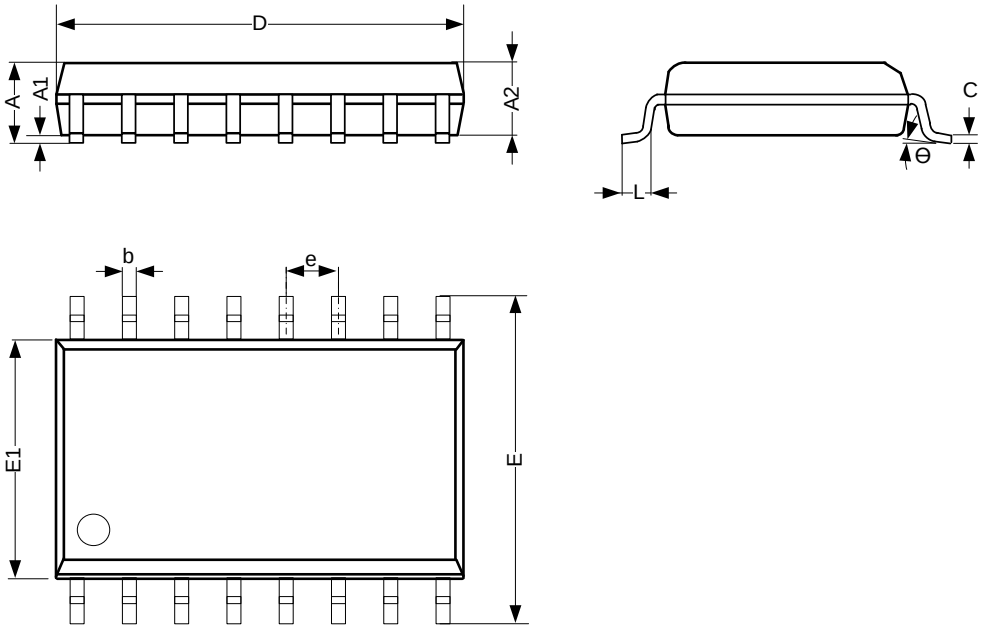
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD
V_{DD}	V_I	t_r , t_f	C_L
5V to 15V	V_{SS} or V_{DD}	≤ 20ns	50pF

9 Mechanical Information

9.1 SOP16 Mechanical Information

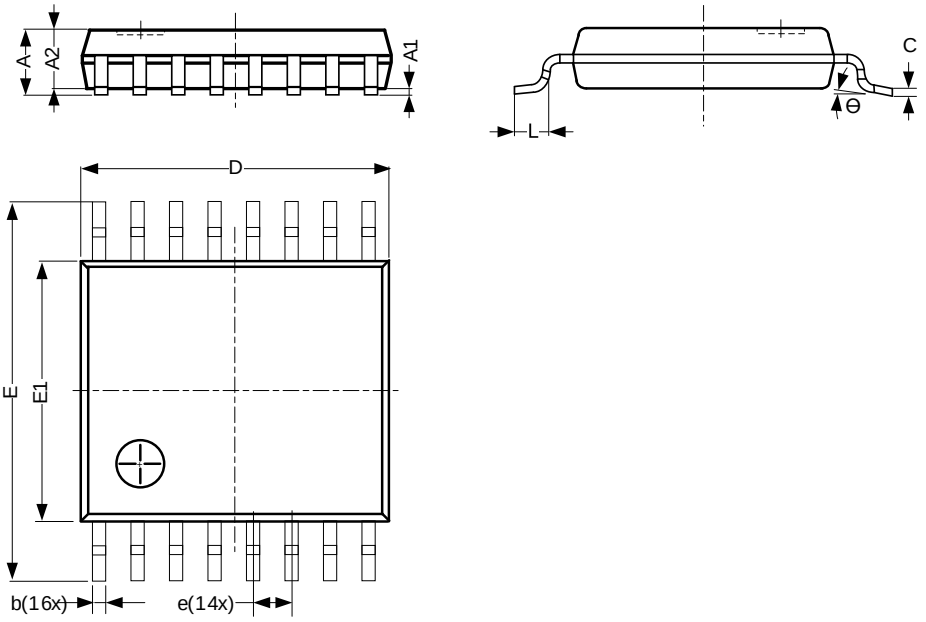
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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