Quad Bilateral Switches

CD4066 Logic

1 Introduction

The CD4066 provides four single-pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

The CD4066 is pin compatible with the CD4016 but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input signal range.

2 Available Packages

PART NUMBER	PACKAGE
CD4066	SOP14
	TSSOP14

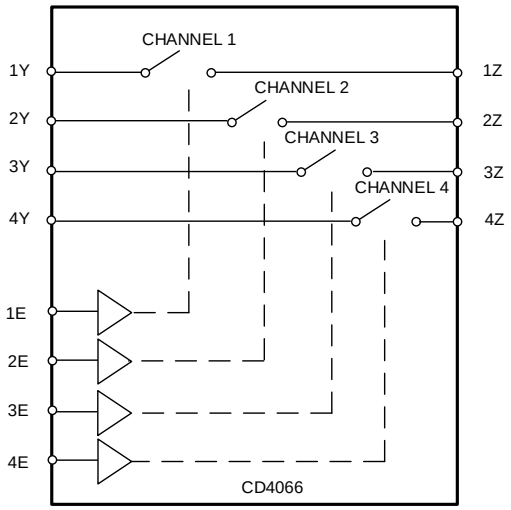
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40°C to +125°C

4 Applications

- Analog signal switching and multiplexing:
  - signal gating, modulators, squelch controls,
  - demodulators, choppers, commutating switches
- Digital signal switching and multiplexing
- Analog-to-digital and digital-to-analog conversions
- Digital control of frequency, impedance, phase, and analog-signal gain
- Building automation



Functional Diagrams

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4066ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CD4066BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

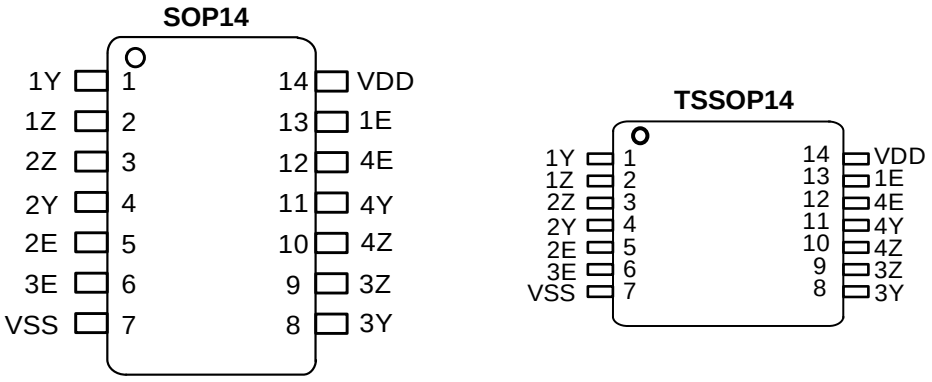


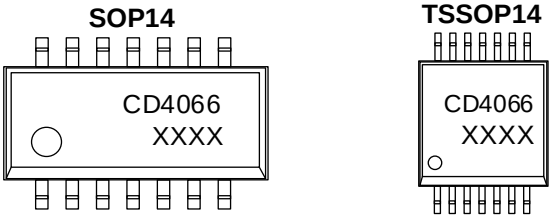
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	1Y	I/O	Independent input or output
2	1Z	I/O	Independent input or output
3	2Z	I/O	Independent input or output
4	2Y	I/O	Independent input or output
5	2E	I	Enable input (active HIGH)
6	3E	I	Enable input (active HIGH)
7	VSS	G	Ground (0V)
8	3Y	I/O	Independent input or output
9	3Z	I/O	Independent input or output
10	4Z	I/O	Independent input or output
11	4Y	I/O	Independent input or output
12	4E	I	Enable input (active HIGH)
13	1E	I	Enable input (active HIGH)
14	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



CD4066: Device number.

XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+12	V
V_I	Input voltage	-		-0.5	V_{DD}+0.5	V
I_{IK}	Input clamping current	V_I<0.5V or V_I>V_{DD}+0.5V		-	±10	mA
$I_{I/O}$	Input/output current	-		-	±10	mA
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

T_{amb}=25°C; R_L=10kΩ; C_L=50pF; nE=V_{DD}; V_{IS}=V_{DD}=5V.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	5	9	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C
V_I	Input voltage	-	0	-	V_{DD}	V
t_{PHZ}	Disable output time（High level→turn off）	nE to nZ or nE to nY	-	80	160	ns
t_{PLZ}	Disable output time（Low level→turn off）	nE to nZ or nE to nY	-	80	160	ns
t_{PZH}, t_{PZL}	Enable output time（turn off→high/low level）	-	-	45	90	ns
C_I	Input capacitance	-	-	-	7.5	pF

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T_{amb}=25°C			UNIT
				MIN.	TYP.	MAX.	
I_{DD}	Supply current	V_I=V_{DD} or V_{SS}, I_O=0A	V_{DD}=5V	-	-	1.0	uA
			V_{DD}=9V	-	-	2.0	uA

V_{IH}	HIGH-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	3.5	-	-	V
			V_{DD}=9V, V_O=0.5V or 8V	7.0	-	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	-	-	1.5	V
			V_{DD}=9V, V_O=0.5V or 8V	-	-	3.0	V
I_I	Input leakage current	V_I=0V or 9V, V_{DD}=9V		-	-	1.0	uA
R_{ON}	ON resistance (rail)	V_I=0V to V_{DD}-V_{EE}	V_{DD}-V_{EE}=5V	-	350	2500	Ω
			V_{DD}-V_{EE}=9V	-	80	245	Ω
		V_I=0V	V_{DD}-V_{EE}=5V	-	115	340	Ω
			V_{DD}-V_{EE}=9V	-	50	160	Ω
		V_I=V_{DD}-V_{EE}	V_{DD}-V_{EE}=5V	-	120	365	Ω
			V_{DD}-V_{EE}=9V	-	65	200	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I=0V to V_{DD}-V_{EE}	V_{DD}-V_{EE}=5V	-	25	-	Ω
			V_{DD}-V_{EE}=9V	-	10	-	Ω

(1) On resistance waveform and test circuit see Figure 8-9 and Figure 8-10.

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T_{amb}=-40°C		T_{amb}=+85°C		UNIT
				MIN.	MAX.	MIN.	MAX.	
I_{DD}	Supply current	V_I=V_{DD} or V_{SS}, I_O=0A	V_{DD}=5V	-	1.0	-	7.5	uA
			V_{DD}=9V	-	2.0	-	15.0	uA
V_{IH}	HIGH-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	3.5	-	3.5	-	V
			V_{DD}=9V, V_O=0.5V or 8V	7.0	-	7.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	-	1.5	-	1.5	V
			V_{DD}=9V, V_O=0.5V or 8V	-	3.0	-	3.0	V
I_I	Input leakage current	V_I=0V or 9V, V_{DD}=9V		-	-	-	1.0	uA

7.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T_{amb}=-40°C		T_{amb}=+125°C		UNIT
				MIN.	MAX.	MIN.	MAX.	
I_{DD}	Supply current	V_I=V_{DD} or V_{SS}, I_O=0A	V_{DD}=5V	-	1.0	-	7.5	uA
			V_{DD}=9V	-	2.0	-	15.0	uA
V_{IH}	HIGH-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	3.5	-	3.5	-	V
			V_{DD}=9V, V_O=0.5V or 8V	7.0	-	7.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	-	1.5	-	1.5	V

			V_{DD}=9V, V_O=0.5V or 8V	-	3.0	-	3.0	V
I_I	Input leakage current	V_I=0V or 9V, V_{DD}=9V		-	-	-	1.0	uA

7.4.4 AC Characteristics 1

T_{amb}=25°C, V_{EE}=V_{SS}=0V, t_r, t_f≤20ns, C_L=50pF, R_L=10kΩ, unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}	HIGH to LOW propagation delay time	nY to nZ; nZ to nY; see Figure 8-4	V_{DD}=5V	-	10	20	ns
			V_{DD}=9V	-	5	10	ns
t_{PLH}	LOW to HIGH propagation delay	nY to nZ; nZ to nY; see Figure 8-4	V_{DD}=5V	-	10	20	ns
			V_{DD}=9V	-	5	10	ns
t_{PHZ}	HIGH to OFF-state propagation delay	nE to nY, nZ; see Figure 8-5	V_{DD}=5V	-	80	160	ns
			V_{DD}=9V	-	65	130	ns
t_{PLZ}	LOW to OFF-state propagation delay	nE to nY, nZ; see Figure 8-5	V_{DD}=5V	-	80	160	ns
			V_{DD}=9V	-	70	140	ns
t_{PZH}	OFF-state to HIGH propagation delay	nE to nY, nZ; see Figure 8-5	V_{DD}=5V	-	40	80	ns
			V_{DD}=9V	-	20	40	ns
t_{PZL}	OFF-state to LOW propagation delay	nE to nY, nZ; see Figure 8-5	V_{DD}=5V	-	45	90	ns
			V_{DD}=9V	-	20	40	ns

7.4.5 AC Characteristics 2

T_{amb}=25°C, V_{EE}=V_{SS}=0V, V_I=0.5V_{DD} (p-p), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
d_{sin}	Square wave distortion	See Figure 8-6; R_L=10kΩ; C_L=15pF; Channel ON; f_i=1kHz	V_{DD}=5V	0.25	-	-	%
			V_{DD}=9V	0.04	-		%
f_{ct}	Any two channel crosstalk	V_{DD}=9V(2)		1	-	-	MHz
V_{ct}	Crosstalk voltage (nE to nY to nZ)	See Figure 8-7; R_L=10kΩ; C_L=15pF; $\overline{E}$ or Sn=V_{DD} (square-wave)		50	-	-	mV
f_{OFF}	OFF frequency	V_{DD}=9V(3)		1	-	-	MHz
f_{ON}	Conduction frequency	V_{DD}=5V(4)		-	-	-	MHz
		V_{DD}=9V(4)		90	-	-	MHz

(1) f_i is biased at 0.5V_{DD}; V_I=0.5V_{DD} (p-p).

(2) R_L=1kΩ; 20logVos/Vis=-50dB, see Figure 8-8.

(3) R_L=1kΩ; C_L=5pF, channel off, 20logVos/Vis=-50dB, see Figure 8-6.

(4) R_L=1kΩ; C_L=5pF, channel on, 20logVos/Vis=-3dB, see Figure 8-6.

8 Detailed Description

8.1 Overview

The CD4066 provides four single-pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

The CD4066 is pin compatible with the CD4016 but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.

8.2 Functional Block Diagram

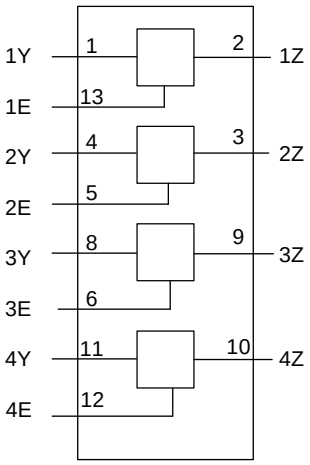


Figure 8-1 Functional diagram

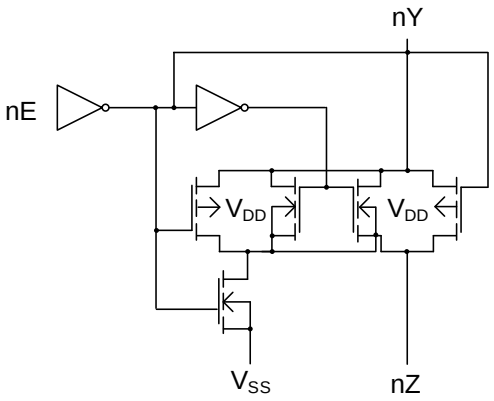


Figure 8-2 Logic diagram (one switch)

8.3 Function Table(1)

INPUT	SWITCH
nE	
H	ON
L	OFF

(1) H=HIGH voltage level; L=LOW voltage level.

8.4 Testing Circuit

8.4.1 AC Testing Circuit 1

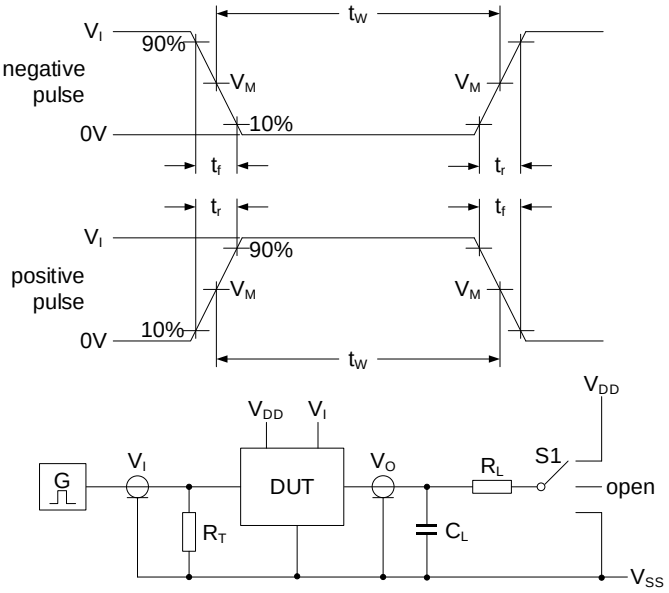


Figure 8-3 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

8.4.2 AC Testing Waveforms

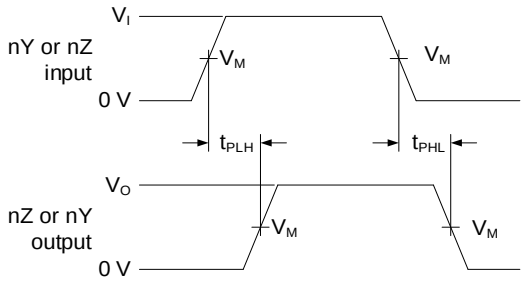


Figure 8-4 nY or nZ to nZ or nY propagation delays

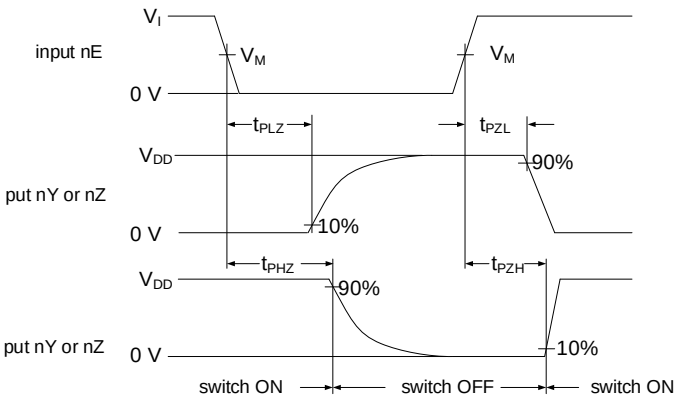


Figure 8-5 Enable and disable times

8.4.3 AC Testing Circuit 2

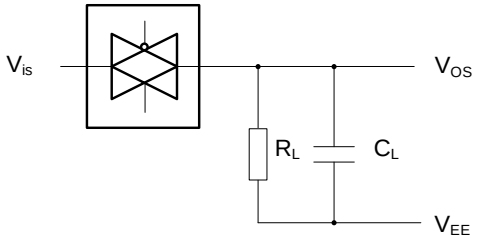


Figure 8-6 Square wave distortion degree of cut-off frequency and conduction frequency test pattern

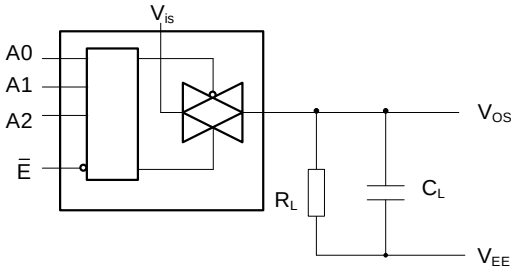
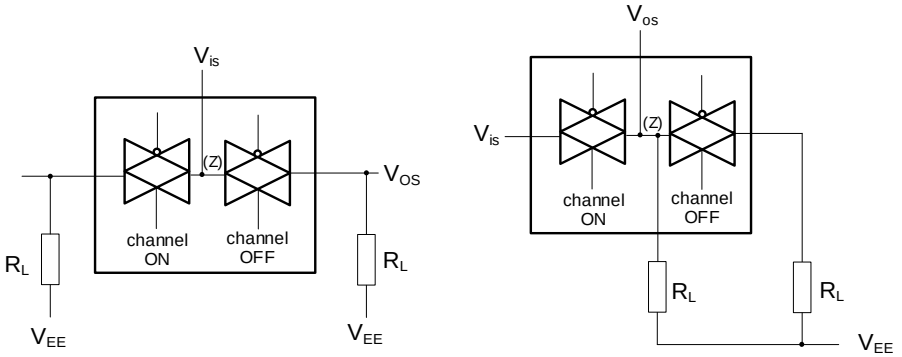


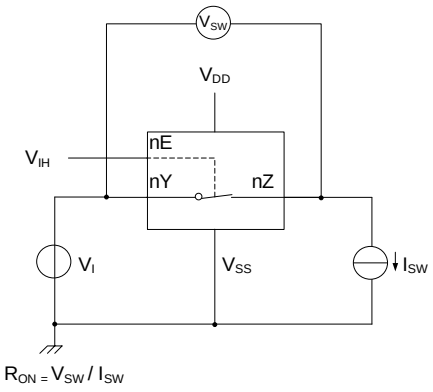
Figure 8-7 Crosstalk logical input/output test



a. channel on b. channel off

Figure 8-8 Inter channel Crosstalk

8.4.4 On Resistance Waveform And Test Circuit



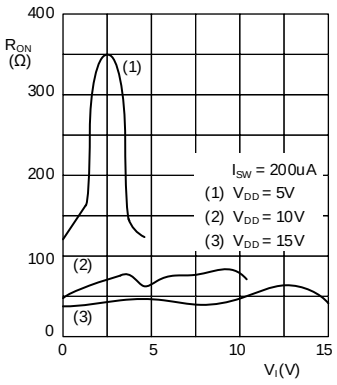


Figure 8-9 Test circuit for measuring R_{ON}

Figure 8-10 Typical R_{ON} as a function of input voltage

8.4.5 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{DD}	V_M	V_M
3V to 9V	0.5xV_{DD}	0.5xV_{DD}

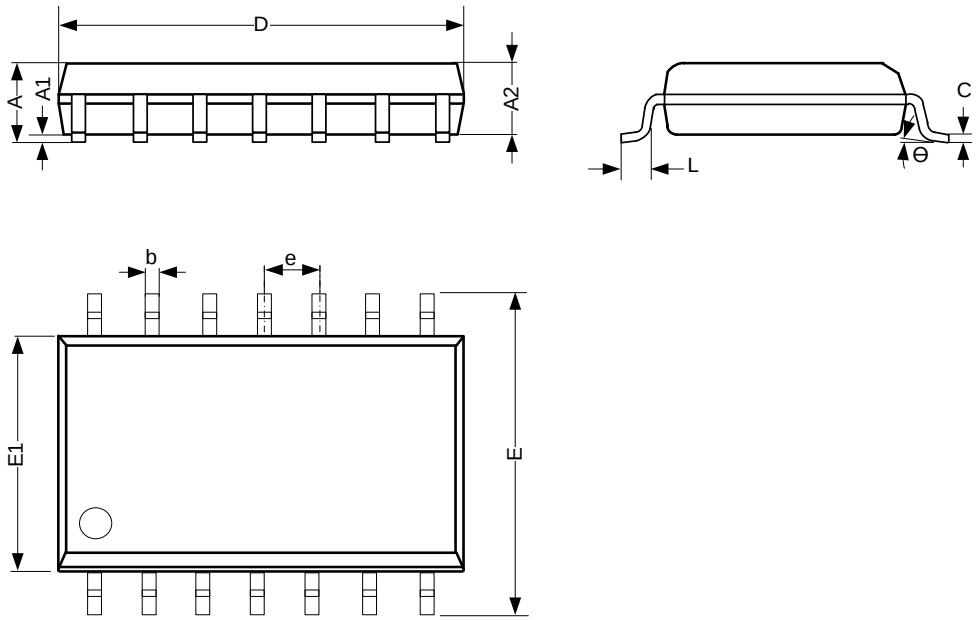
8.4.6 Test Data

TEST	INPUT		LOAD		SWITCH
	V_{is}	t_r, t_f	C_L	R_L	
t_{PHL}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
t_{PLH}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZH}, t_{PHZ}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZL}, t_{PLZ}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
Others	Pulse	20ns	50pF	10kΩ	Open

9 Mechanical Information

9.1 SOP14 Mechanical Information

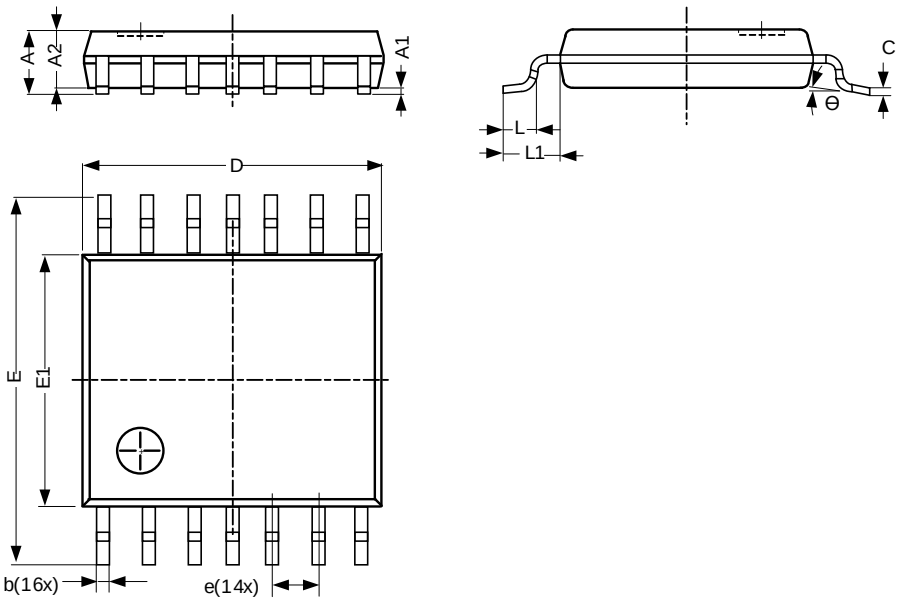
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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