JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

16-channel Analog Multiplexer/Demultiplexer

CD4067

Logic

1 Introduction

The CD4067 is a 16-channel analog

multiplexer/demultiplexer with four address inputs (A0 to A3), an active LOW enable input (/E), sixteen independent inputs/outputs (Y0 to Y15) and a common input/output (Z). The device contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y15) and the other side connected to the common input/output (Z). With /E LOW, one of the sixteen switches is selected (low-impedance ON-state) by A0 to A3. All unselected switches are in the high-impedance OFF-state. With /E HIGH all switches are in the high-impedance OFF-state, independent of A0 to A3. The analog inputs/outputs (Y0 to Y15 and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 9V.

2 Available Packages

PART NUMBER	PACKAGE
CD4067	SOP24
	TSSOP24
	SSOP24(0.65mm)
	SSOP24(0.635mm)

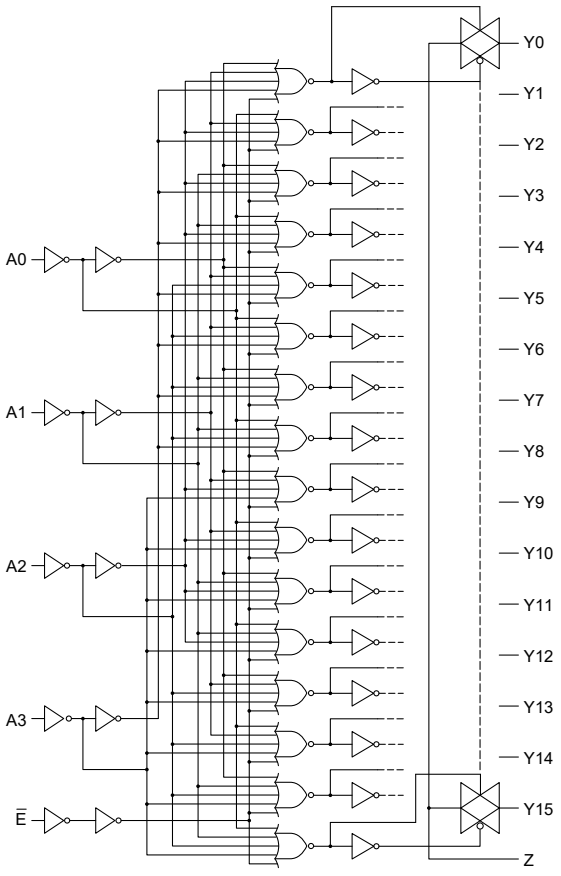
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C

4 Applications

- Analog signal and digital multiplexing
- Transmission-gate logic implementation
- A/DI and D/A conversion
- Signal gating



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4067AHN	SOP24	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 1000 Units/Reel	Active
CD4067BHN	TSSOP24	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CD4067SHN	SSOP24(0.65mm)	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2500 Units/Reel	Active
CD4067SHA	SSOP24(0.635mm)	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

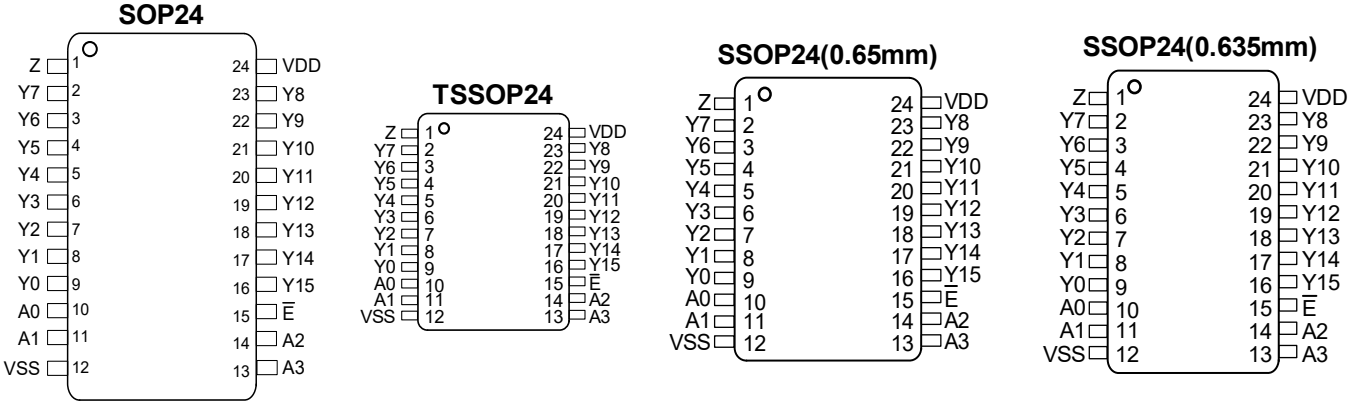


Figure 6-1 Pin configuration

6.2 Pin Function

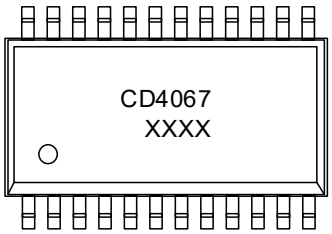
PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	Z	I/O	Common input/output
2	Y7	I/O	Independent input/output
3	Y6	I/O	Independent input/output
4	Y5	I/O	Independent input/output
5	Y4	I/O	Independent input/output
6	Y3	I/O	Independent input/output
7	Y2	I/O	Independent input/output
8	Y1	I/O	Independent input/output
9	Y0	I/O	Independent input/output
10	A0	I	Address input
11	A1	I	Address input
12	VSS	G	Ground (0V)
13	A3	I	Address input
14	A2	I	Address input
15	$\overline{E}$	I	Enable input (active LOW)
16	Y15	I/O	Independent input/output
17	Y14	I/O	Independent input/output
18	Y13	I/O	Independent input/output
19	Y12	I/O	Independent input/output
20	Y11	I/O	Independent input/output
21	Y10	I/O	Independent input/output
22	Y9	I/O	Independent input/output
23	Y8	I/O	Independent input/output

PIN		I/O(1)	DESCRIPTION
No.	NAME		
24	VDD	P	Supply voltage

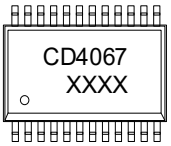
(1) I-Input, O-Output, P-Power, G-Ground.

6.3 Marking Information

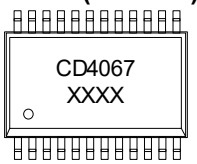
SOP24



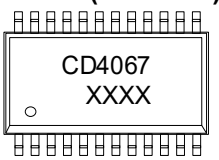
TSSOP24



SSOP24(0.65mm)



SSOP24(0.635mm)



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-	-0.5	+12	V
I_{IK}	Input clamping current	V_I<0.5V or V_I>V_{DD}+0.5V	-	±20	mA
I	Switch current	-	-	±25	mA
V_I	Input voltage	All inputs	-0.5	V_{DD}+0.5	V
T_{stg}	Storage temperature	-	-65	+150	°C
P_{tot}	Total power dissipation	-	-	500	mW
P	Device dissipation	Per output transistor	-	100	mW
T_L	Soldering temperature	10s	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	5	9	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C
V_I	Input voltage	-	0	-	V_{DD}	V
-	Multiplexer switch input current capability	-	-	-	25	mA
-	Output load resistance	-	100	-	-	Ω

7.3 Electrical Characteristics

7.3.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		T_{amb}=25°C			UNIT
				MIN.	TYP.	MAX.	
V_{IL}	LOW-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V; V_O=0.5V or 4.5V	-	-	1.5	V
			V_{DD}=9V; V_O=1.0V or 9V	-	-	3	V
V_{IH}	HIGH-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V; V_O=0.5V or 4.5V	3.5	-	-	V
			V_{DD}=9V; V_O=1.0V or 9V	7	-	-	V
I_I	Input leakage current	V_I=0V or 9V; V_{DD}=9V		-	-	±1	uA
$I_{S(OFF)}$	OFF-state leakage current	V_{SS}=0V; V_{DD}=9V		-	-	±100	nA
I_{DD}	Supply current	All valid input combinations; I_O=0A	V_{DD}=5V	-	-	5	uA
			V_{DD}=9V	-	-	10	uA
C_I	Input capacitance	Any address or inhibit input		-	5	7.5	pF
R_{ON}	ON resistance	V_{SS}≤V_{is}≤V_{DD}	V_{DD}=5V	-	470	1050	Ω
			V_{DD}=9V	-	180	400	Ω
ΔR_{ON}	Change in on-state resistance between channels	-	V_{DD}=5V	-	15	-	Ω
			V_{DD}=9V	-	10	-	Ω

7.3.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		T_{amb}=-40°C		T_{amb}=+85°C		T_{amb}=+125°C		UNIT
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IL}	LOW-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V; V_O=0.5V or 4.5V	-	1.5	-	1.5	-	1.5	V
			V_{DD}=9V; V_O=1.0V or 9V	-	3	-	3	-	3	V
V_{IH}	HIGH-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V; V_O=0.5V or 4.5V	3.5	-	3.5	-	3.5	-	V
			V_{DD}=9V; V_O=1.0V or 9V	7	-	7	-	7	-	V
I_I	Input leakage current	V_I=0V or 9V, V_{DD}=9V		-	±1	-	±1	-	±1	uA
$I_{S(OFF)}$	OFF-state leakage current	V_{SS}=0V; V_{DD}=9V		-	±100	-	±1000	-	±1000	nA
I_{DD}	Supply current	All valid input combinations; I_O=0A	V_{DD}=5V	-	5	-	150	-	150	uA
			V_{DD}=9V	-	10	-	300	-	300	uA
R_{ON}	ON resistance	V_{SS}≤V_{is}≤V_{DD}	V_{DD}=5V	-	850	-	1200	-	1300	Ω
			V_{DD}=9V	-	330	-	520	-	550	Ω

7.3.3 AC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}	HIGH to LOW propagation delay time	Yn, Z to Z, Yn; See Figure 8-5	V_{DD}=5V	-	30	60	ns
			V_{DD}=9V	-	15	30	ns
t_{PLH}	LOW to HIGH propagation delay	Yn, Z to Z, Yn; See Figure 8-5	V_{DD}=5V	-	30	60	ns
			V_{DD}=9V	-	15	30	ns
t_{PHL}	HIGH to LOW propagation delay time	An to Z, Yn; See Figure 8-6	V_{DD}=5V	-	190	380	ns
			V_{DD}=9V	-	70	140	ns
t_{PLH}	LOW to HIGH propagation delay	An to Z, Yn; See Figure 8-6	V_{DD}=5V	-	175	350	ns
			V_{DD}=9V	-	70	140	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{E}$ to Yn, Z; See Figure 8-7	V_{DD}=5V	-	325	650	ns
			V_{DD}=9V	-	135	270	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{E}$ to Yn, Z; See Figure 8-7	V_{DD}=5V	-	325	650	ns
			V_{DD}=9V	-	135	270	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{E}$ to Yn, Z; See Figure 8-7	V_{DD}=5V	-	220	440	ns
			V_{DD}=9V	-	90	180	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{E}$ to Yn, Z; See Figure 8-7	V_{DD}=5V	-	220	440	ns
			V_{DD}=9V	-	90	180	ns

7.3.4 AC Characteristics 2

T_{amb}=25°C , voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$f_{(-3dB)}$	-3dB frequency response	V_{is}=5V; V_{DD}=9V; R_L=1kΩ; See Figure 8-9	V_{os} at Z	-	14	-	MHz
			V_{os} at any channel	-	60	-	MHz
THD	Total harmonic distortion	f_{is}=1kHz sine wave; See Figure 8-8	V_{is}=2V; V_{DD}=5V; R_L=10kΩ	-	0.3	-	%
			V_{is}=3V; V_{DD}=9V; R_L=10kΩ	-	0.2	-	%
$f_{(-40dB)}$	-40dB feed through frequency	V_{is}=5V; V_{DD}=9V; R_L=1kΩ; All channel off	V_{os} at Z	-	20	-	MHz
			V_{os} at any channel	-	8	-	MHz
X_{talk}	Crosstalk	V_{is}=5V; V_{DD}=9V; R_L=1kΩ; Frequency at -40dB; Between any 2 channels; See Figure 8-11		-	1	-	MHz
V_{ct}	Crosstalk voltage	V_{DD}=9V; R_L=10kΩ; V_C=V_{DD}-V_{SS} (square wave); See Figure 8-10		-	75	-	mV

Note:

(1) 20log (V_{os}/V_{is}) =-3dB.

(2) 20log (V_{os}/V_{is}) =-40dB.

(3) Peak-to-peak voltage symmetrical about (V_{DD}-V_{SS})/2.

8 Detailed Description

8.1 Overview

The CD4067 is a 16-channel analog multiplexer/demultiplexer with four address inputs (A0 to A3), an active LOW enable input (/E), sixteen independent inputs/outputs (Y0 to Y15) and a common input/output (Z). The device contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y15) and the other side connected to the common input/output (Z). With /E LOW, one of the sixteen switches is selected (low-impedance ON-state) by A0 to A3. All unselected switches are in the high-impedance OFF-state. With /E HIGH all switches are in the high-impedance OFF-state, independent of A0 to A3. The analog inputs/outputs (Y0 to Y15 and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 9V.

8.2 Functional Block Diagram

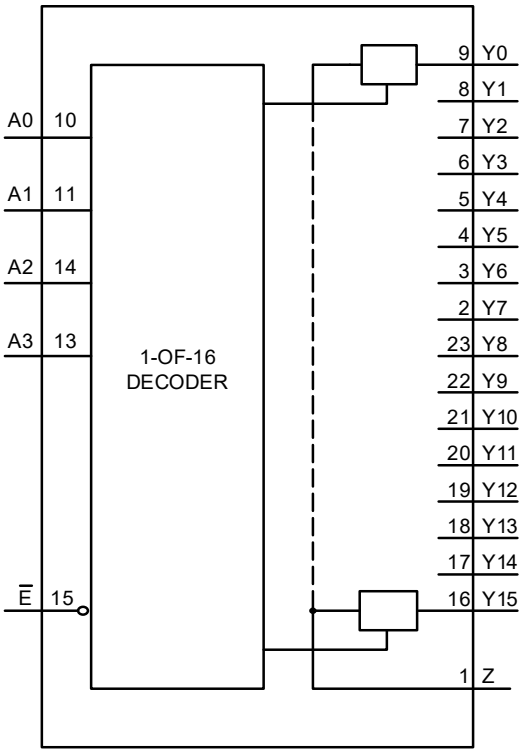


Figure 8-1 Functional diagram

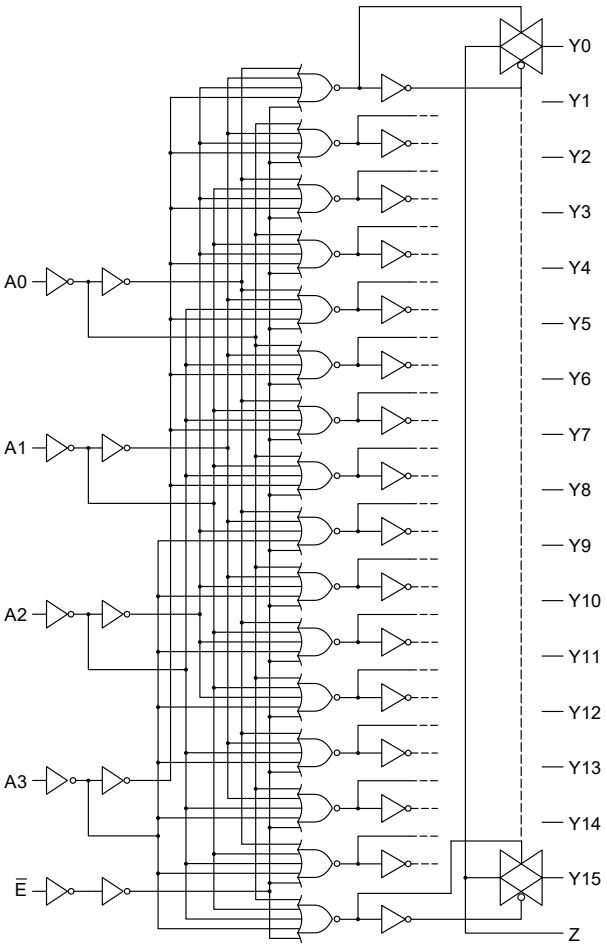


Figure 8-2 Logic diagram

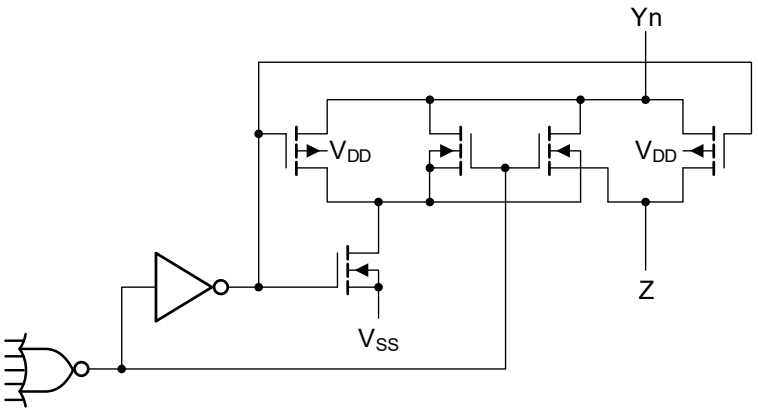


Figure 8-3 Schematic diagram (one switch)

8.3 Function Table

INPUT					CHANNEL ON
$\bar{E}$	A3	A2	A1	A0	
L	L	L	L	L	Y0=Z
L	L	L	L	H	Y1=Z
L	L	L	H	L	Y2=Z
L	L	L	H	H	Y3=Z
L	L	H	L	L	Y4=Z
L	L	H	L	H	Y5=Z
L	L	H	H	L	Y6=Z
L	L	H	H	H	Y7=Z
L	H	L	L	L	Y8=Z
L	H	L	L	H	Y9=Z
L	H	L	H	L	Y10=Z
L	H	L	H	H	Y11=Z
L	H	H	L	L	Y12=Z
L	H	H	L	H	Y13=Z
L	H	H	H	L	Y14=Z
L	H	H	H	H	Y15=Z
H	X	X	X	X	None

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

8.4 Testing Circuit

8.4.1 AC Testing Circuit 1

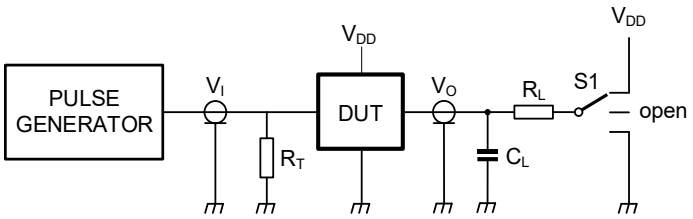


Figure 8-4 Test circuit for switching times

Definitions for test circuit:

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

S1=Test selection switch.

8.4.2 AC Testing Waveforms

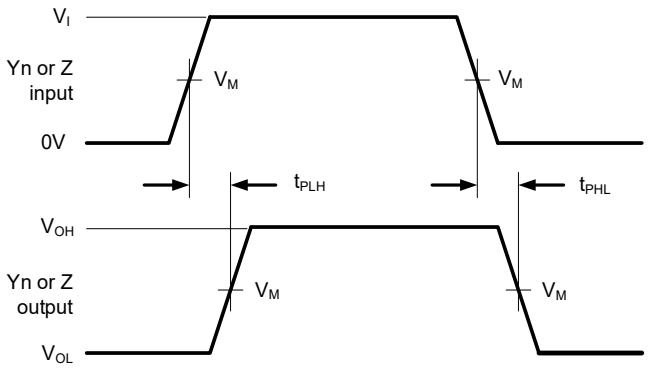


Figure 8-5 Yn, Z to Z, Yn propagation delays

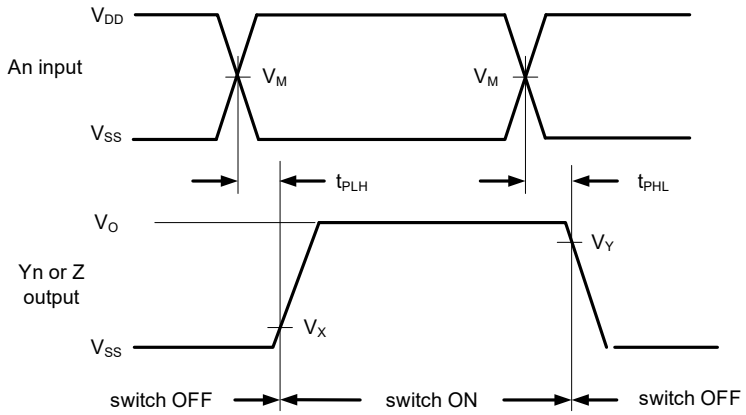


Figure 8-6 An to Yn, Z propagation delays

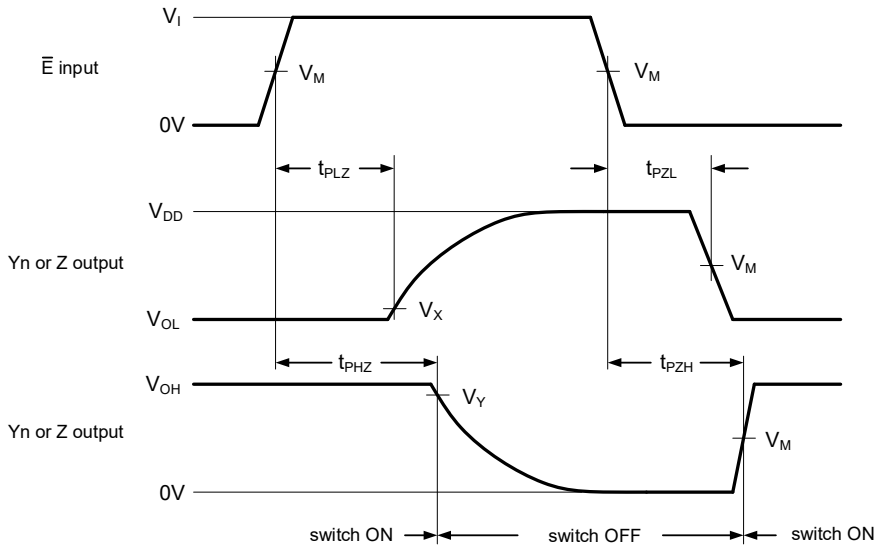


Figure 8-7 Enable and disable times

8.4.3 AC Testing Circuit 2

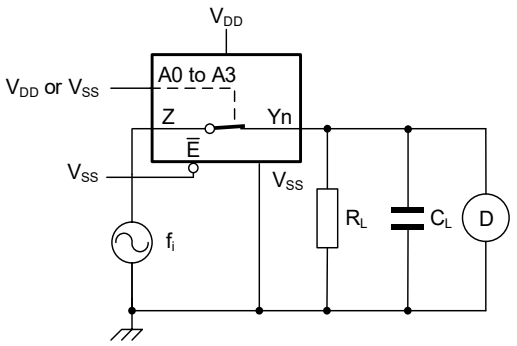


Figure 8-8 Test circuit for measuring total harmonic distortion

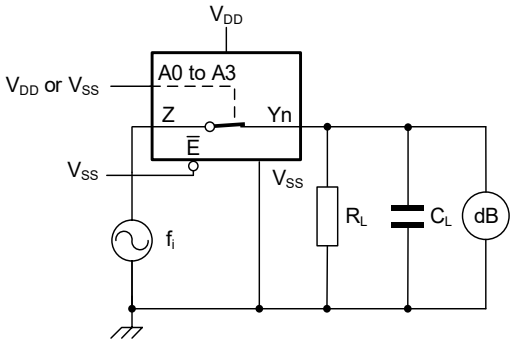
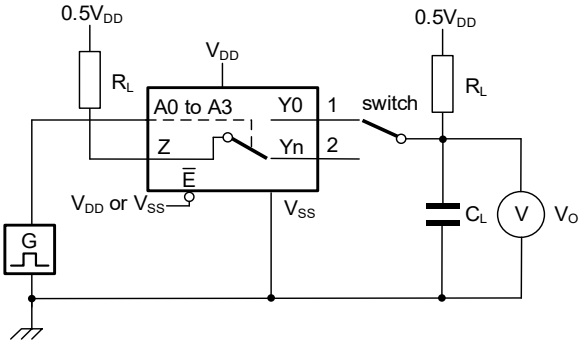
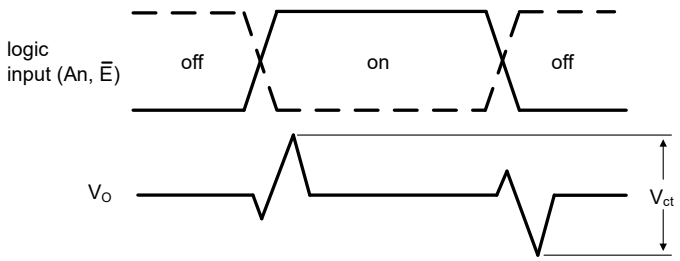


Figure 8-9 Test circuit for measuring frequency response

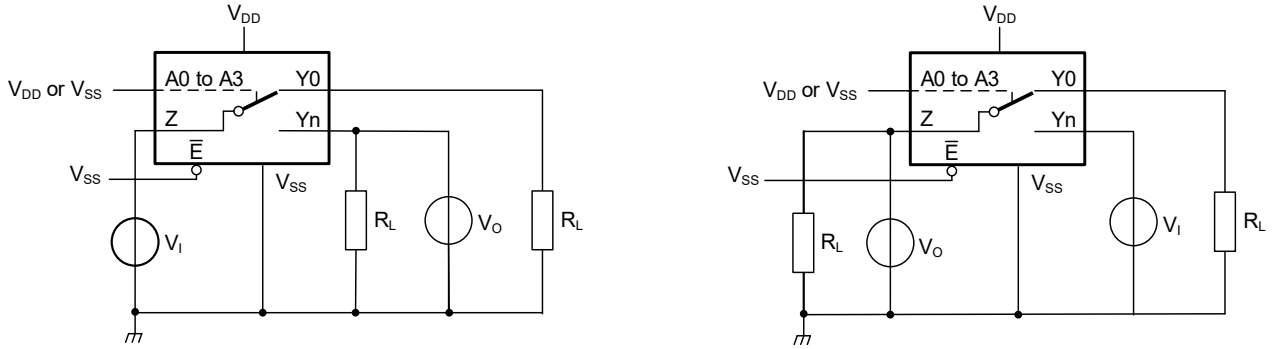


a. Test circuit



b. Input and output pulse definitions

Figure 8-10 Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition

b. Switch open condition

Figure 8-11 Test circuit for measuring crosstalk between switches

8.4.4 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{DD}	V_M	V_M
3V to 9V	0.5xV_{DD}	0.5xV_{DD}

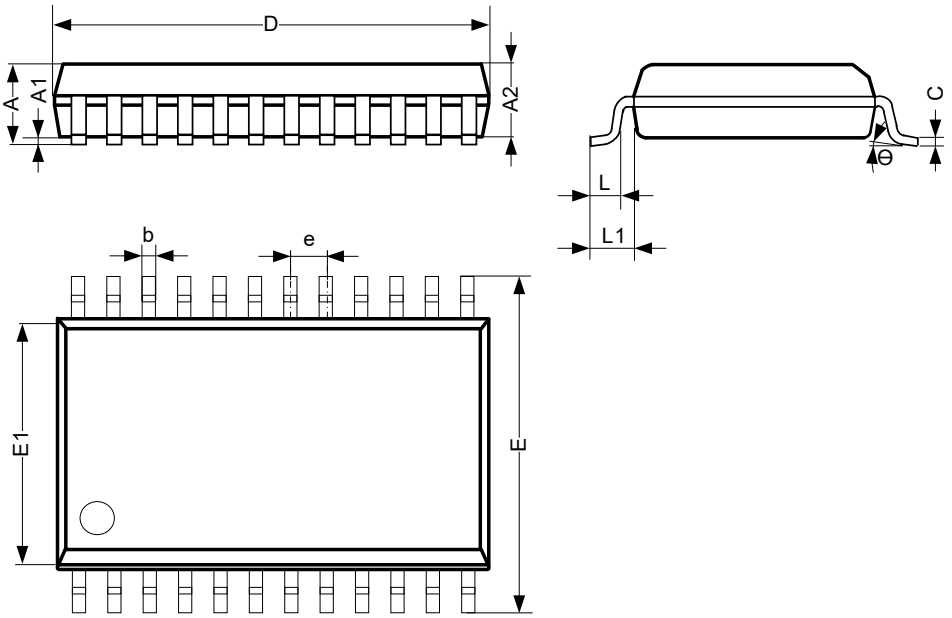
8.4.5 Test Data

TEST	INPUT		LOAD		S1 POSITION
	V_M	t_r, t_f	C_L	R_L	
t_{PHL}	0.5xV_{DD}	≤20ns	50pF	10kΩ	V_{DD} or V_{SS}
t_{PLH}	0.5xV_{DD}	≤20ns	50pF	10kΩ	V_{SS}
t_{PZH}, t_{PHZ}	0.5xV_{DD}	≤20ns	50pF	10kΩ	V_{SS}
t_{PZL}, t_{PLZ}	0.5xV_{DD}	≤20ns	50pF	10kΩ	V_{DD}
Other	0.5xV_{DD}	≤20ns	50pF	10kΩ	V_{SS}

9 Mechanical Information

9.1 SOP24 Mechanical Information

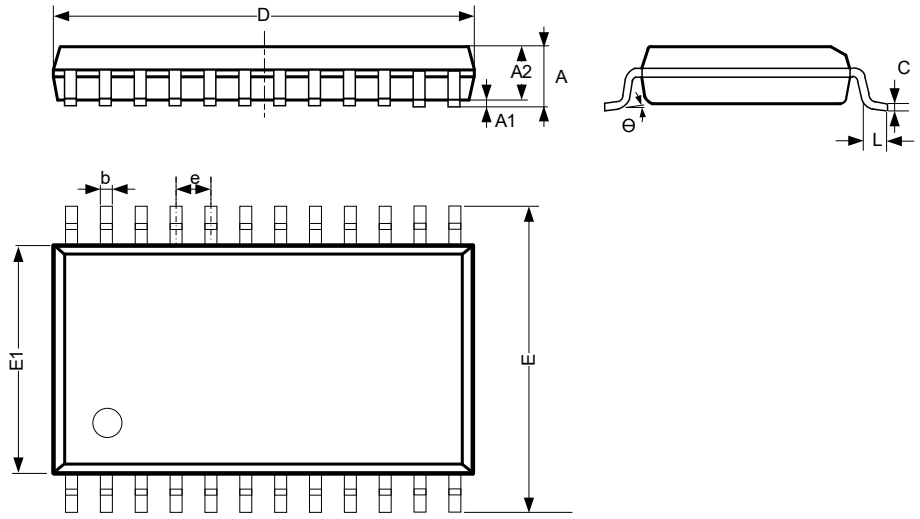
9.1.1 SOP24 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.13	-	2.44
b	0.39	-	0.47
c	0.25	-	0.30
D	15.19	-	15.55
E	10.10	-	10.57
E1	7.40	-	7.62
e	1.27 BSC		
L	0.41	-	1.00
L1	1.30	-	1.50
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP24 Mechanical Information

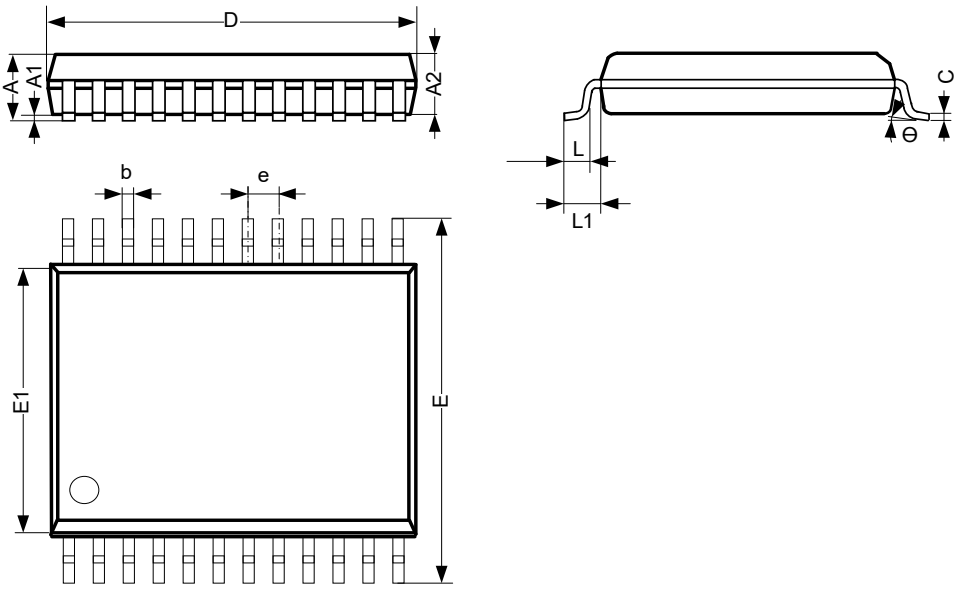
9.2.1 TSSOP24 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	7.70	-	7.90
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
θ	0°	-	8°
Unit: mm			

9.3 SSOP24 (0.65mm) Mechanical Information

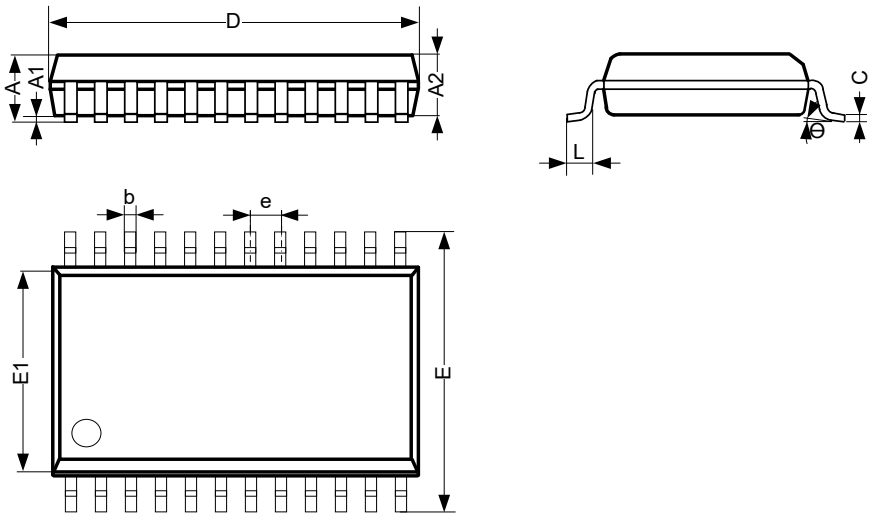
9.3.1 SSOP24 (0.65mm) Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.60	-	2.00
A1	0.05	-	0.25
A2	1.40	-	1.85
b	0.28	-	0.37
c	0.15	-	0.20
D	8.00	-	8.40
E	7.60	-	8.00
E1	5.10	-	5.50
e	0.65 BSC		
L	0.55	-	1.10
L1	1.15	-	1.35
θ	0°	-	8°
Unit: mm			

9.4 SSOP24 (0.635mm) Mechanical Information

9.4.1 SSOP24 (0.635mm) Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.30	-	1.55
b	0.23	-	0.47
c	0.19	-	0.26
D	8.45	-	8.85
E	5.80	-	6.20
E1	3.70	-	4.10
e	0.635 BSC		
L	0.40	-	0.80
θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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