

Hex Inverter

CD4069

Logic

1 Introduction

The CD4069 is a general purpose hex unbuffered inverter. Each inverter has a single stage.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2 Available Packages

PART NUMBER	PACKAGE
CD4069	SOP14
	TSSOP14

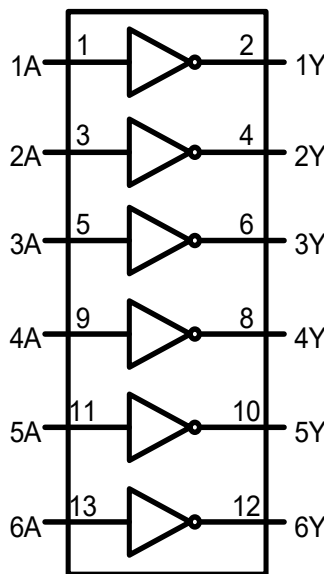
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C

4 Applications

- Logic inversion
- Pulse shaping
- Oscillators
- High-input-impedance amplifiers



Functional diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4069ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CD4069BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

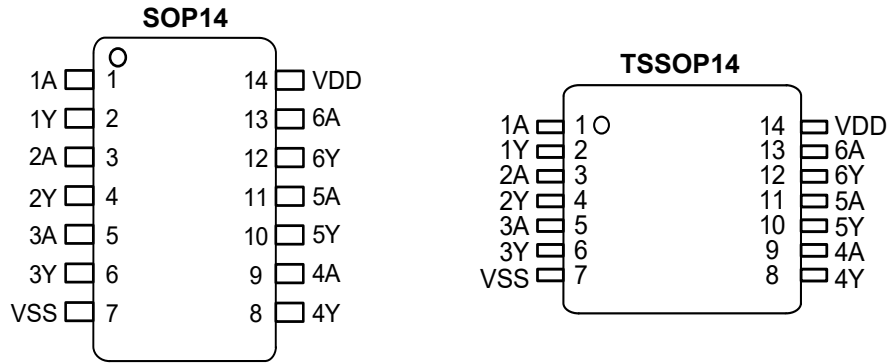


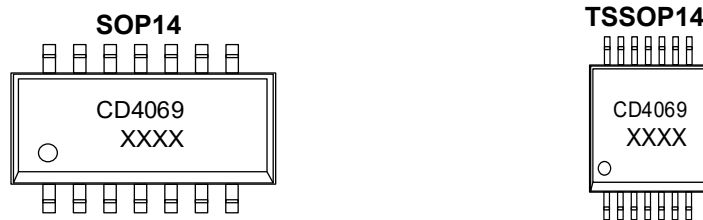
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	1A	I	Data input
2	1Y	O	Data output
3	2A	I	Data input
4	2Y	O	Data output
5	3A	I	Data input
6	3Y	O	Data output
7	VSS	G	Ground (0V)
8	4Y	O	Data output
9	4A	I	Data input
10	5Y	O	Data output
11	5A	I	Data input
12	6Y	O	Data output
13	6A	I	Data input
14	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+18	V
I_{IK}	DC input current	Any one input		-	± 10	mA
V_I	Input voltage	All inputs		-0.5	$V_{DD}+0.5$	V
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	15	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C

7.3 Electrical Characteristics

7.3.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			T _{amb} =25°C			UNIT
		V _O	V _{IN}	V _{DD}	MIN.	TYP.	MAX.	
I _{DD}	Supply current	-	0/5	5	-	-	1	uA
		-	0/10	10	-	-	1	uA
		-	0/15	15	-	-	1	uA
I _{OL}	LOW-level output current	0.4	0/5	5	0.41	-	-	mA
		0.5	0/10	10	0.55	-	-	mA
		1.5	0/15	15	1.7	-	-	mA
I _{OH}	HIGH-level output current	4.6	0/5	5	-0.41	-	-	mA
		2.5	0/5	5	-1.6	-	-	mA
		9.5	0/10	10	-0.65	-	-	mA
		13.5	0/15	15	-2.0	-	-	mA
V _{OL}	LOW-level output voltage	-	0/5	5	-	0	0.05	V
		-	0/10	10	-	0	0.05	V
		-	0/15	15	-	0	0.05	V
V _{OH}	HIGH-level output voltage	-	0/5	5	4.95	5	-	V
		-	0/10	10	9.95	10	-	V
		-	0/15	15	14.95	15	-	V
V _{IL}	LOW-level input voltage	0.5/4.5	-	5	-	-	1	V
		1/9	-	10	-	-	2	V
		1.5/13.5	-	15	-	-	2.5	V
V _{IH}	HIGH-level input voltage	0.5	-	5	4	-	-	V
		1	-	10	8	-	-	V
		1.5	-	15	12.5	-	-	V
I _I	Input leakage current	-	0/15	15	-	-	±1	uA

7.3.2 DC Characteristics 2
 $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			$T_{amb} = -40^{\circ}\text{C}$		$T_{amb} = +85^{\circ}\text{C}$		UNIT
		V_O	V_{IN}	V_{DD}	MIN.	MAX.	MIN.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	7.5	-	7.5	μA
		-	0/10	10	-	15	-	15	μA
		-	0/15	15	-	30	-	30	μA
I_{OL}	LOW-level output current	0.4	0/5	5	0.5	-	0.34	-	mA
		0.5	0/10	10	0.63	-	0.46	-	mA
		1.5	0/15	15	2	-	1.4	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.5	-	-0.34	-	mA
		2.5	0/5	5	-1.8	-	-1.3	-	mA
		9.5	0/10	10	-0.75	-	-0.55	-	mA
		13.5	0/15	15	-2.4	-	-1.65	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0.05	-	0.05	V
		-	0/10	10	-	0.05	-	0.05	V
		-	0/15	15	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	-	4.95	-	V
		-	0/10	10	9.95	-	9.95	-	V
		-	0/15	15	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	1	-	1	V
		1/9	-	10	-	2	-	2	V
		1.5/13.5	-	15	-	2.5	-	2.5	V
V_{IH}	HIGH-level input voltage	0.5	-	5	4	-	4	-	V
		1	-	10	8	-	8	-	V
		1.5	-	15	12.5	-	12.5	-	V
I_I	Input leakage current	-	0/15	15	-	± 10	-	± 10	μA

7.3.3 DC Characteristics 3

$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			$T_{amb} = -40^{\circ}\text{C}$		$T_{amb} = +125^{\circ}\text{C}$		UNIT
		V_O	V_{IN}	V_{DD}	MIN.	MAX.	MIN.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	7.5	-	7.5	μA
		-	0/10	10	-	15	-	15	μA
		-	0/15	15	-	30	-	30	μA
I_{OL}	LOW-level output current	0.4	0/5	5	0.5	-	0.29	-	mA
		0.5	0/10	10	0.63	-	0.38	-	mA
		1.5	0/15	15	2	-	1.2	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.5	-	-0.3	-	mA
		2.5	0/5	5	-1.8	-	-1.15	-	mA
		9.5	0/10	10	-0.75	-	-0.45	-	mA
		13.5	0/15	15	-2.4	-	-1.4	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0.05	-	0.05	V
		-	0/10	10	-	0.05	-	0.05	V
		-	0/15	15	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	-	4.95	-	V
		-	0/10	10	9.95	-	9.95	-	V
		-	0/15	15	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	1	-	1	V
		1/9	-	10	-	2	-	2	V
		1.5/13.5	-	15	-	2.5	-	2.5	V
V_{IH}	HIGH-level input voltage	0.5	-	5	4	-	4	-	V
		1	-	10	8	-	8	-	V
		1.5	-	15	12.5	-	12.5	-	V
I_I	Input leakage current	-	0/15	15	-	± 10	-	± 10	μA

7.3.4 AC Characteristics

$T_{amb}=25^{\circ}C$, $V_{SS}=0V$, $t_r, t_f=20ns$, $C_L=50pF$, $R_L=200k\Omega$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
t_{PHL}, t_{PLH}	Propagation delay time	See Figure 8-4	$V_{DD}=5V$	-	55	110	ns
			$V_{DD}=10V$	-	30	60	ns
			$V_{DD}=15V$	-	25	50	ns
t_{THL}, t_{TLH}	Transition time	See Figure 8-4	$V_{DD}=5V$	-	100	200	ns
			$V_{DD}=10V$	-	50	100	ns
			$V_{DD}=15V$	-	40	80	ns
C_i	Input capacitance	Any input	-	10	15	pF	

8 Detailed Description

8.1 Overview

The CD4069 is a general purpose hex unbuffered inverter. Each inverter has a single stage.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

8.2 Functional Block Diagram

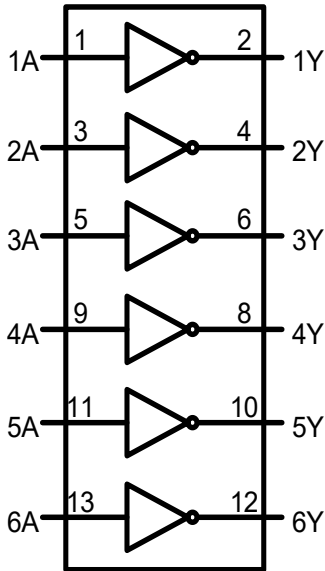


Figure 8-1 Functional diagram

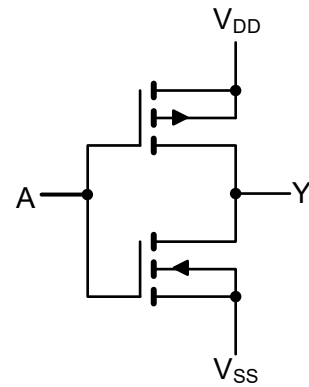


Figure 8-2 Schematic diagram (one inverter)

8.3 Function Table

INPUT	OUTPUT
nA	nY
L	H
H	L

Note: H=HIGH voltage level; L=LOW voltage level.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

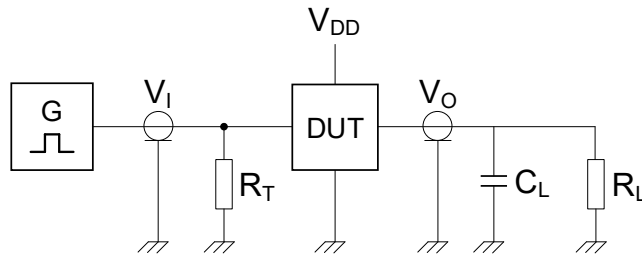


Figure 8-3 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

8.4.2 AC Testing Waveforms

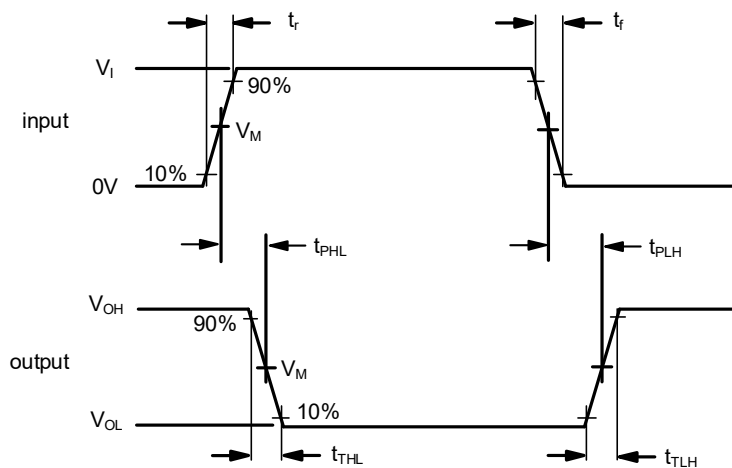


Figure 8-4 Propagation delay, output transition time

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{DD}	V_M	V_M
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

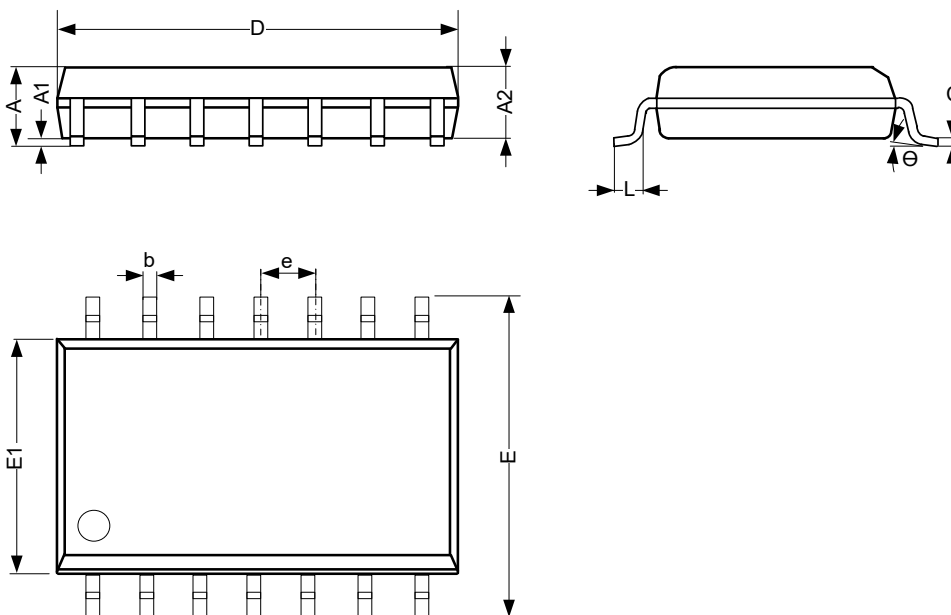
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD
V_{DD}	V_I	t_r, t_f	C_L
5V to 15V	V_{SS} or V_{DD}	$\leq 20ns$	50pF

9 Mechanical Information

9.1 SOP14 Mechanical Information

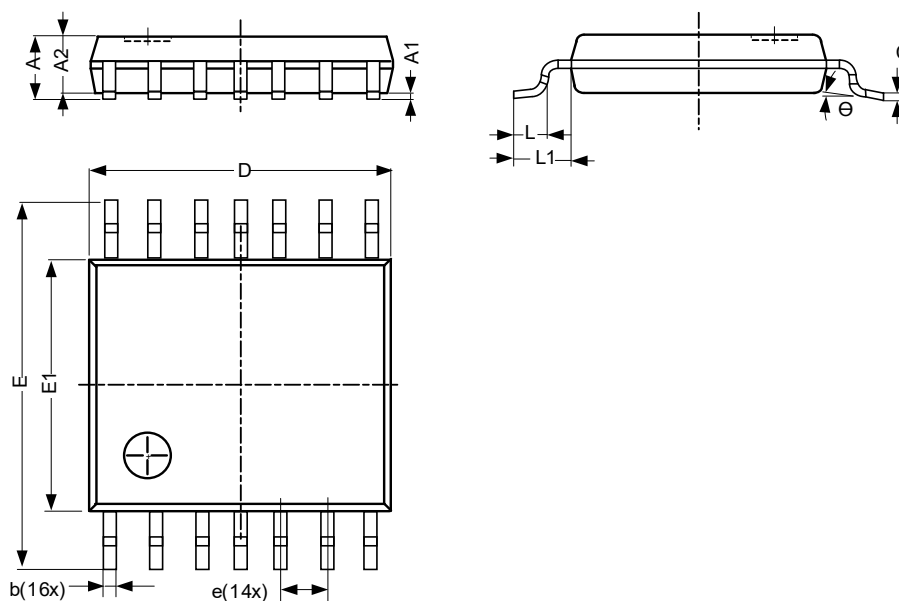
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

Official Website: www.jscj-elec.com

Copyright © JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD