8-stage Shift-and-store Bus Register

CD4094 Logic

1 Introduction

The CD4094 is an 8-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs QP0 to QP7. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (OE) signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of CD4094 devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading CD4094 devices when the clock has a slow rise time.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2 Available Packages

PART NUMBER	PACKAGE
CD4094	SOP16
	TSSOP16

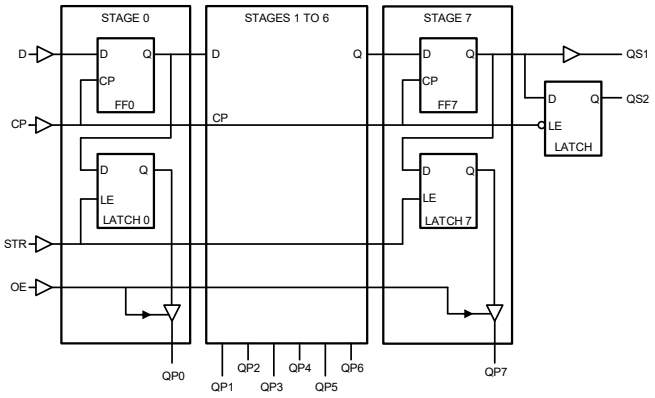
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C

4 Applications

- Serial-to-parallel data conversion
- Remote control holding register
- Dual-rank shift, hold, and bus applications



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4094AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CD4094BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

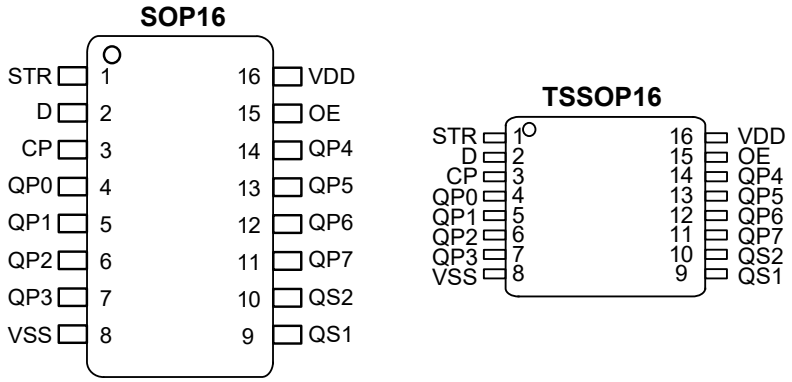


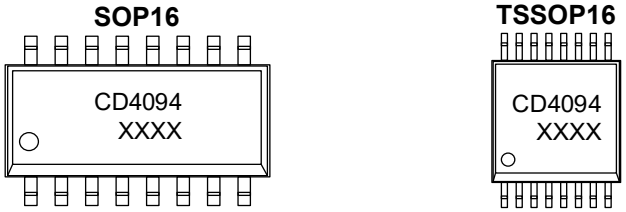
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	STR	I	Strobe input
2	D	I	Data input
3	CP	I	Clock input
4	QP0	O	Parallel output
5	QP1	O	Parallel output
6	QP2	O	Parallel output
7	QP3	O	Parallel output
8	VSS	G	Ground (0V)
9	QS1	O	Serial output
10	QS2	O	Serial output
11	QP7	O	Parallel output
12	QP6	O	Parallel output
13	QP5	O	Parallel output
14	QP4	O	Parallel output
15	OE	I	Output enable input
16	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground.

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+18	V
I_{IK}	DC input current	Any one input		-	±10	mA
V_I	Input voltage	All inputs		-0.5	V_{DD}+0.5	V
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	15	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C
t_{su}	Data setup time	V_{DD}=5V	125	-	-	ns
		V_{DD}=10V	55	-	-	ns
		V_{DD}=15V	35	-	-	ns
t_w	Clock pulse width	V_{DD}=5V	200	-	-	ns
		V_{DD}=10V	100	-	-	ns
		V_{DD}=15V	83	-	-	ns
f_{max}	Clock input frequency	V_{DD}=5V	dc	-	1.25	MHz
		V_{DD}=10V	dc	-	2.5	MHz
		V_{DD}=15V	dc	-	3	MHz
t_{rCL}, t_{fCL}	Clock rise and fall time	V_{DD}=5V	-	-	15	us
		V_{DD}=10V	-	-	5	us
		V_{DD}=15V	-	-	5	us
t_w	Strobe setup time	V_{DD}=5V	200	-	-	ns
		V_{DD}=10V	80	-	-	ns
		V_{DD}=15V	70	-	-	ns

7.3 Electrical Characteristics

7.3.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			T_{amb}=25°C			UNIT
		V_O	V_{IN}	V_{DD}	MIN.	TYP.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	-	5	uA
		-	0/10	10	-	-	10	uA
		-	0/15	15	-	-	20	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.51	1	-	mA
		0.5	0/10	10	1.3	2.6	-	mA
		1.5	0/15	15	3.4	6.8	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.51	-	-	mA
		2.5	0/5	5	-1.6	-	-	mA
		9.5	0/10	10	-1.3	-	-	mA
		13.5	0/15	15	-3.4	-	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0	0.05	V
		-	0/10	10	-	0	0.05	V
		-	0/15	15	-	0	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	5	-	V
		-	0/10	10	9.95	10	-	V
		-	0/15	15	14.95	15	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	-	1.5	V
		1/9	-	10	-	-	3	V
		1.5/13.5	-	15	-	-	4	V
V_{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	-	V
		1/9	-	10	7	-	-	V
		1.5/13.5	-	15	11	-	-	V
I_I	Input leakage current	-	0/15	15	-	-	±1	uA
I_{OZ}	OFF-state output current	0/15	0/15	15	-	-	±1	uA

7.3.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			T_{amb}=-40°C		T_{amb}=+85°C		UNIT
		V_O	V_{IN}	V_{DD}	MIN.	MAX.	MIN.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	5	-	150	uA
		-	0/10	10	-	10	-	300	uA
		-	0/15	15	-	20	-	600	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.61	-	0.42	-	mA
		0.5	0/10	10	1.5	-	1.1	-	mA
		1.5	0/15	15	4	-	2.8	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.61	-	-0.42	-	mA
		2.5	0/5	5	-1.8	-	-1.3	-	mA
		9.5	0/10	10	-1.5	-	-1.1	-	mA
		13.5	0/15	15	-4	-	-2.8	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0.05	-	0.05	V
		-	0/10	10	-	0.05	-	0.05	V
		-	0/15	15	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	-	4.95	-	V
		-	0/10	10	9.95	-	9.95	-	V
		-	0/15	15	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	1.5	-	1.5	V
		1/9	-	10	-	3	-	3	V
		1.5/13.5	-	15	-	4	-	4	V
V_{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	3.5	-	V
		1/9	-	10	7	-	7	-	V
		1.5/13.5	-	15	11	-	11	-	V
I_I	Input leakage current	-	0/15	15	-	±1	-	±1	uA
I_{OZ}	OFF-state output current	0/15	0/15	15	-	±1	-	±12	uA

7.3.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (V)			T_{amb}=-40°C		T_{amb}=+125°C		UNIT
		V_O	V_{IN}	V_{DD}	MIN.	MAX.	MIN.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	5	-	150	uA
		-	0/10	10	-	10	-	300	uA
		-	0/15	15	-	20	-	600	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.61	-	0.36	-	mA
		0.5	0/10	10	1.5	-	0.9	-	mA
		1.5	0/15	15	4	-	2.4	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.61	-	-0.36	-	mA
		2.5	0/5	5	-1.8	-	-1.15	-	mA
		9.5	0/10	10	-1.5	-	-0.9	-	mA
		13.5	0/15	15	-4	-	-2.4	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0.05	-	0.05	V
		-	0/10	10	-	0.05	-	0.05	V
		-	0/15	15	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	-	4.95	-	V
		-	0/10	10	9.95	-	9.95	-	V
		-	0/15	15	14.95	-	14.95	-	V
V_{IL}	LOW-level input voltage	0.5/4.5	-	5	-	1.5	-	1.5	V
		1/9	-	10	-	3	-	3	V
		1.5/13.5	-	15	-	4	-	4	V
V_{IH}	HIGH-level input voltage	0.5/4.5	-	5	3.5	-	3.5	-	V
		1/9	-	10	7	-	7	-	V
		1.5/13.5	-	15	11	-	11	-	V
I_I	Input leakage current	-	0/15	15	-	±1	-	±1	uA
I_{OZ}	OFF-state output current	0/15	0/15	15	-	±1	-	±12	uA

7.3.4 AC Characteristics

T_{amb}=25°C, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200kΩ, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time	CP to QS1; See Figure 8-6	V_{DD}=5V	-	300	600	ns
			V_{DD}=10V	-	125	250	ns
			V_{DD}=15V	-	95	190	ns
		CP to QS2; See Figure 8-6	V_{DD}=5V	-	230	460	ns
			V_{DD}=10V	-	110	220	ns
			V_{DD}=15V	-	75	150	ns

		CP to QPn; See Figure 8-6	V_{DD}=5V	-	420	840	ns
			V_{DD}=10V	-	195	390	ns
			V_{DD}=15V	-	135	270	ns
		STR to QPn; See Figure 8-7	V_{DD}=5V	-	290	580	ns
			V_{DD}=10V	-	145	290	ns
			V_{DD}=15V	-	100	200	ns
t_{PHZ}, t_{PZH}	HIGH to OFF-state/OFF-state to HIGH propagation delay	OE to QPn; See Figure 8-8	V_{DD}=5V	-	140	280	ns
			V_{DD}=10V	-	60	120	ns
			V_{DD}=15V	-	45	90	ns
t_{PLZ}, t_{PZL}	LOW to OFF-state/OFF-state to LOW propagation delay	OE to QPn; See Figure 8-8	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	80	ns
t_W	Pulse width	Minimum HIGH strobe pulse; See Figure 8-7	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	40	80	ns
			V_{DD}=15V	-	35	70	ns
		Minimum LOW clock pulse; See Figure 8-6	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	83	ns
t_{su}	Data setup time	D to CP; See Figure 8-9	V_{DD}=5V	-	60	125	ns
			V_{DD}=10V	-	30	55	ns
			V_{DD}=15V	-	20	35	ns
t_t	Transition time	-	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	80	ns
t_{rCL}, t_{fCL}	Clock input rise and fall time	-	V_{DD}=5V	15	-	-	us
			V_{DD}=10V	5	-	-	us
			V_{DD}=15V	5	-	-	us
f_{max}	Maximum clock frequency	See Figure 8-6	V_{DD}=5V	1.25	2.5	-	MHz
			V_{DD}=10V	2.5	5	-	MHz
			V_{DD}=15V	3	6	-	MHz
C_I	Input capacitance	Any input		-	5	7.5	pF

Note: t_t is the same as t_{TLH} and t_{THL}.

8 Detailed Description

8.1 Overview

The CD4094 is an 8-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs QP0 to QP7. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (OE) signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of CD4094 devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading CD4094 devices when the clock has a slow rise time.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

8.2 Functional Block Diagram

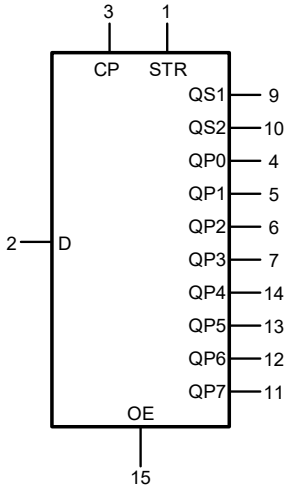


Figure 8-1 Logic symbol

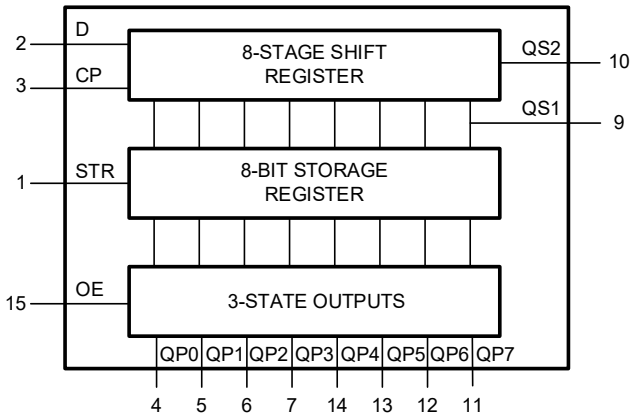


Figure 8-2 Functional diagram

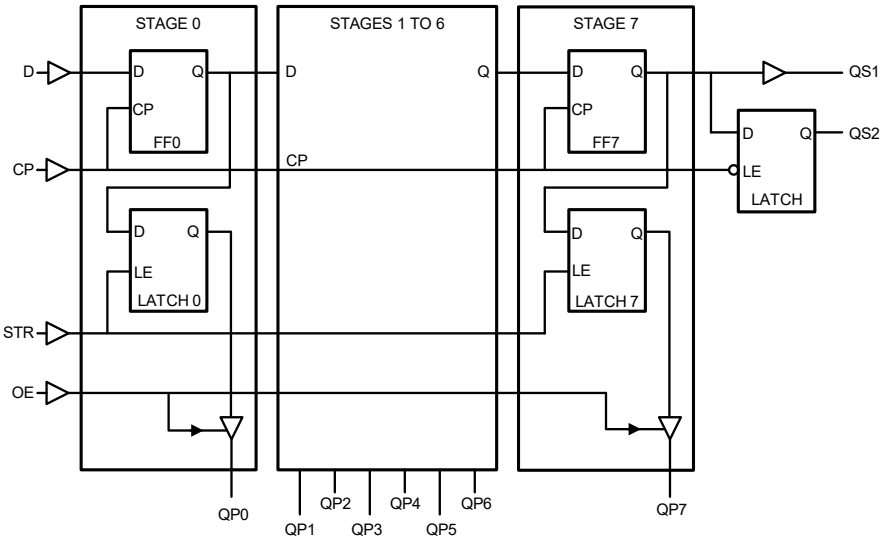


Figure 8-3 Logic diagram

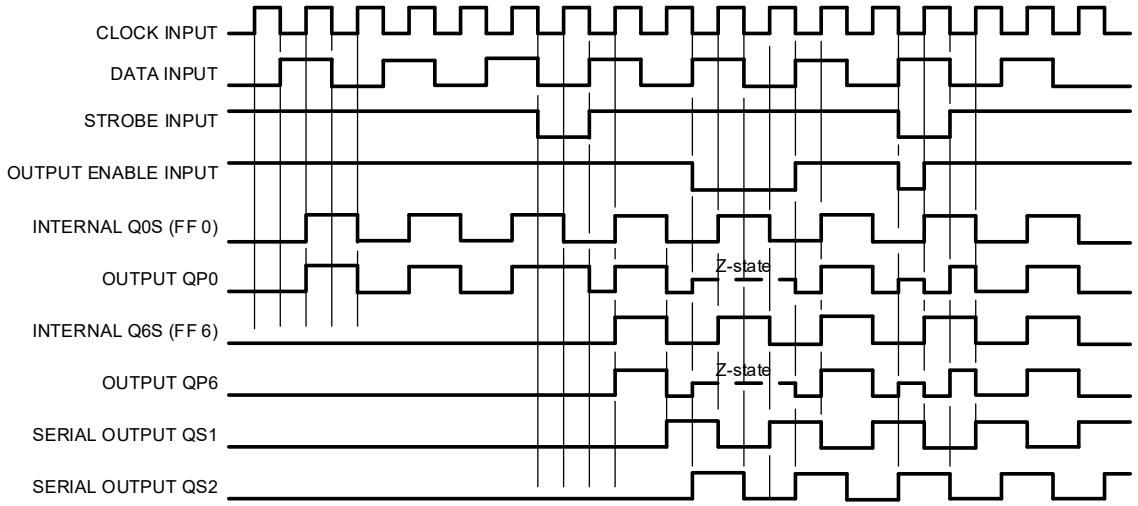


Figure 8-4 Timing diagram

8.3 Function Table

INPUT				PARALLEL OUTPUT		SERIAL OUTPUT	
CP	**OE**	**STR**	**D**	**QP0**	**QPn**	**QS1**	**QS2**
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn-1	Q6S	NC
↑	H	H	H	H	QPn-1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

Note:

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=HIGH-impedance OFF-state;

(2) NC=no change; ↑=positive-going transition; ↓=negative-going transition;

(3) Q6S=the data in register stage 6 before the LOW to HIGH clock transition;

(4) Q7S=the data in register stage 7 before the HIGH to LOW clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

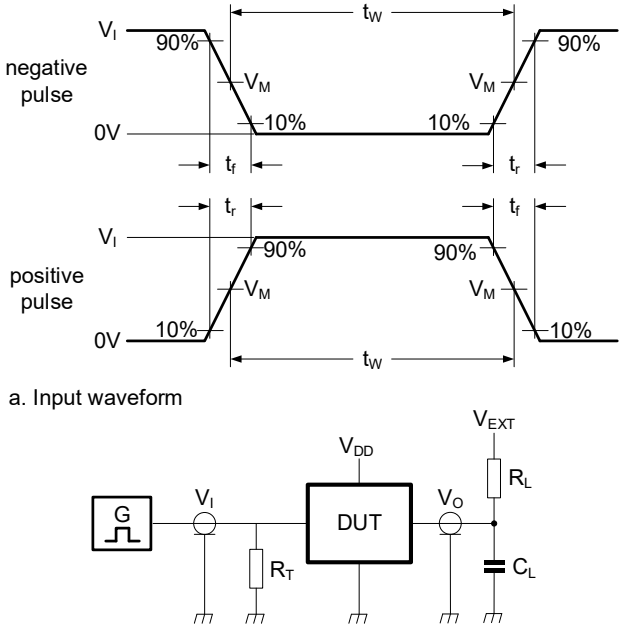


Figure 8-5 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

V_{EXT}=External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

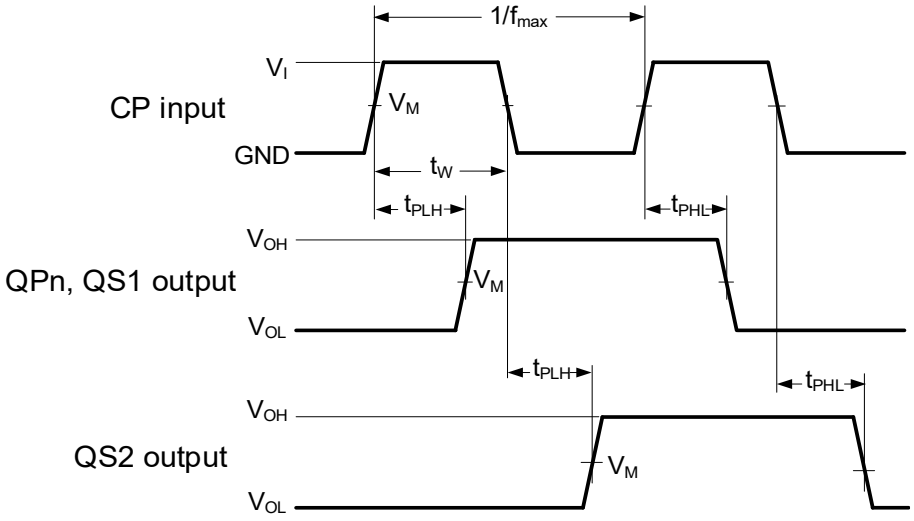


Figure 8-6 Clock to outputs propagation delays, and clock pulse width and maximum frequency

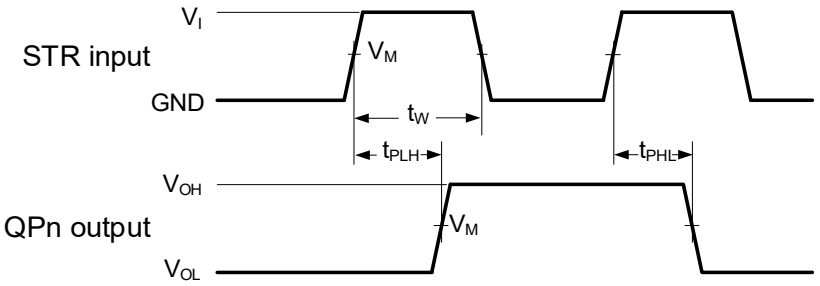


Figure 8-7 Strobe to output propagation delays, and strobe pulse width, set up and hold times

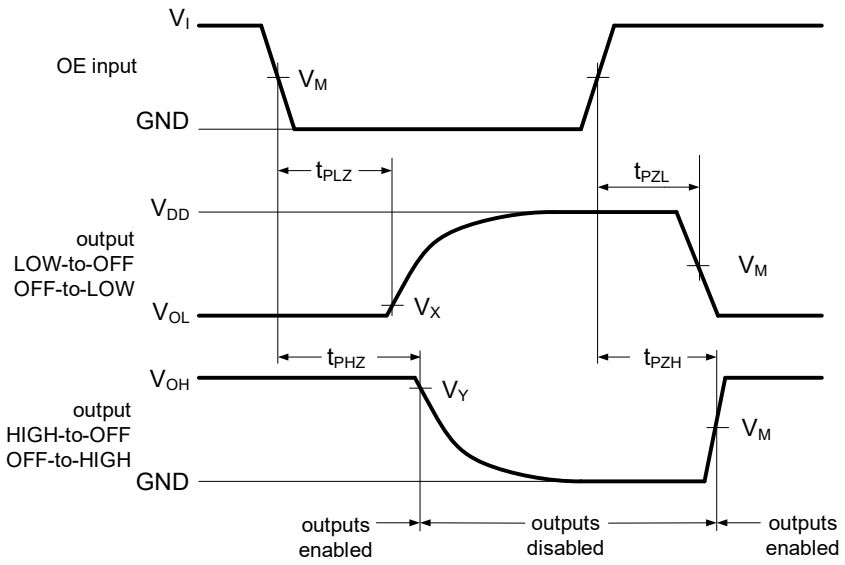


Figure 8-8 3-state output enable and disable times for OE input

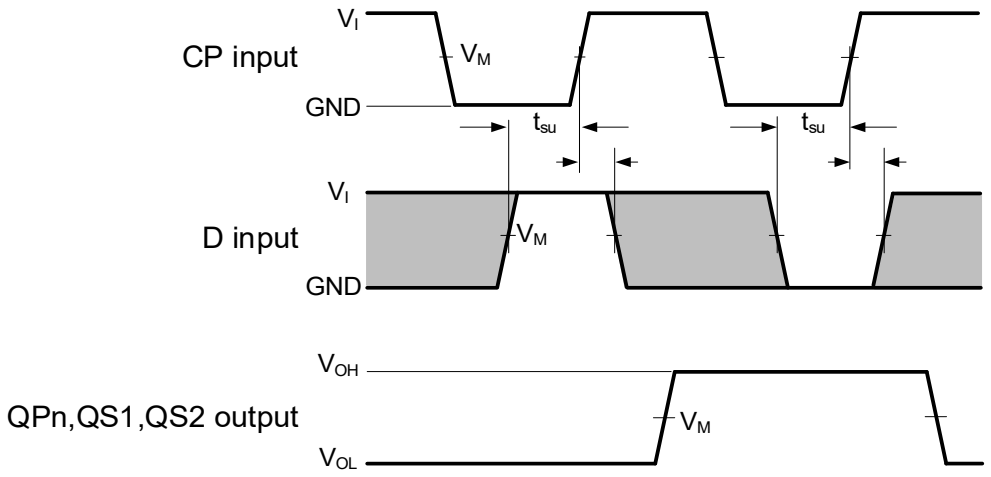


Figure 8-9 Data input data set up and hold times

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT		
V_{DD}	V_M	V_M	V_X	V_Y
5V to 15V	0.5xV_{DD}	0.5xV_{DD}	0.1xV_{DD}	0.9xV_{DD}

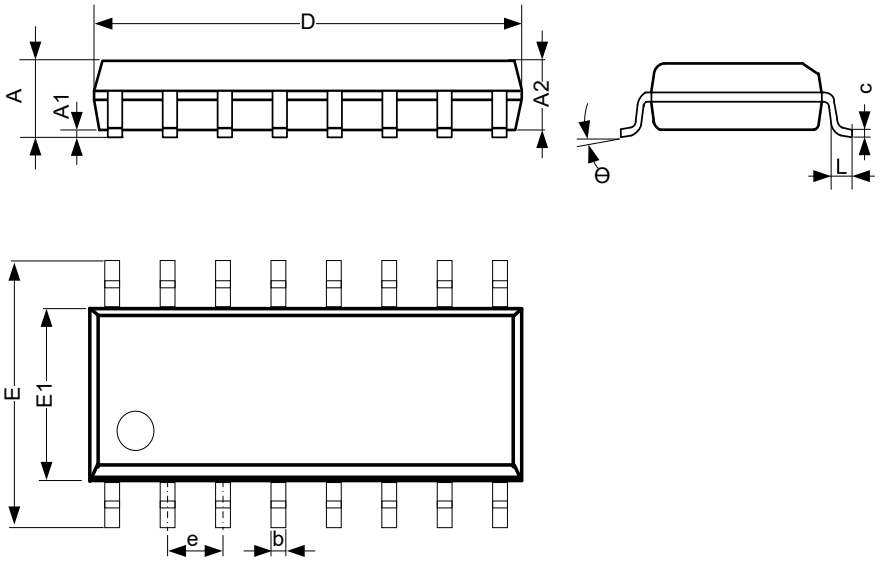
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{DD}	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}
5V to 15V	V_{SS} or V_{DD}	≤ 20ns	50pF	1kΩ	Open	V_{SS}	V_{DD}

9 Mechanical Information

9.1 SOP16 Mechanical Information

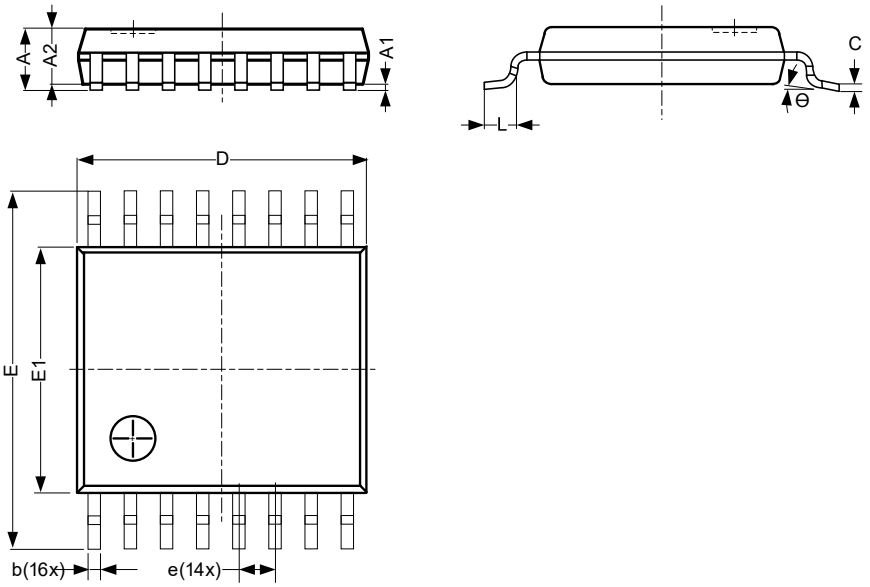
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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