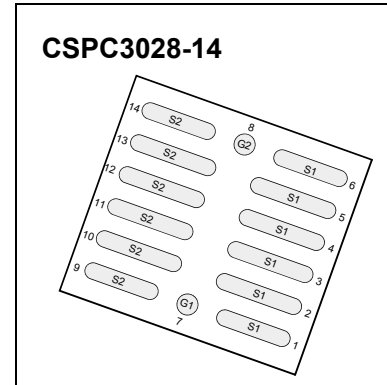




CSP Enhancement Mode Power MOSFET

CJ12209SP-A Dual N-Channel MOSFET

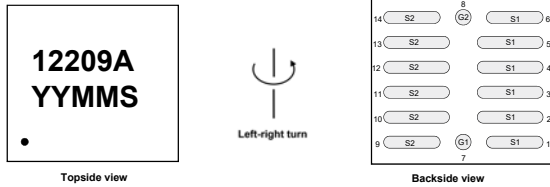
V _{SSS}	R _{SS(on)} TYP	I _S
12V	1.0mΩ@4.5V	20A
	1.1mΩ@3.8V	
	1.2mΩ@3.1V	
	1.4mΩ@2.5V	



DESCRIPTION

The CJ12209SP-A uses advanced trench technology to provide excellent R_{SS(ON)}, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V V_{GS(MAX)} rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

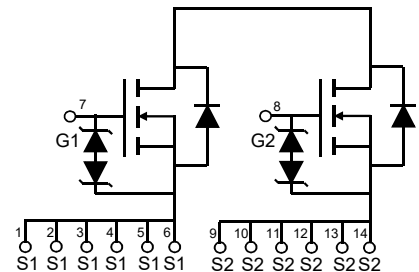
Marking and pin assignment



Marking:

- | | | |
|-------------------------|-----------------------|---------|
| 1. 12209A: Product Code | 1, 2, 3, 4, 5, 6 | Source1 |
| 2. YYMMS: Date Code | 9, 10, 11, 12, 13, 14 | Source2 |
| 3. Solid dot: Pin 1 | 7 Gate1 | |
| | 8 Gate2 | |

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V _{SSS}	12	V
Gate-Source Voltage	V _{GSS}	±8	V
Source Current(DC)	I _S ^①	20	A
Source Current (Pulsed)	I _{SP} ^①	200	A
Total Power Dissipation	P _T ^①	1.3	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature Range	T _{STG}	-55 To 150	°C

MOSFET ELECTRICAL CHARACTERISTICS

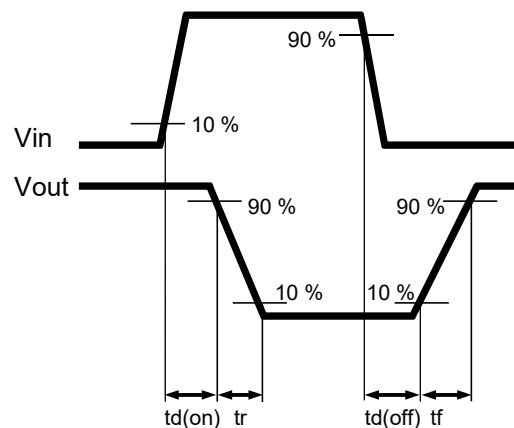
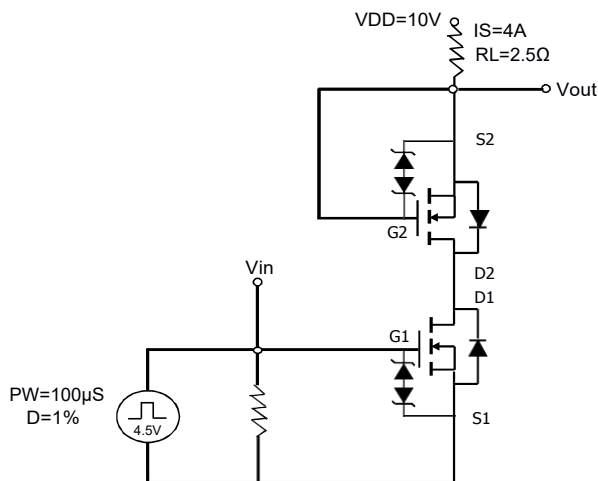
$T_a=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	$I_S=1\text{mA}, V_{GS}=0\text{V}$	12			V
Zero-Gate Voltage Source Current	I_{SSS}	$V_{SS}=10\text{V}, V_{GS}=0\text{V}$			1.0	μA
Gate to Source Leakage Current	I_{GSS}	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$			± 10	μA
Gate to Source Threshold Voltage	V_{TH}	$V_{S2S1}=6\text{V}, I_{S1}=2.3\text{mA}$	0.35	0.7	1.4	V
		$V_{S1S2}=6\text{V}, I_{S2}=2.3\text{mA}$				
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=4.5\text{V}, I_S=10\text{A}$	0.8	1.0	1.5	$\text{m}\Omega$
		$V_{GS}=3.8\text{V}, I_S=10\text{A}$	0.9	1.1	1.65	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=10\text{A}$	1.0	1.2	1.8	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=10\text{A}$	1.1	1.4	3.2	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{SS}=10\text{V}, V_{GS}=0\text{V}, f=1\text{kHz}$		5862		pF
Output Capacitance	C_{oss}			1315		pF
Reverse Transfer Capacitance	C_{rss}			1028		pF
Turn-on Delay Time	$t_{d(on)}$		$V_{DD}=10\text{V}, I_S=4\text{A}, V_{GS}=4.5\text{V}$		1.2	
Turn-on Rise Time	t_r			5.7		μs
Turn-off Delay Time	$t_{d(off)}$			11		μs
Turn-off Fall Time	t_f			15.4		μs
Total Gate Charge	Q_g				72	
Gate1-source1 charge	Q_{g1s1}	$V_{SS}=10\text{V}, I_S=10\text{A}, V_{GS}=4.5\text{V}$		7.2		nC
Gate1-source2 charge	Q_{g1s2}			32.7		nC
Diode Forward Voltage	$V_{F(S-S)}$	$V_{G1S1}=0\text{V}, V_{G2S2}=4.5\text{V}, I_S=2\text{A}$			1.0	V
		$V_{G1S1}=4.5\text{V}, V_{G2S2}=0\text{V}, I_S=2\text{A}$				

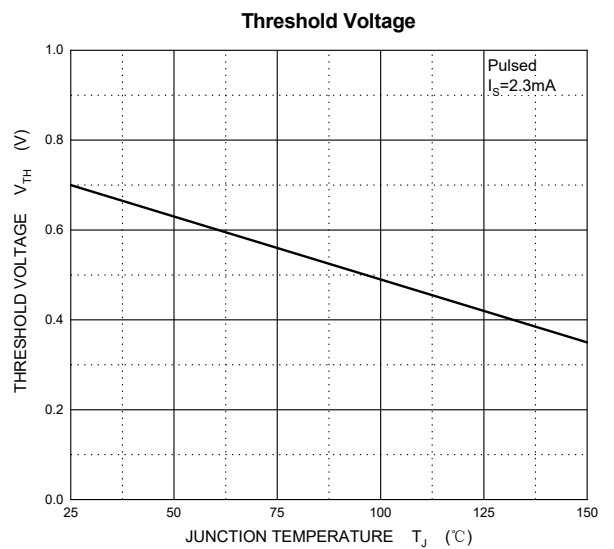
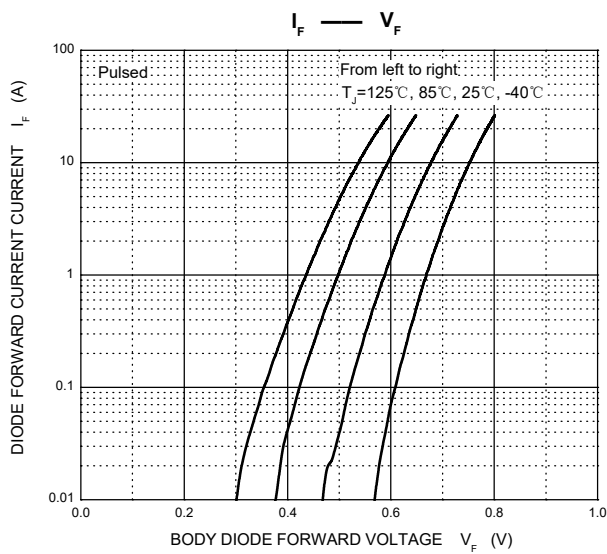
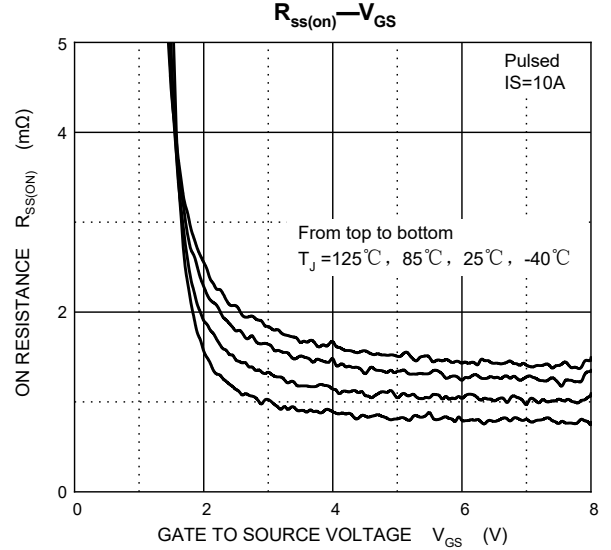
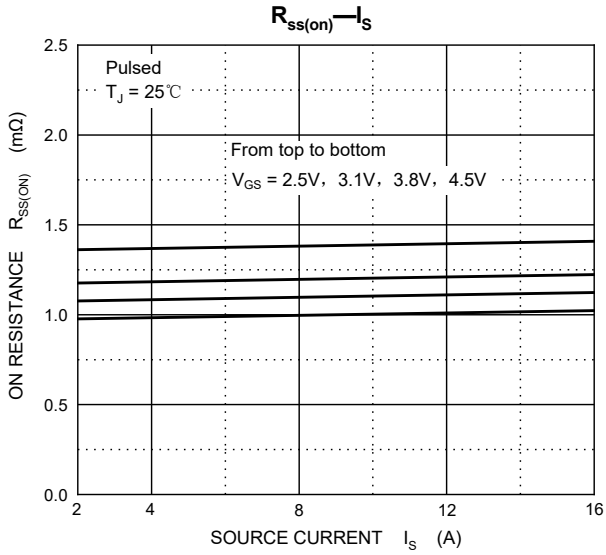
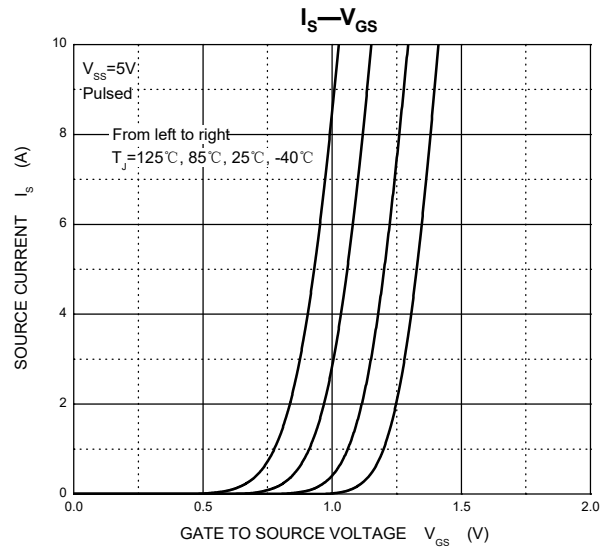
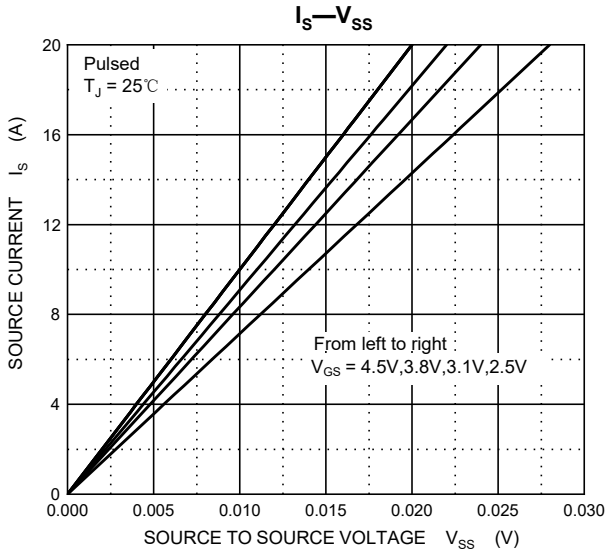
Notes: 1. Mounted on FR4 board (25.4mm×25.4mm×1.0mm) using the minimum recommended pad size (36um Copper).

2. $t = 10\text{ ms}$, Duty Cycle = 1%.

3. When FET1 is measured, G2 and S2 are short-circuited.

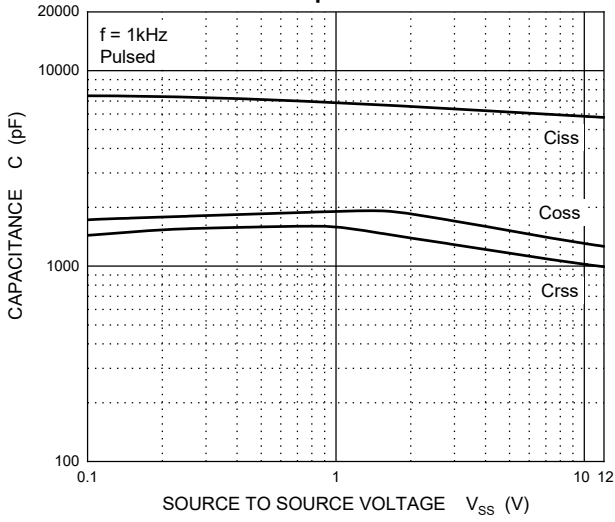


Typical Characteristics

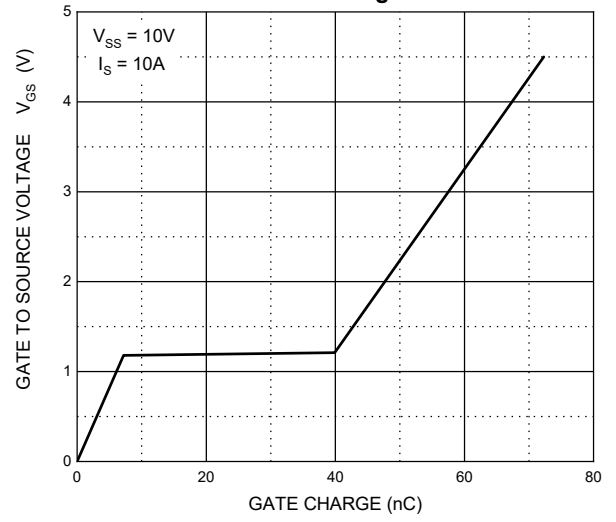


Typical Characteristics

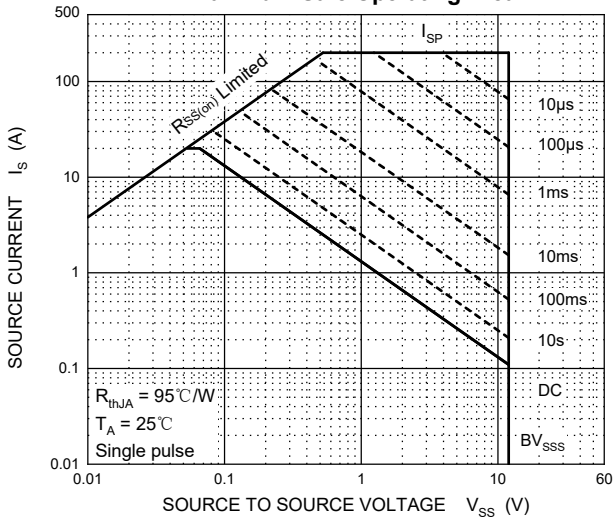
Capacitances



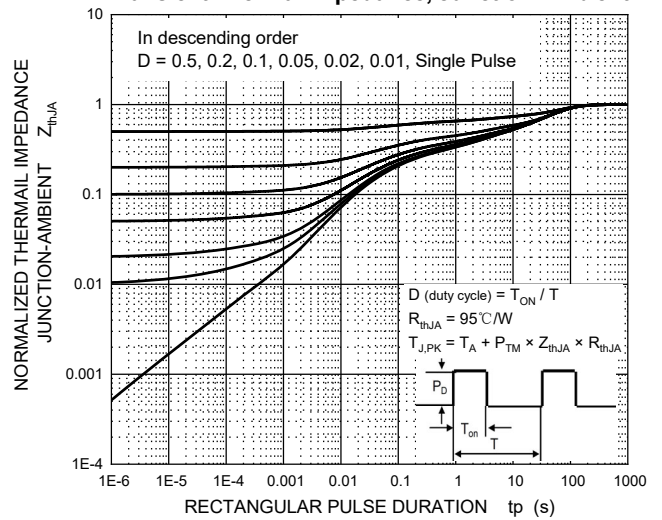
Gate Charge



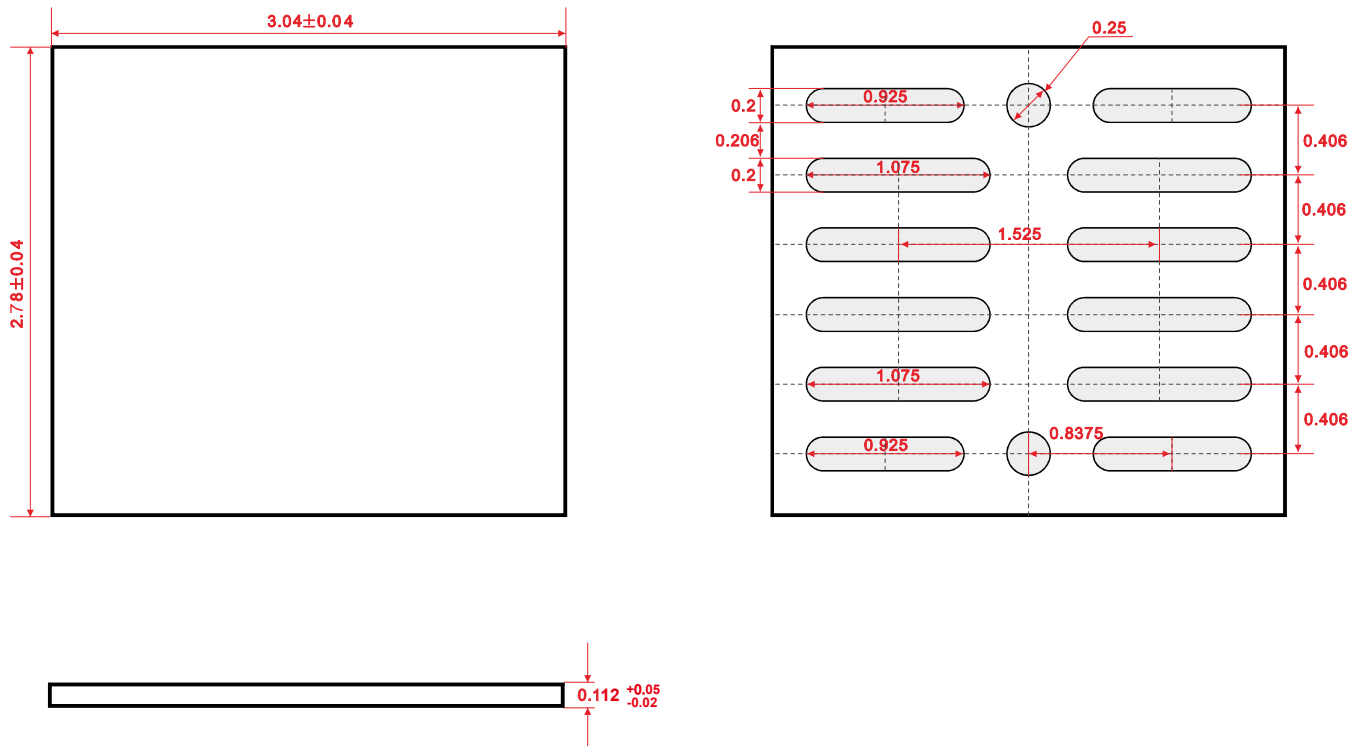
Maximum Safe Operating Area



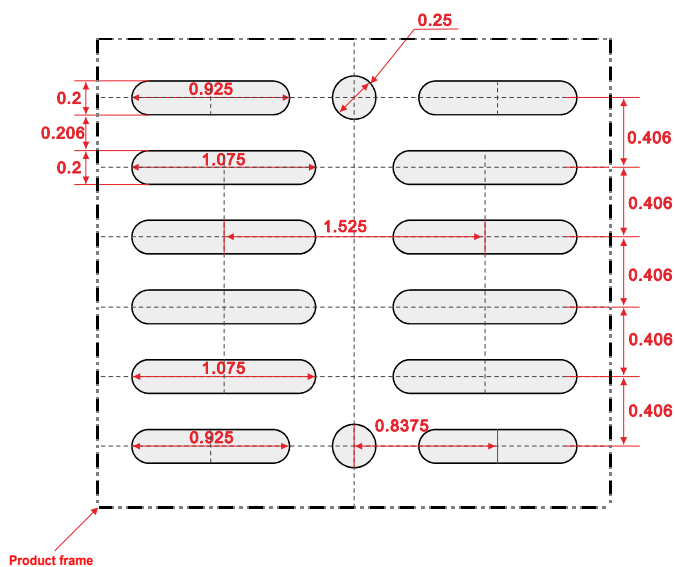
Transient Thermal Impedance, Junction-Ambient



CSPC3028-14 Package Outline Dimensions(Unit:mm)



CSPC3028-14 Suggested Pad Layout (Unit:mm)

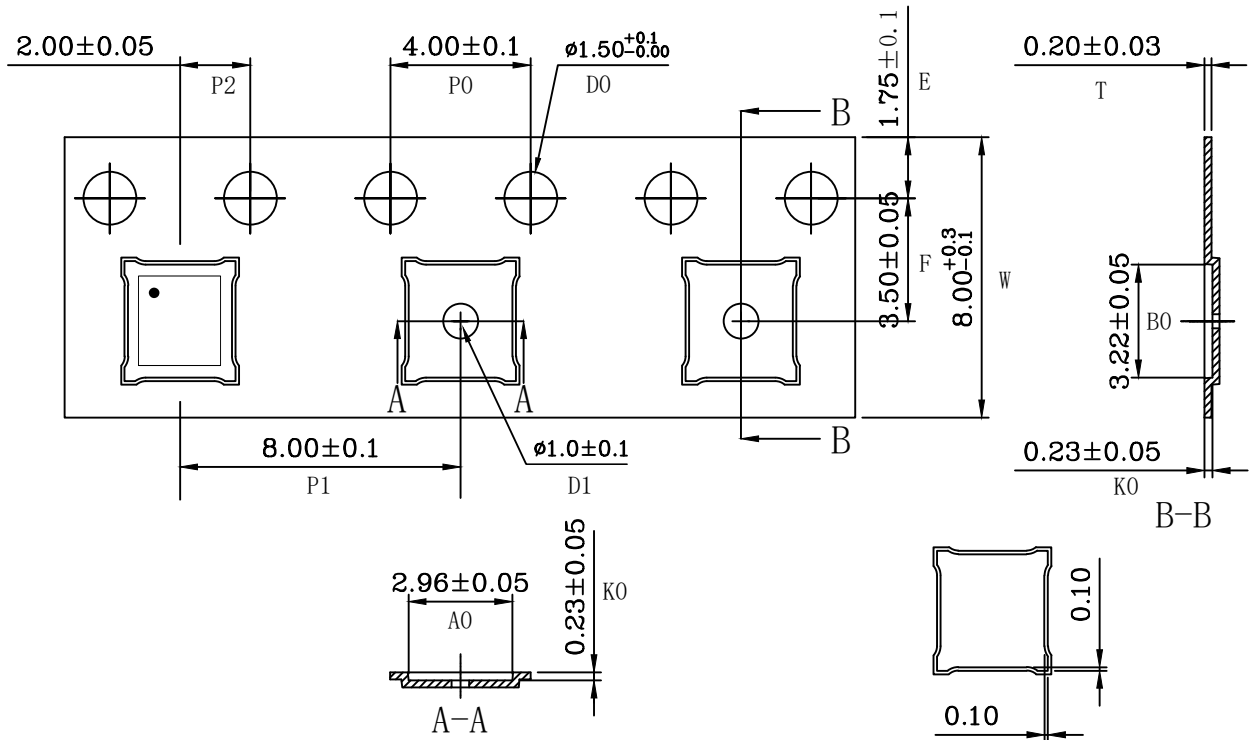


- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.050 mm.
 3. The pad layout is for reference purposes only.

NOTICE

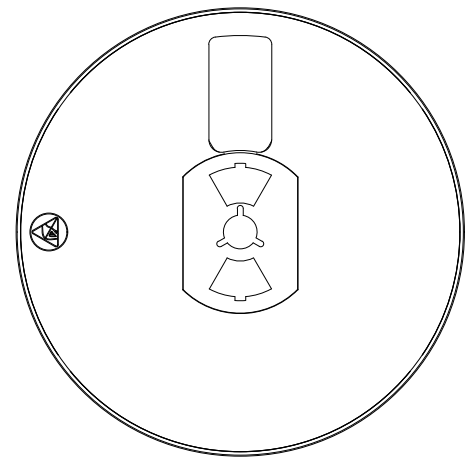
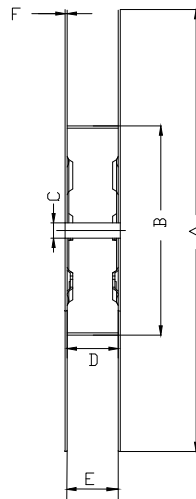
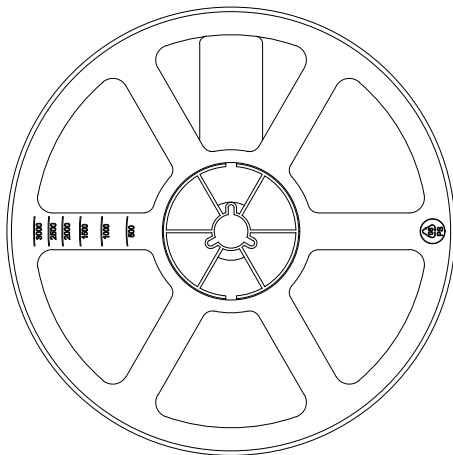
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Tape and Reel



产品尺寸规格(UNT:mm)

规格	W	P1	E	F	D0	D1
尺寸	8.00 ^{+0.3} _{-0.1}	8.00±0.10	1.75±0.10	3.50±0.05	1.50 ^{+0.1} ₋₀	1.00±0.10
规格	A0	B0	K0	T	P0	P2
尺寸	2.96±0.05	3.22±0.05	0.23±0.05	0.20±0.03	4.00±0.10	2.00±0.05



SIZE	8MM
A	178±2.0
B	55±1.0
C	13.0 ^{+0.35} _{-0.15}
D	8.4 ^{+2.5} _{-0.4}
E	8.65 ^{+4.7} _{-0.65}
F	1.5±0.5

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