JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

Trickle-Charge Timekeeping Chip

CJ1302

1 Introduction

The CJ1302 trickle-charge timekeeping chip contains a real-time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator.

The CJ1302 has the additional features of dual power pins for primary and backup power supplies, programmable trickle charger for VCC1, and seven additional bytes of scratchpad memory.

The CJ1302 is widely used in telephone, fax, portable instruments and battery-powered instruments.

2 Available Package

PART NUMBER	PACKAGE
CJ1302	SOP8

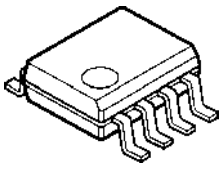


Figure 2-1. SOP8 Package

3 Features

- Real-Time Clock Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
- 31 x 8 Battery-Backed General-Purpose RAM
- Simple Serial Port Interfaces to Most Microcontrollers:
  Simple 3-Wire Interface
- TTL-Compatible (V_{CC} = 5V)
- Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock or RAM Data
- 2.0V to 5.5V Full Operation
- Uses Less Than 300nA at 2.0V
- Optional Industrial Temperature Range: -20°C to +85°C

4 Applications

- Mobile phone
- Facsimile
- Portable instrument
- Instrument

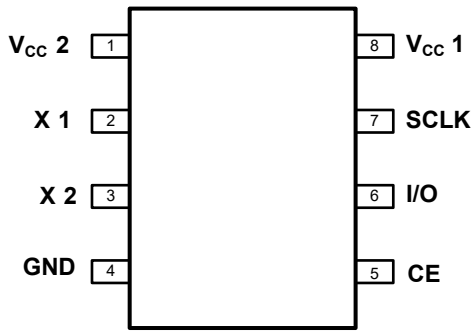


Figure 2-2. Pin Connections

5 Orderable Information and Marking Information

5.1 Orderable Information

MODEL	DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
-	CJ1302	SOP8	-25 ~ 85°C	RoHS & Green	Level 3 168 HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

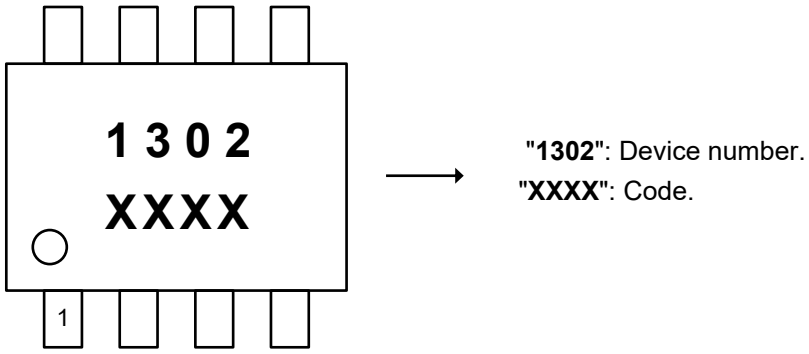
Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

5.2 Marking Information



"**1302**": Device number.

"**XXXX**": Code.

6 Pin Configuration and Function

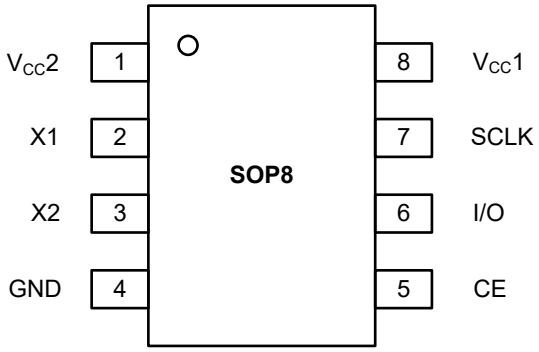


Figure 6-1. CJ1302 Pin Map (Top View)

PIN NAME	CJ1302 SOP8	I/O	DESCRIPTION
V_{CC2}	1	P	Primary Power-Supply Pin in Dual Supply Configuration. V_{CC1} is connected to a backup source to maintain the time and date in the absence of primary power. The CJ1302 operates from the larger of V_{CC1} or V_{CC2}. When V_{CC2} is greater than V_{CC1} + 0.2V, V_{CC2} powers the CJ1302. When V_{CC2} is less than V_{CC1}, V_{CC1} powers the CJ1302.
X1	2	I	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. The CJ1302 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
X2	3	O	
GND	4	G	Ground.
CE	5	I	Input. CE signal must be asserted high during a read or a write. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
I/O	6	I/O	Input/Push-Pull Output. The I/O pin is the bidirectional data pin for the 3-wire interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
SCLK	7	I	Input. SCLK is used to synchronize data movement on the serial interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
V_{CC1}	8	P	Low-Power Operation in Single Supply and Battery-Operated Systems and Low-Power Battery Backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin. UL recognized to ensure against reverse charging current when used with a lithium battery.

7 Specifications

7.1 Absolute Maximum Ratings

(over operating ambient temperature range, unless otherwise specified)(1)

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Voltage Range on Any Pin Relative to Ground	V_P	-0.5 ~ 7.0	V
Operating Temperature Range	T_A	-20 ~ 85	°C
Storage temperature	T_{stg}	-50 ~ 140	°C
Soldering temperature & time	T_{solder}	260°C, 10s	-

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(TA = -20°C to +85°C.)(1)

PARAMETER(4)	SYMBOL		CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC1}, V_{CC2}	V_{CC1},V_{CC2}		(Notes 2, 10)	2	3.3	5.5	V
Logic 1 Input	V_{IH}		(Note 2)	2	-	V_{CC}+0.3	V
Logic 0 Input	V_{IL}	V_{CC}=2V	(Note 2)	-0.3	-	0.3	V
		V_{CC}=5V		-0.3	-	0.8	

7 Specifications

7.3 DC Electrical Characteristics

CJ1302(TA = -20°C to +85°C, unless otherwise specified)(1)

CHARACTERISTIC	SYMBOL		CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Leakage	I_{LI}		(Notes 5, 13)	-	85	500	μA
I/O Leakage	I_{LO}		(Notes 5, 13)	-	85	500	μA
Logic 1 Output (IOH = -0.4mA)	V_{OH}	V_{CC}=2.0V	(Note 2)	1.6	-	-	V
Logic 1 Output (IOH = -1.0mA)		V_{CC}=5.0V	(Note 2)	2.4	-	-	V
Logic 0 Output (IOL = 1.5mA)	V_{OL}	V_{CC}=2.0V	(Note 2)	-	-	0.4	V
Logic 0 Output (IOL = 4.0mA)		V_{CC}=5.0V	(Note 2)	-	-	0.4	V
Active Supply Current (Oscillator Enabled)	I_{CC1A}	V_{CC1} = 2.0V	CH = 0 (Notes 4, 11)	-	-	0.4	mA
		V_{CC1} = 5.0V		-	-	1.2	
Timekeeping Current (Oscillator Enabled)	I_{CC1T}	V_{CC1} = 2.0V	CH = 0 (Notes 3, 11,13)	-	0.2	0.3	μA
		V_{CC1} = 5.0V		-	0.45	1	
Standby Current (Oscillator Disabled	I_{CC1S}	V_{CC1} = 2.0V	CH = 1 (Notes 9, 11, 13)	-	1	100	nA
		V_{CC1} = 5.0V		-	1	100	
		IND		-	5	200	
Active Supply Current (Oscillator Enabled)	I_{CC2A}	V_{CC2} = 2.0V	CH = 0 (Notes 4, 12)	-	-	0.425	mA
		V_{CC2} = 5.0V		-	-	1.28	
Timekeeping Current (Oscillator Enabled)	I_{CC2T}	V_{CC2} = 2.0V	CH = 0 (Notes 3, 12)	-	-	25.3	μA
		V_{CC2} = 5.0V		-	-	81	
Standby Current (Oscillator Disabled)	I_{CC2S}	V_{CC2} = 2.0V	CH = 1 (Notes 9, 12	-	-	25	μA
		V_{CC2} = 5.0V		-	-	80	
Trickle-Charge Resistors	R1			-	2	-	kΩ
	R2			-	4	-	
	R3			-	8	-	
Trickle-Charge Diode Voltage Drop	V_{TD}			-	0.7	-	V

7.4 Capacitance

CJ1302(TA = 25°C, unless otherwise specified)(1)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_I	-	-	10	-	pF
I/O Capacitance	$C_{I/O}$	-	-	15	-	pF

7 Specifications

7.5 AC Electrical Characteristics

CJ1302(TA = -20°C to +85°C, unless otherwise specified)(1)

CHARACTERISTIC	SYMBOL		CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data to CLK Setup	t_{DC}	V_{CC} = 2.0V	(Notes 6)	200	-	-	ns
		V_{CC} = 5.0V		50	-	-	
CLK to Data Hold	t_{CDH}	V_{CC} = 2.0V	(Notes 6)	280	-	-	ns
		V_{CC} = 5.0V		70	-	-	
CLK to Data Delay	t_{CDD}	V_{CC} = 2.0V	(Notes 6, 7, 8)	-	-	800	ns
		V_{CC} = 5.0V		-	-	200	
CLK Low Time	t_{CL}	V_{CC} = 2.0V	(Notes 6)	1000	-	-	ns
		V_{CC} = 5.0V		250	-	-	
CLK High Time	t_{CH}	V_{CC} = 2.0V	(Notes 6)	1000	-	-	ns
		V_{CC} = 5.0V		250	-	-	
CLK Frequency	F_{CLK}	V_{CC} = 2.0V	(Notes 6)	-	-	0.5	MHz
		V_{CC} = 5.0V		DC	-	2.0	
CLK Rise and Fall	t_R, t_F	V_{CC} = 2.0V		-	-	2000	ns
		V_{CC} = 5.0V		-	-	500	
CE to CLK Setup	t_{CC}	V_{CC} = 2.0V	(Notes 6)	4	-	-	μs
		V_{CC} = 5.0V		1	-	-	
CLK to CE Hold	t_{CCH}	V_{CC} = 2.0V	(Notes 6)	240	-	-	ns
		V_{CC} = 5.0V		60	-	-	
CE Inactive Time	t_{CWH}	V_{CC} = 2.0V	(Notes 6)	4	-	-	μs
		V_{CC} = 5.0V		1	-	-	
CE to I/O High Impedance	t_{CDZ}	V_{CC} = 2.0V	(Notes 6)	-	-	280	ns
		V_{CC} = 5.0V		-	-	70	
SCLK to I/O High Impedance	t_{CCZ}	V_{CC} = 2.0V	(Notes 6)	-	-	280	ns
		V_{CC} = 5.0V		-	-	70	

Note 1: Limits at -20°C are guaranteed by design and are not production tested.

Note 2: All voltages are referenced to ground.

Note 3: I_{CC1T} and I_{CC2T} are specified with I/O open, CE and SCLK set to a logic 0.

Note 4: I_{CC1A} and I_{CC2A} are specified with the I/O pin open, CE high, SCLK = 2MHz at V_{CC} = 5V; SCLK = 500kHz, V_{CC} = 2.0V.

Note 5: CE, SCLK, and I/O all have 40kΩ pulldown resistors to ground.

Note 6: Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.

Note 7: Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.

Note 8: Load capacitance = 50pF.

Note 9: I_{CC1S} and I_{CC2S} are specified with CE, I/O, and SCLK open.

Note 10: V_{CC} = V_{CC2}, when V_{CC2} > V_{CC1} + 0.2V; V_{CC} = V_{CC1}, when V_{CC1} > V_{CC2}.

Note 11: V_{CC2} = 0V.

Note 12: V_{CC1} = 0V.

Note 13: Typical values are at +25°C.

7 Specifications

7.6 Timing Diagrams

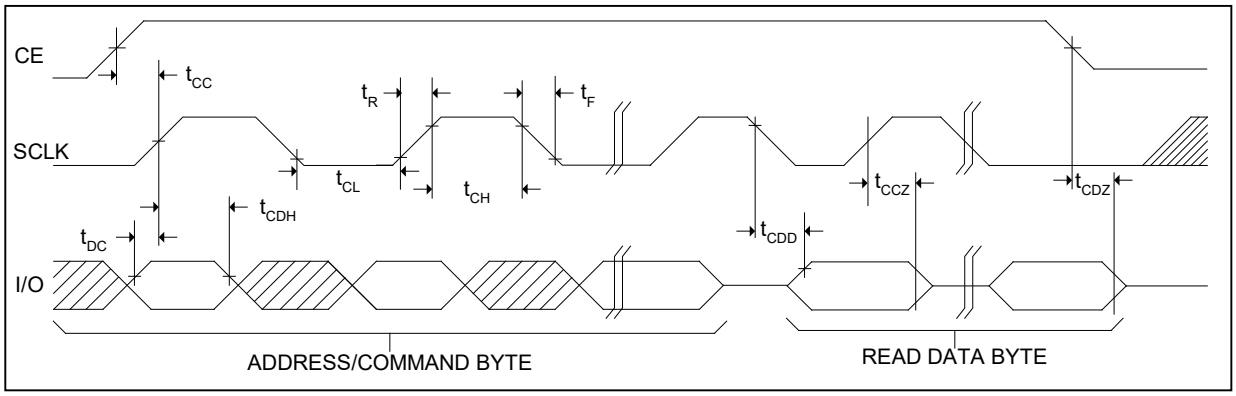


Figure 7-1. Read Data Transfer

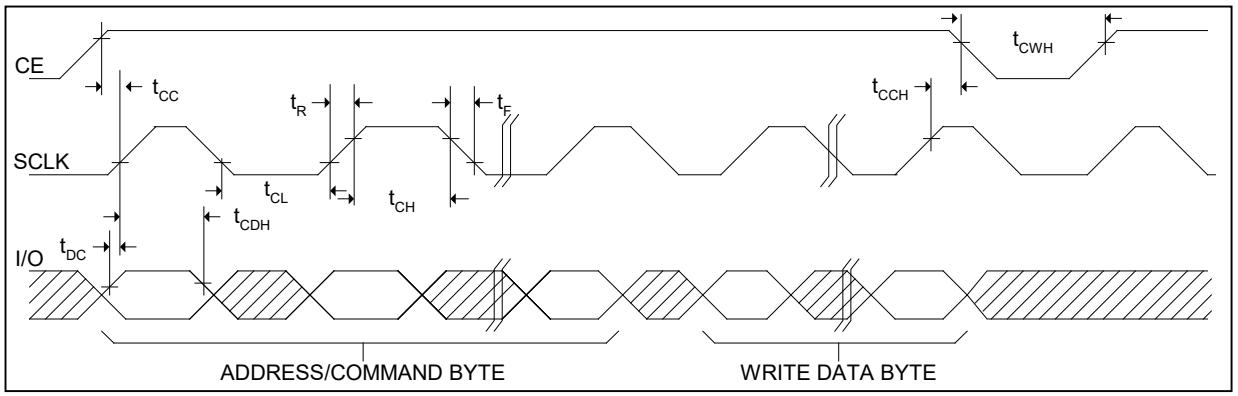


Figure 7-2. Write Data Transfer

7.7 Typical Application Circuit

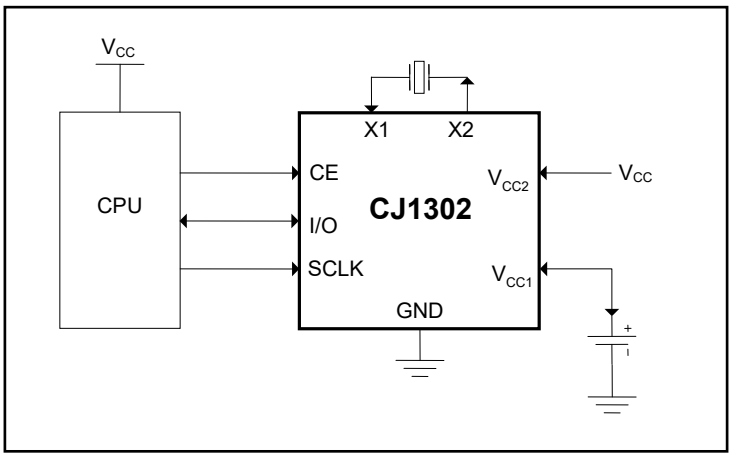


Figure 7-3. Typical Application Circuit

8 Detailed Description

8.1 Description

The CJ1302 trickle-charge timekeeping chip contains a real-time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator.

8.2 Function Block Diagram

Figure 8-1 shows the main elements of the serial timekeeper: shift register, control logic, oscillator, real-time clock, and RAM.

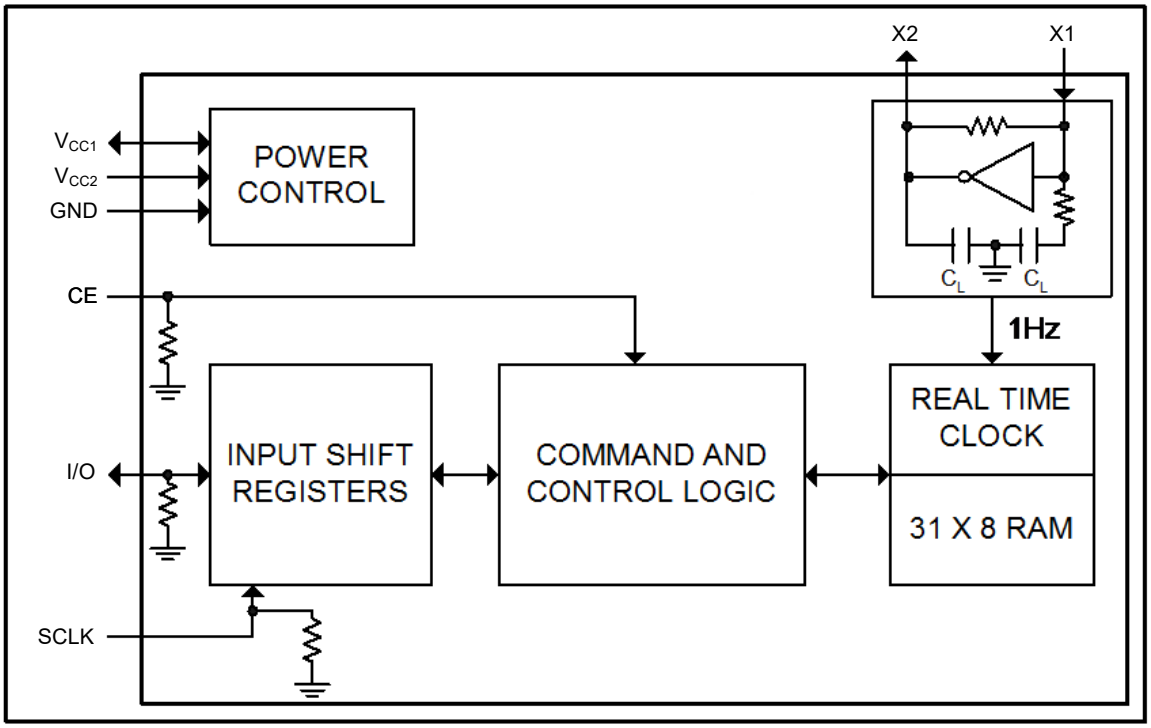


Figure 8-1. Read Data Transfer

8.3 Feature Description

Oscillator Circuit

The CJ1302 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 8-1 specifies several crystal parameters for the external crystal. Figure 8-1 shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.

Table 8-1. Input and Output Logic

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	45	kΩ
Load Capacitance	C_L	-	6	-	pF

8 Detailed Description

8.3 Feature Description (continued)

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. Figure 8-2 shows a typical PC board layout for isolating the crystal and oscillator from noise.

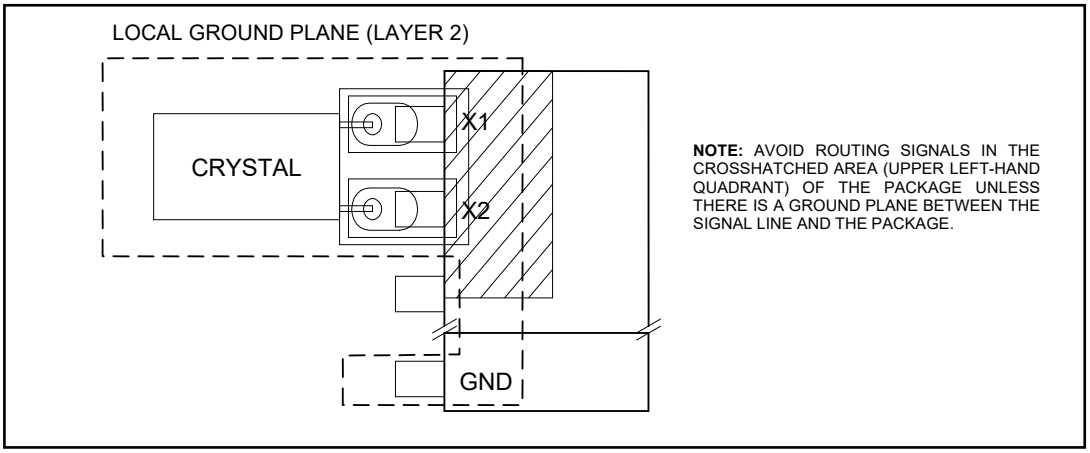


Figure 8-2. Typical PC Board Layout for Crystal

Command Byte

Table 8-2 shows the command byte. A command byte initiates each data transfer. The MSB (bit 7) must be a logic 1. If it is 0, writes to the CJ1302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 to 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

Table 8-2. Address/Command Byte

7	6	5	4	3	2	1	0
1	RAM $\overline{CK}$	A4	A3	A2	A1	A0	RD $\overline{WR}$

CE and Clock Control

Driving the CE input high initiates all data transfers. The CE input serves two functions. First, CE turns on the control logic that allows access to the shift register for the address/command sequence. Second, the CE signal provides a method of terminating either single-byte or multiple-byte CE data transfer.

A clock cycle is a sequence of a rising edge followed by a falling edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the CE input is low, all data transfer terminates and the I/O pin goes to a high-impedance state. Figure 8-3 shows data transfer. At power-up, CE must be a logic 0 until V_{CC} > 2.0V. Also, SCLK must be at a logic 0 when CE is driven to a logic 1 state.

Date Input

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

8 Detailed Description

8.3 Feature Description (continued)

Date Output

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as CE remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri-stated upon each rising edge of SCLK. Data is output starting with bit 0.

Burst Mode

Burst mode can be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits 1 through 5 = logic 1). As before, bit 6 specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit 0 of address 0.

When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. However, when writing to RAM in burst mode it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 31 bytes are written or not.

Clock/Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Table 8-4 illustrates the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.
The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers the rising edge of CE.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the falling edge of CE. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second.

The CJ1302 can be run in either 12-hour or 24-hour mode. Bit 7 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). The hours data must be re-initialized whenever the 12/24 bit is changed.

Clock Halt Flag

Bit 7 of the seconds register is defined as the clock halt (CH) flag. When this bit is set to logic 1, the clock oscillator is stopped and the CJ1302 is placed into a low-power standby mode with a current drain of less than 100nA. When this bit is written to logic 0, the clock will start. The initial power-on state is not defined.

Write-protect Bit

Bit 7 of the control register is the write-protect bit. The first seven bits (bits 0 to 6) are forced to 0 and always read 0 when read. Before any write operation to the clock or RAM, bit 7 must be 0. When high, the write-protect bit prevents a write operation to any other register. The initial power-on state is not defined. Therefore, the WP bit should be cleared before attempting to write to the device.

8 Detailed Description

8.3 Feature Description (continued)

Trickle-charge Register

This register controls the trickle-charge characteristics of the CJ1302. The simplified schematic of Figure 8-4 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern of 1010 enables the trickle charger. All other patterns will disable the trickle charger. The CJ1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2 and 3) select whether one diode or two diodes are connected between V_{CC2} and V_{CC1}. If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independently of TCS. The RS bits (bits 0 and 1) select the resistor that is connected between V_{CC2} and V_{CC1}. The resistor and diodes are selected by the RS and DS bits as shown in Table 8-3.

Table 8-3. Trickle Charger Resistor and Diode Select

TCS BIT 7	TCS BIT 6	TCS BIT 5	TCS BIT 4	DS BIT 3	DS BIT 2	RS BIT 1	RS BIT 0	FUNCTION
X	X	X	X	X	X	0	0	Disabled
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
1	0	1	0	0	1	0	1	1 Diode, 2kΩ
1	0	1	0	0	1	1	0	1 Diode, 4kΩ
1	0	1	0	0	1	1	1	1 Diode, 8kΩ
1	0	1	0	1	0	0	1	1 Diode, 2kΩ
1	0	1	0	1	0	1	0	1 Diode, 4kΩ
1	0	1	0	1	0	1	1	1 Diode, 8kΩ
0	1	0	1	1	1	0	0	Initial power-on state

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to V_{CC2} and a super cap is connected to V_{CC1}. Also assume that the trickle charger has been enabled with one diode and resistor R_1 between V_{CC2} and V_{CC1}. The maximum current IMAX would therefore be calculated as follows:

$$I_{MAX} = (5.0V – \text{diode drop}) / R_1 \approx (5.0V – 0.7V) / 2k\Omega \approx 2.2mA$$

As the super cap charges, the voltage drop between V_{CC2} and V_{CC1} decreases and therefore the charge current decreases.

Clock/Calendar Burst Mode

The clock/calendar command byte specifies burst mode operation. In this mode, the first eight clock/calendar registers can be consecutively read or written (see Table 8-4) starting with bit 0 of address 0.

If the write-protect bit is set high when a write clock/calendar burst mode is specified, no data transfer will occur to any of the eight clock/calendar registers (this includes the control register). The trickle charger is not accessible in burst mode.

At the beginning of a clock burst read, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

8 Detailed Description

8.3 Feature Description (continued)

RAM

The static RAM is 31 x 8 bytes addressed consecutively in the RAM address space.

RAM Burst Mode

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written (see Table 8-4) starting with bit 0 of address 0.

Register Summary

A register data format summary is shown in Table 8-4.

Crystal Selection

A 32.768kHz crystal can be directly connected to the CJ1302 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 10pF-33pF. For more information on crystal selection and crystal layout consideration.

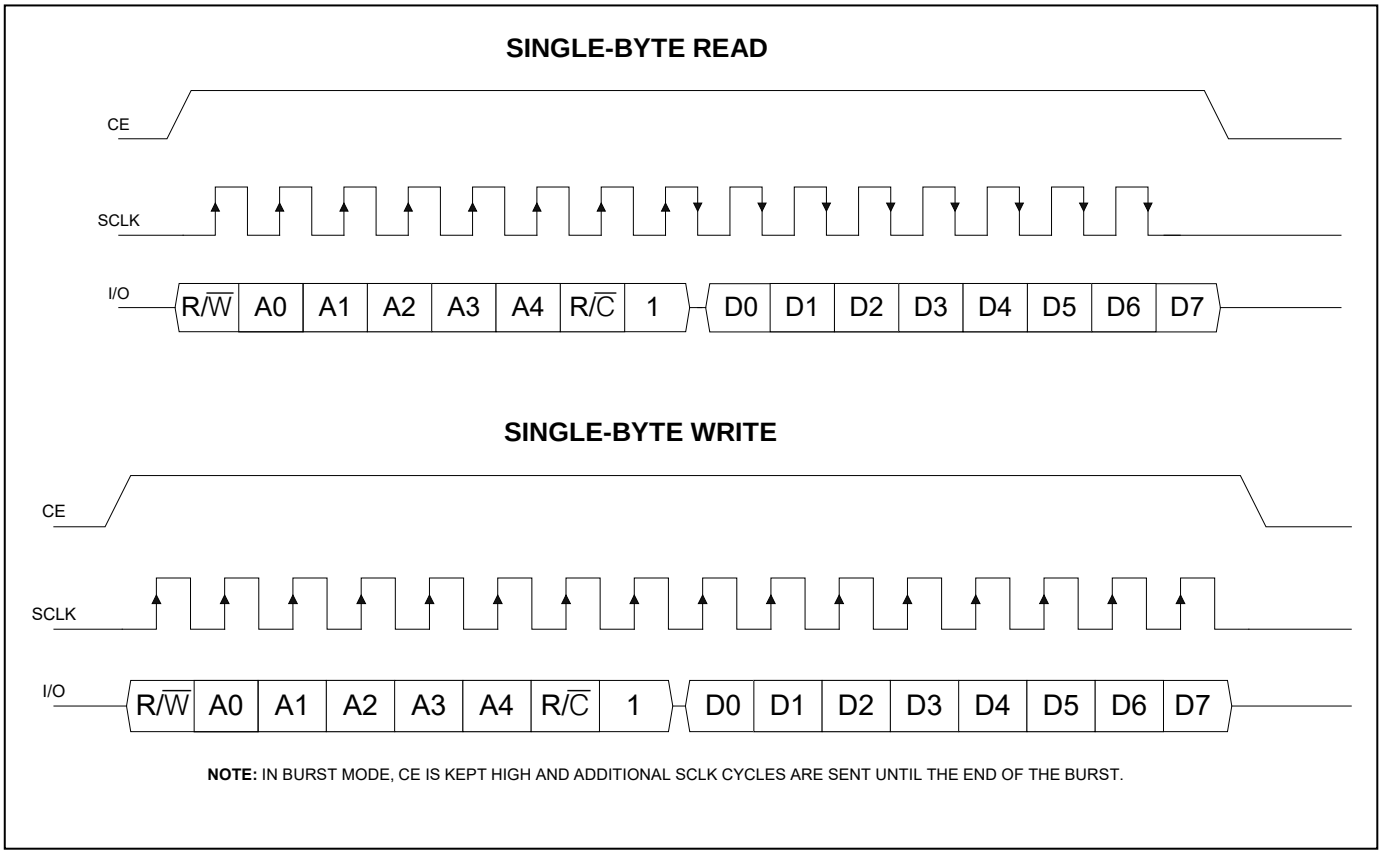


Figure 8-3. Data Transfer Summary

8 Detailed Description

8.3 Feature Description (continued)

Table 8-4. Register Address/Definition

RTC

READ	WRITE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RANGE
81h	80h	CH	10 Seconds			Seconds				00-59
83h	82h		10 Minutes			Minutes				00-59
85h	84h	12/$\overline{24}$	0	10 $\overline{AM}$/PM	Hour	Hour				1-12/0-23
87h	86h	0	0	10 Date		Date				1-31
89h	88h	0	0	0	10 Month	Month				1-12
8Bh	8Ah	0	0	0	0	0	Day			1-7
8Dh	8Ch	10 Year				Year				00-99
8Fh	8Eh	WP	0	0	0	0	0	0	0	—
91h	90h	TCS	TCS	TCS	TCS	DS	DS	RS	RS	—

Clock Burst

BFh	BEh

RAM

C1h	C0h		00-FFh
C3h	C2h		00-FFh
C5h	C4h		00-FFh
- - -	- - -		- - -
FDh	FCh		00-FFh

Clock Burst

FFh	FEh

8 Detailed Description

8.3 Feature Description (continued)

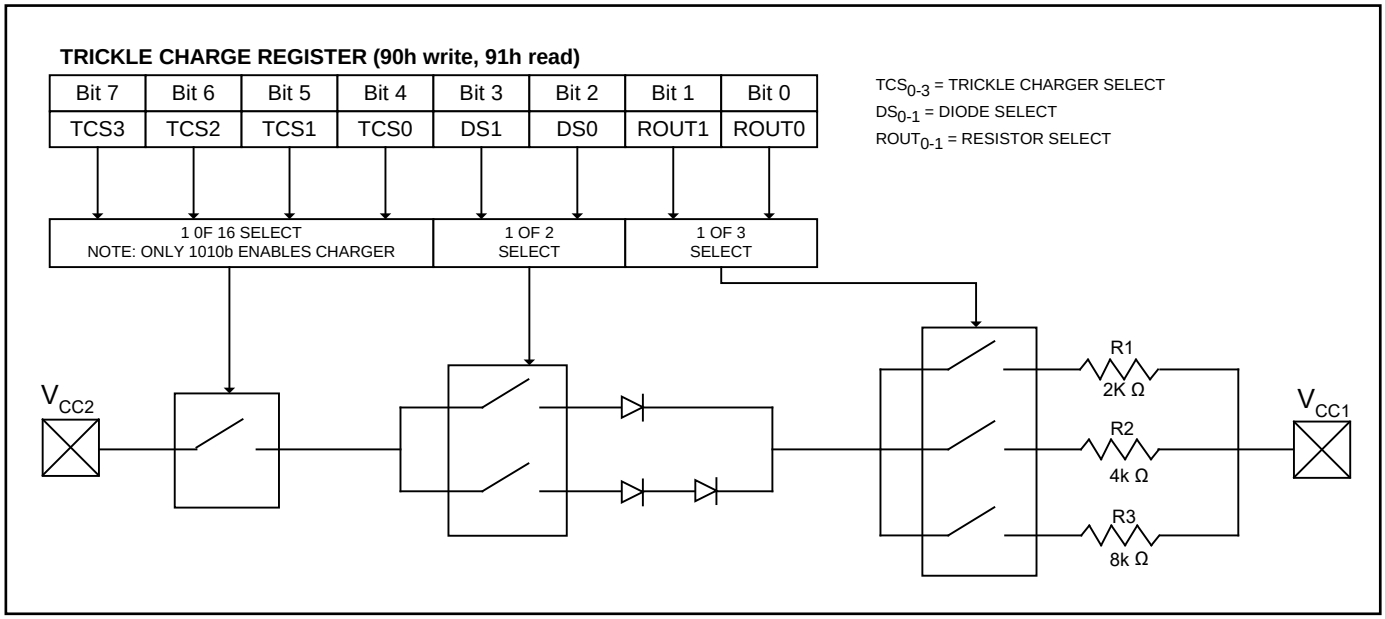


Figure 8-4. Programmable Trickle Charger

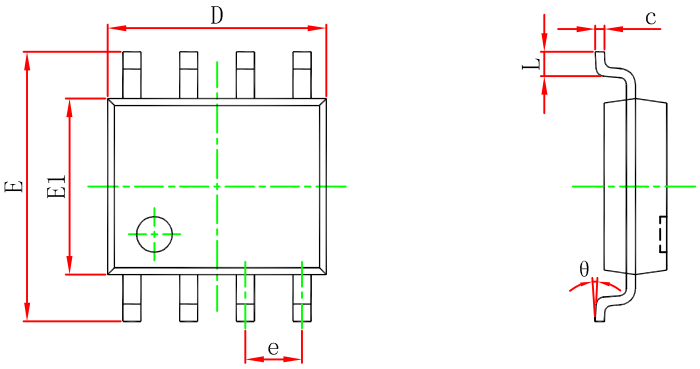
NOTE

The application information in this section is not part of the data sheet component specification, and JSCJ makes no commitment or statement to guarantee its accuracy or completeness. Customers are responsible for determining the rationality of corresponding components in their circuit design and making tests and verifications to ensure the normal realization of their circuit design.

9 Mechanical Information

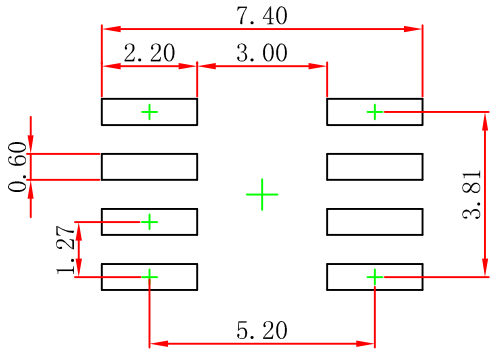
SOP8 Package

Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.450	0.049	0.057
b	0.330	0.510	0.013	0.020
c	0.190	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270（BSC）		0.050（BSC）	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP8 Suggest Pad Layout



NOTE:

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purposes only.

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- https: ***www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

April, 2024: released CJ1302 rev - 1.0.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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