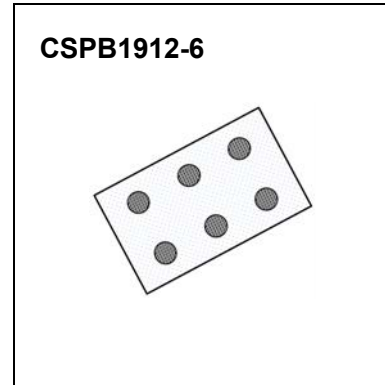




CSP Enhancement Mode Power MOSFET

CJ13024SP Dual N-Channel MOSFET

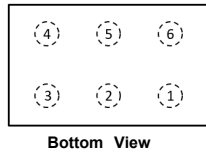
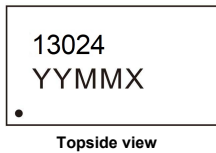
V _{SSS}	R _{SS(on)} TYP	I _S
12V	4.7mΩ@4.5V	9A
	5.0mΩ@3.8V	
	5.5mΩ@3.1V	
	6.5mΩ@2.5V	



DESCRIPTION

The CJ13024SP uses advanced trench technology to provide excellent R_{SS(ON)}, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V V_{GS(MAX)} rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

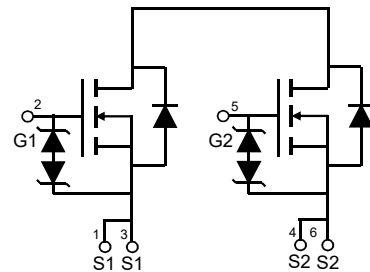
Marking and pin assignment



Marking:

- | | | |
|------------------------|--------------|----------|
| 1. 13024: Product Code | 1,3. Source1 | 2. Gate1 |
| 2. YYMMX: Date Code | 4,6. Source2 | 5. Gate2 |
| 3. Solid dot: Pin 1 | | |

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_J=25°C unless otherwise noted)

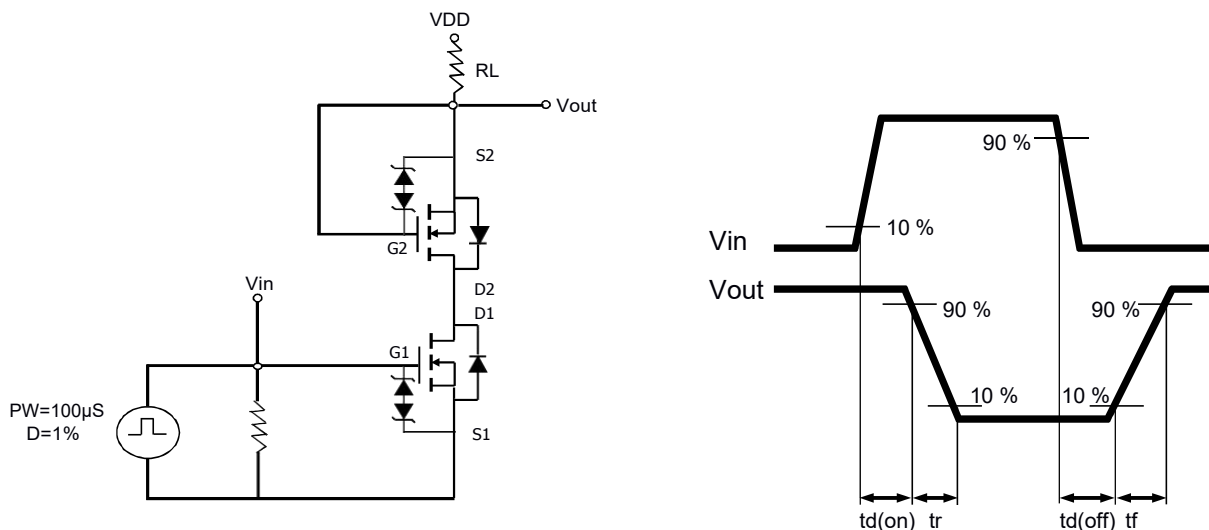
Parameter	Symbol	Limit	Unit
Source to Source Voltage	V _{SSS}	12	V
Gate-Source Voltage	V _{GSS}	±8	V
Source Current(DC)	I _S ^①	9	A
Source Current(DC)	I _S ^②	15	A
Source Current (Pulsed)	I _{SP} ^③	90	A
Total Power Dissipation	P _T ^①	2.1	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature Range	T _{STG}	-55 To 150	°C

MOSFET ELECTRICAL CHARACTERISTICS

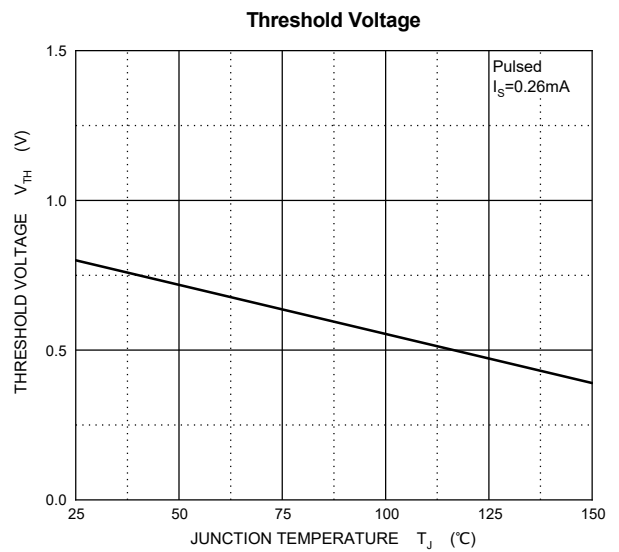
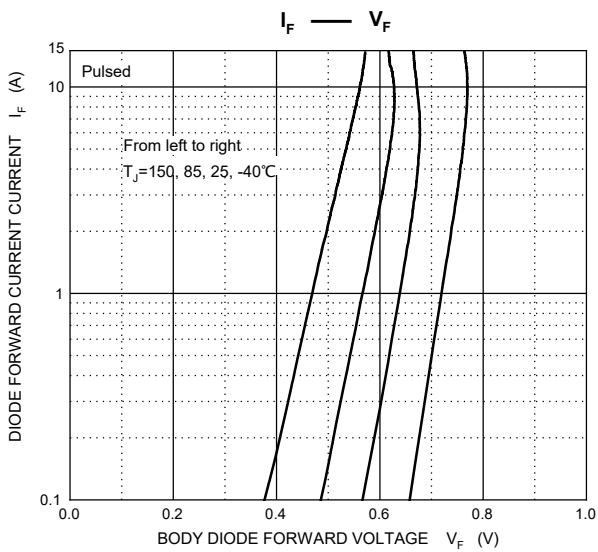
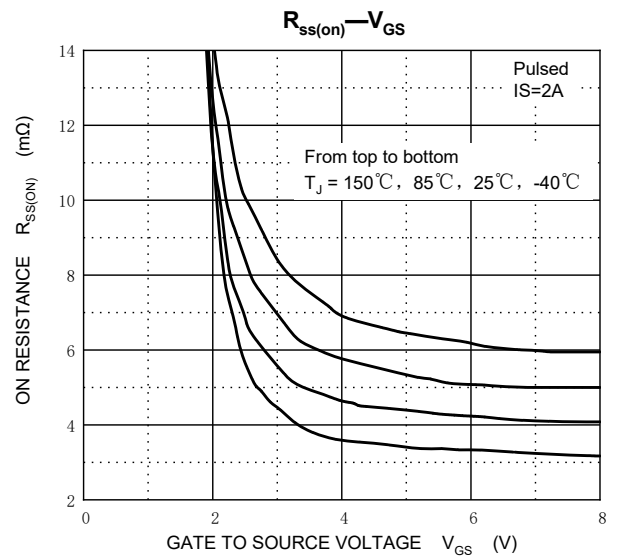
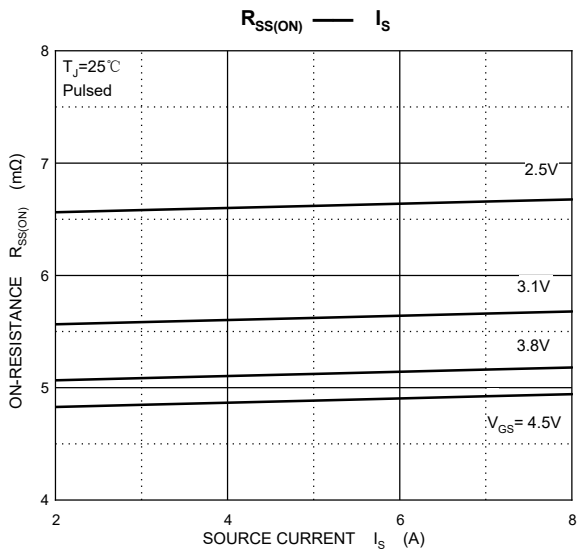
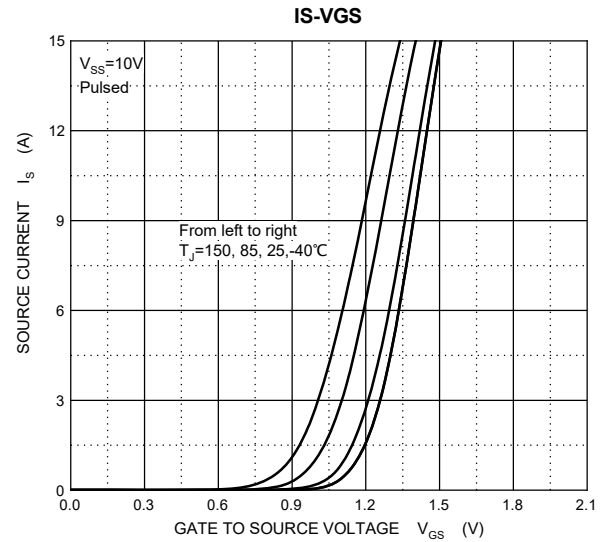
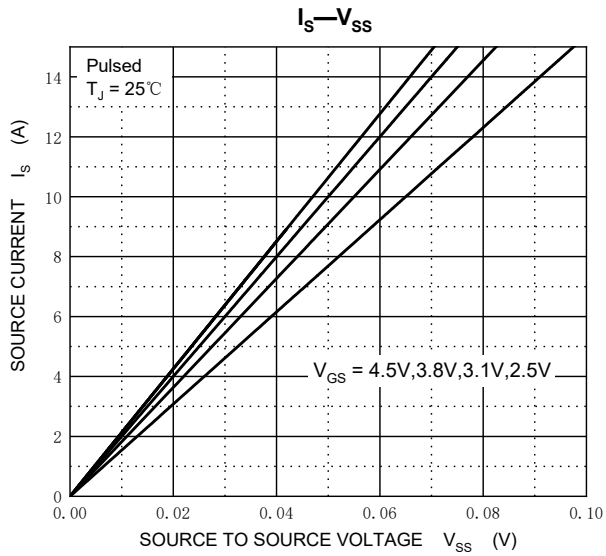
$T_J=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	$I_S=1\text{mA}, V_{GS}=0\text{V}$	12			V
Zero-Gate Voltage Source Current	I_{SSS}	$V_{SS}=10\text{V}, V_{GS}=0\text{V}$			100	nA
Gate to Source Leakage Current	I_{GSS}	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$			± 10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{SS}=V_{GS}, I_S=0.26\text{mA}$	0.4	0.8	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=4.5\text{V}, I_S=2\text{A}$	3.0	4.7	5.4	m Ω
		$V_{GS}=3.8\text{V}, I_S=2\text{A}$	3.3	5.0	6.0	m Ω
		$V_{GS}=3.1\text{V}, I_S=2\text{A}$	3.5	5.5	7.7	m Ω
		$V_{GS}=2.5\text{V}, I_S=2\text{A}$	4.5	6.5	13.6	m Ω
Input Capacitance	C_{iss}			1417		pF
Output Capacitance	C_{oss}	$V_{SS}=6\text{V}, V_{GS}=0\text{V}, f=100\text{kHz}$		463		pF
Reverse Transfer Capacitance	C_{rss}			360		pF
Turn-on Delay Time	$t_{d(on)}$ ④	$V_{DD}=6\text{V}, R_L=1.3\Omega, V_{GS}=4\text{V}$		269		nS
Turn-on Rise Time	t_r ④			329		nS
Turn-off Delay Time	$t_{d(off)}$ ④			1377		nS
Turn-off Fall Time	t_f ④			1253		nS
Total Gate Charge	Q_g ④	$V_{SS}=10\text{V}, I_S=10\text{A}, V_{GS}=6\text{V}$		37.8		nC
Gate1-source1 charge	Q_{g1s1} ④			2.4		nC
Gate1-source2 charge	Q_{g1s2} ④			7.7		nC
Diode Forward Voltage	$V_{F(S-S)}$	$V_{GS}=0\text{V}, I_S=2\text{A}$			1.2	V

- Notes: 1. Mounted on FR4 board (25.4mm×25.4mm×1.0mm) using minimum recommended pad size (partial coverage of single-sided 36 μm Copper).
 2. Mounted on FR4 board(25.4mm×25.4mm×1.0mm) using minimum recommended pad size (full coverage of single-sided 36 μm Copper).
 3. $t = 10\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$.
 4. When FET1 is measured, G2 and S2 are short-circuited.

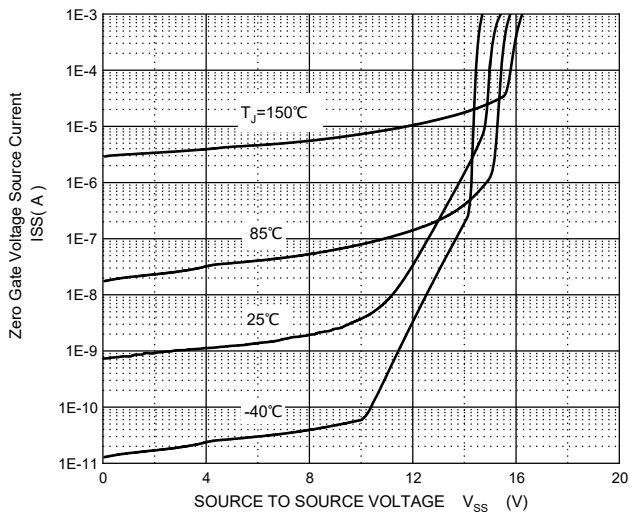


Typical Characteristics

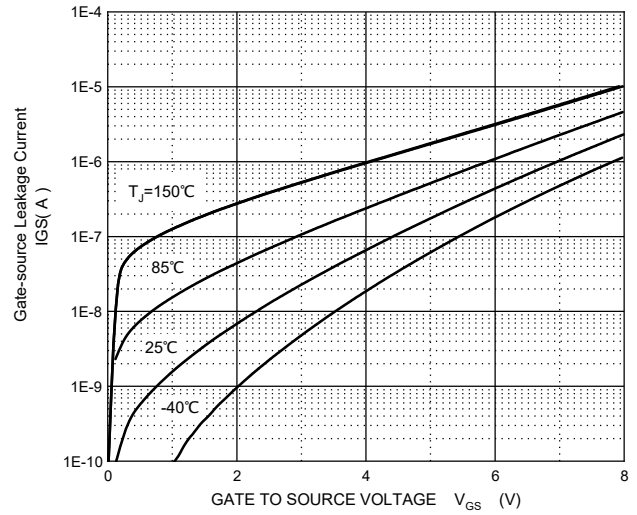


Typical Characteristics

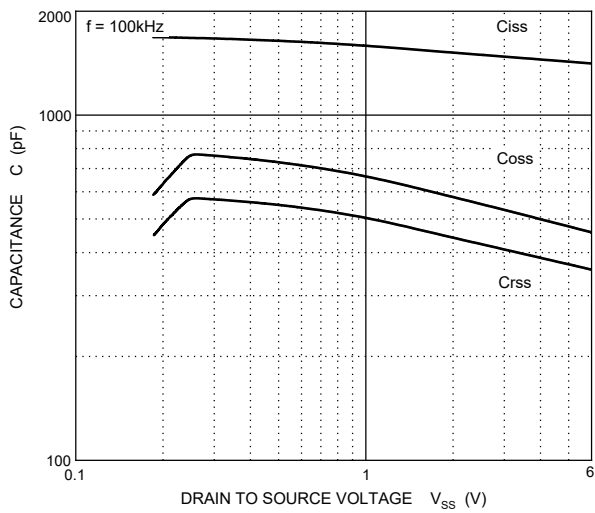
ISS-VSS



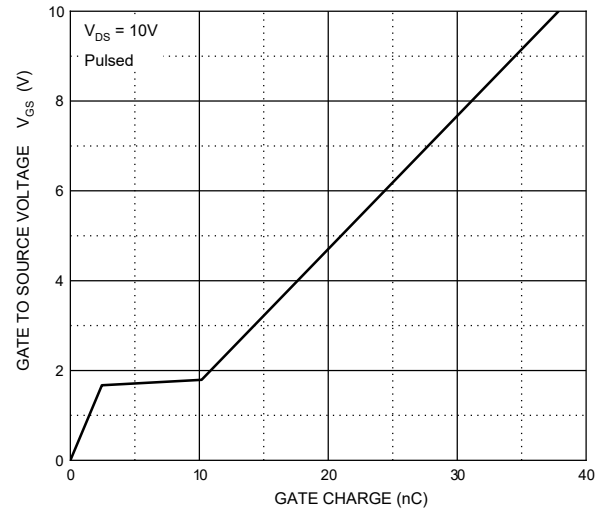
IGS-VGS



Typical Capacitances

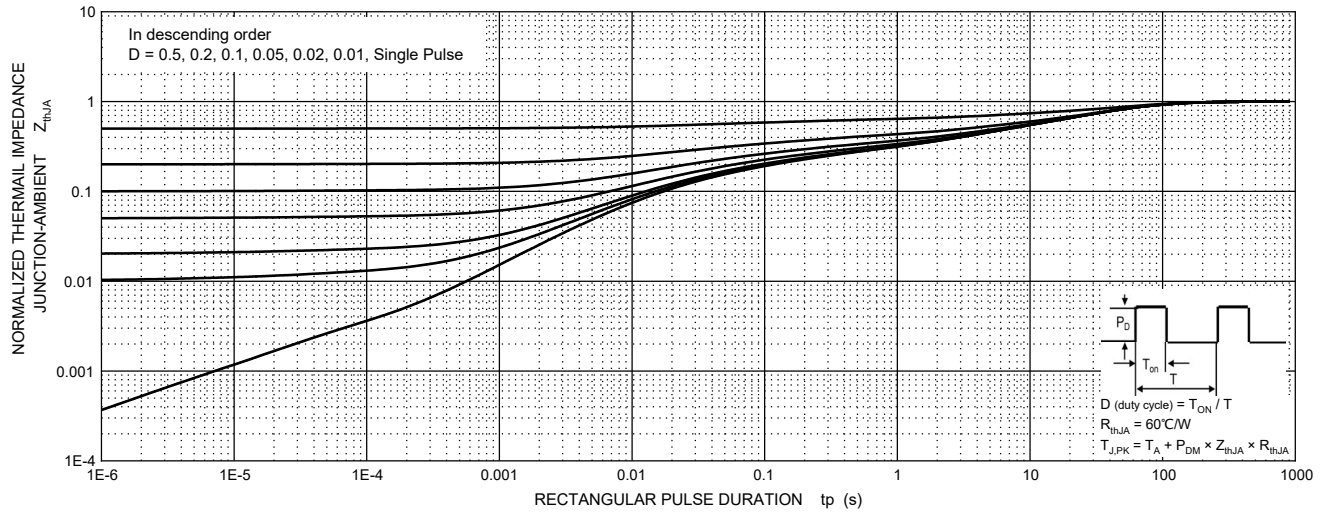


Gate Charge

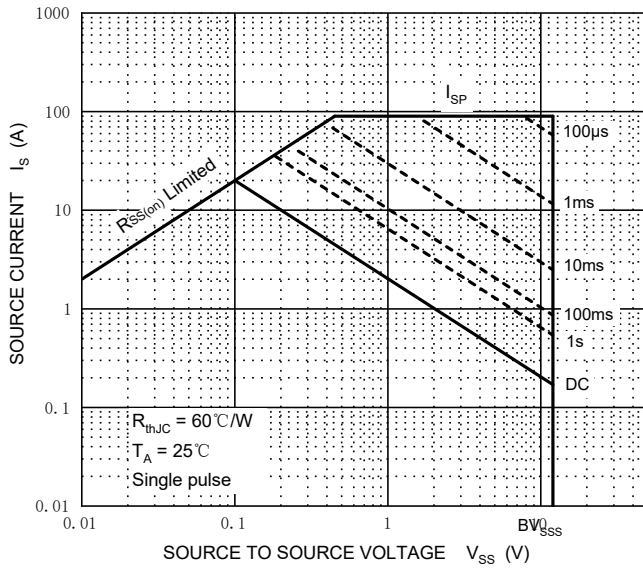


Typical Characteristics

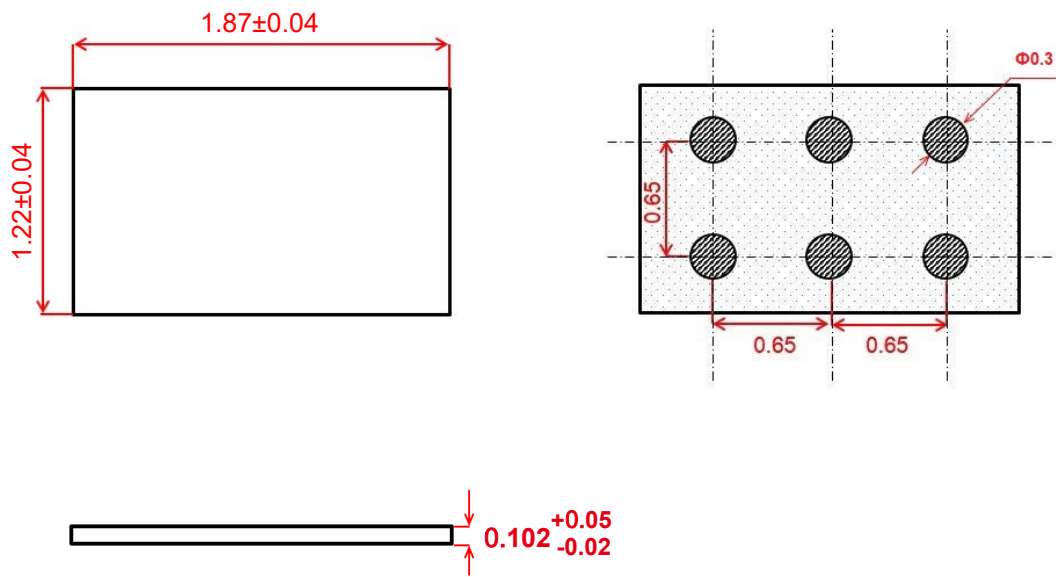
Transient Thermal Impedance, Junction-Ambient



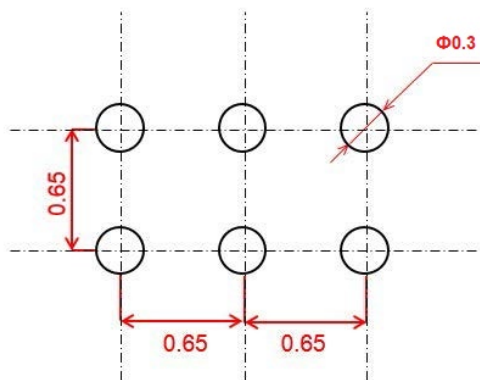
Maximum Safe Operating Area



CSPB1912-6 Package Outline Dimensions(Unit:mm)



CSPB1912-6 Suggested Pad Layout (Unit:mm)



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.050 mm.
3. The pad layout is for reference purposes only.

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