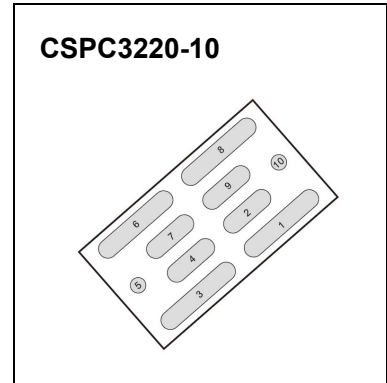




# CSP Enhancement Mode Power MOSFET

## CJ15221SP Dual N-Channel MOSFET

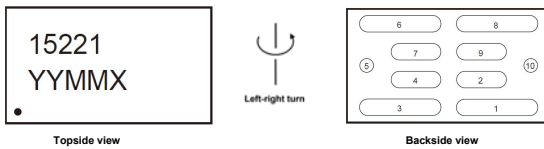
V <sub>SSS</sub>	R <sub>SS(on)</sub> TYP	I <sub>S</sub>
12V	1.1mΩ@4.5V	22.7A
	1.3mΩ@3.8V	
	1.4mΩ@3.1V	
	1.7mΩ@2.5V	



### DESCRIPTION

The CJ15221SP uses advanced trench technology to provide excellent R<sub>SS(ON)</sub>, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V V<sub>GS(MAX)</sub> rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

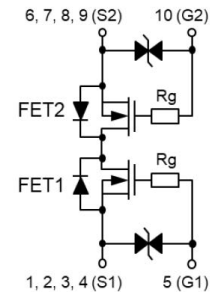
### Marking and pin assignment



Marking:

- |                        |                    |
|------------------------|--------------------|
| 1. 15221: Product Code | 1, 2, 3, 4 Source1 |
| 2. YYMMX: Date Code    | 6, 7, 8, 9 Source2 |
| 3. Solid dot: Pin 1    | 5 Gate1            |
|                        | 10 Gate2           |

### Equivalent Circuit



### ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V <sub>SSS</sub>	12	V
Gate-Source Voltage	V <sub>GSS</sub>	±8	V
Source Current(DC)	I <sub>S</sub> <sup>①</sup>	22.7	A
Source Current (Pulsed)	I <sub>SP</sub> <sup>①</sup>	227	A
Total Power Dissipation	P <sub>T</sub> <sup>①</sup>	1.6	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55 To 150	°C

# MOSFET ELECTRICAL CHARACTERISTICS

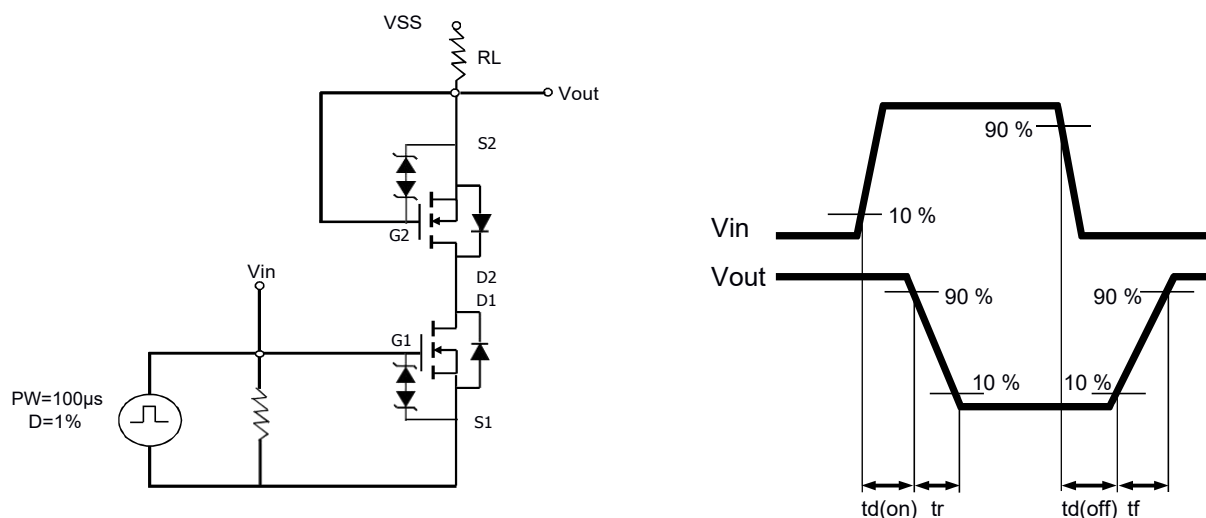
$T_a=25^{\circ}\text{C}$  unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
Source to Source Breakdown Voltage	$BV_{SSS}$	$I_S=1\text{mA}, V_{GS}=0\text{V}$	12			V
Zero-Gate Voltage Source Current	$I_{SSS}$	$V_{SS}=10\text{V}, V_{GS}=0\text{V}$			100	nA
Gate to Source Leakage Current	$I_{GSS}$	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$			$\pm 10$	$\mu\text{A}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{SS}=6\text{V}, I_S=1.11\text{mA}$	0.4	0.65	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=4.5\text{V}, I_S=2\text{A}$	0.6	1.1	1.4	$\text{m}\Omega$
		$V_{GS}=3.8\text{V}, I_S=2\text{A}$	0.6	1.3	1.5	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=2\text{A}$	0.7	1.4	1.6	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=2\text{A}$	1.0	1.7	2.9	$\text{m}\Omega$
Input Capacitance	$C_{iss}$	$V_{SS}=6\text{V}, V_{GS}=0\text{V}, f=1\text{kHz}$		4500		pF
Output Capacitance	$C_{oss}$			1500		pF
Reverse Transfer Capacitance	$C_{rss}$			1200		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{SS}=6\text{V}, R_L=0.6\Omega, V_{GS}=4\text{V}$		1.4		$\mu\text{s}$
Turn-on Rise Time	$t_r$			2.8		$\mu\text{s}$
Turn-off Delay Time	$t_{d(off)}$			6.9		$\mu\text{s}$
Turn-off Fall Time	$t_f$			6.5		$\mu\text{s}$
Total Gate Charge	$Q_g$	$V_{SS}=6\text{V}, I_S=10\text{A}, V_{GS}=4\text{V}$		43		nC
Gate1-source1 charge	$Q_{g1s1}$			7		nC
Gate1-source2 charge	$Q_{g1s2}$			17		nC
Diode Forward Voltage	$V_{F(S-S)}$	$V_{GS}=0\text{V}, I_S=2\text{A}$			1.2	V

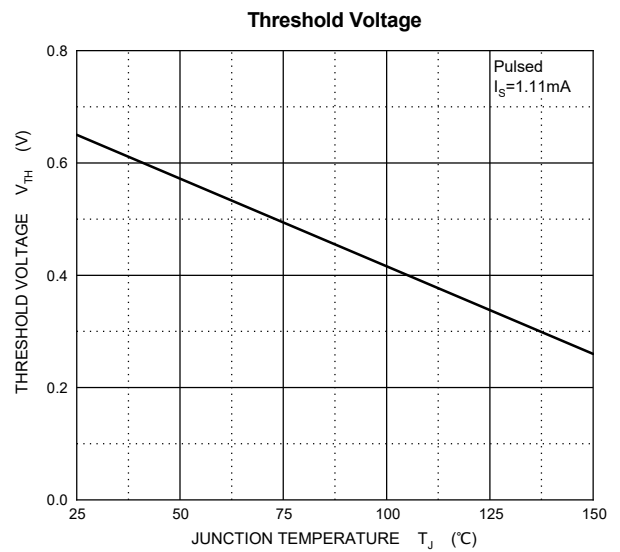
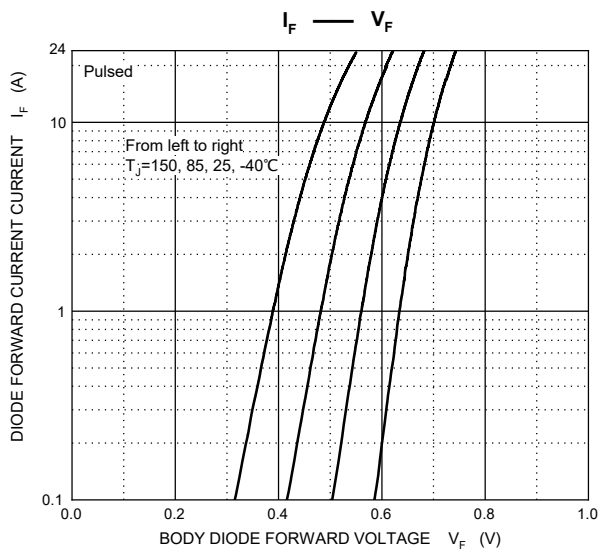
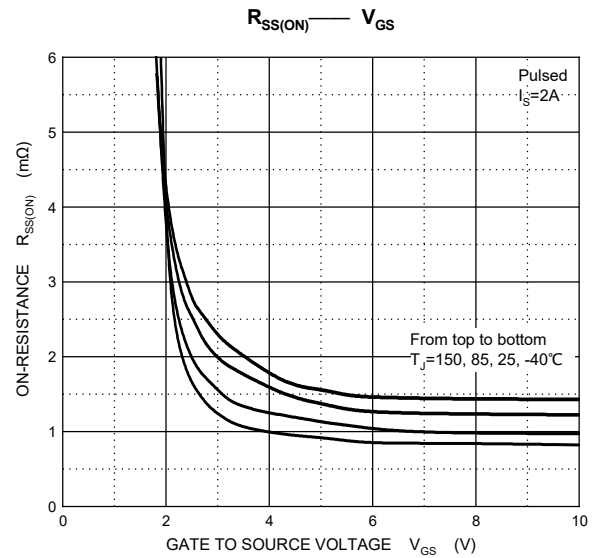
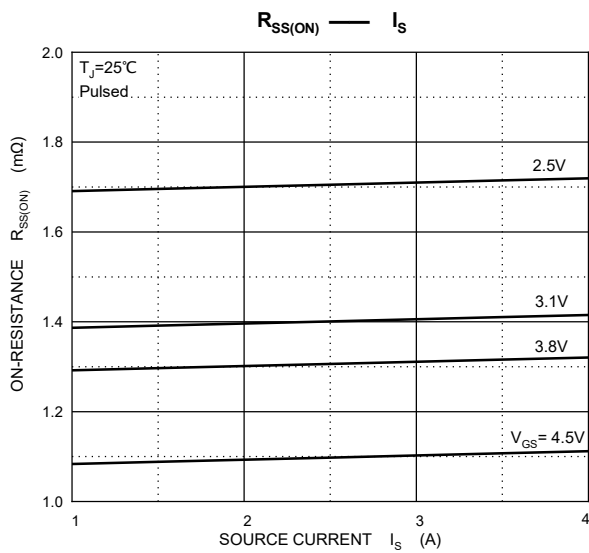
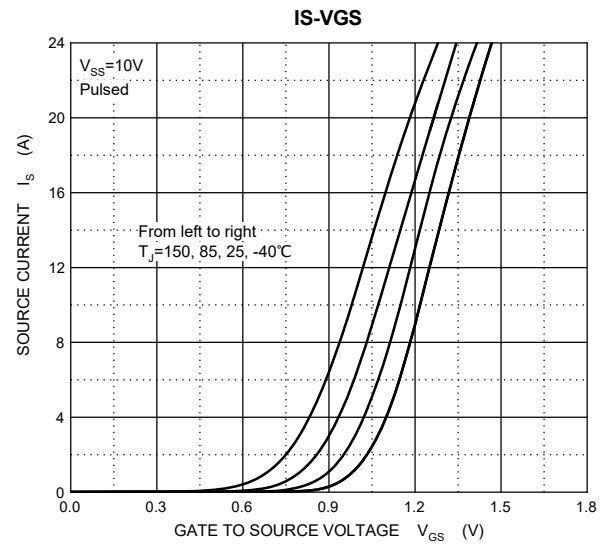
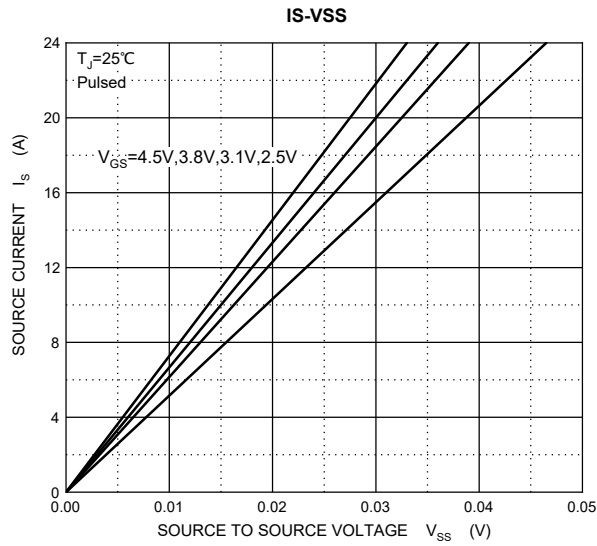
Notes: 1. Mounted on FR4 board partially covered with copper pad.

2.  $t = 10\ \mu\text{s}$ , Duty Cycle = 1%.

3. When FET1 is measured, G2 and S2 are short-circuited.

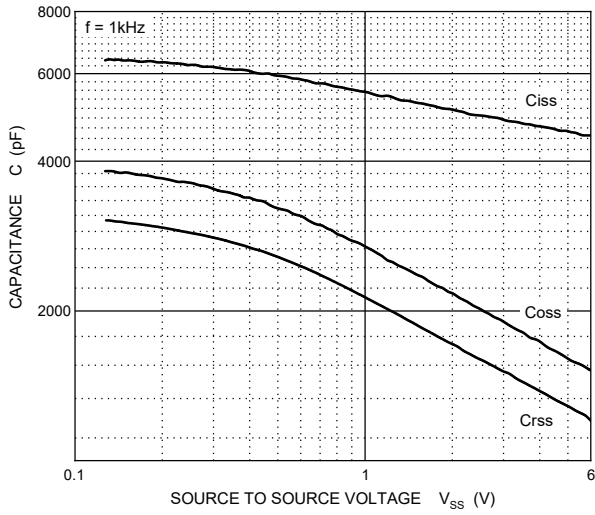


# Typical Characteristics

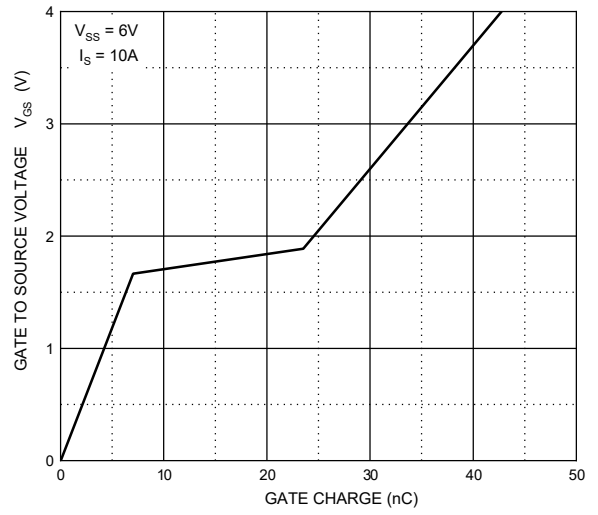


# Typical Characteristics

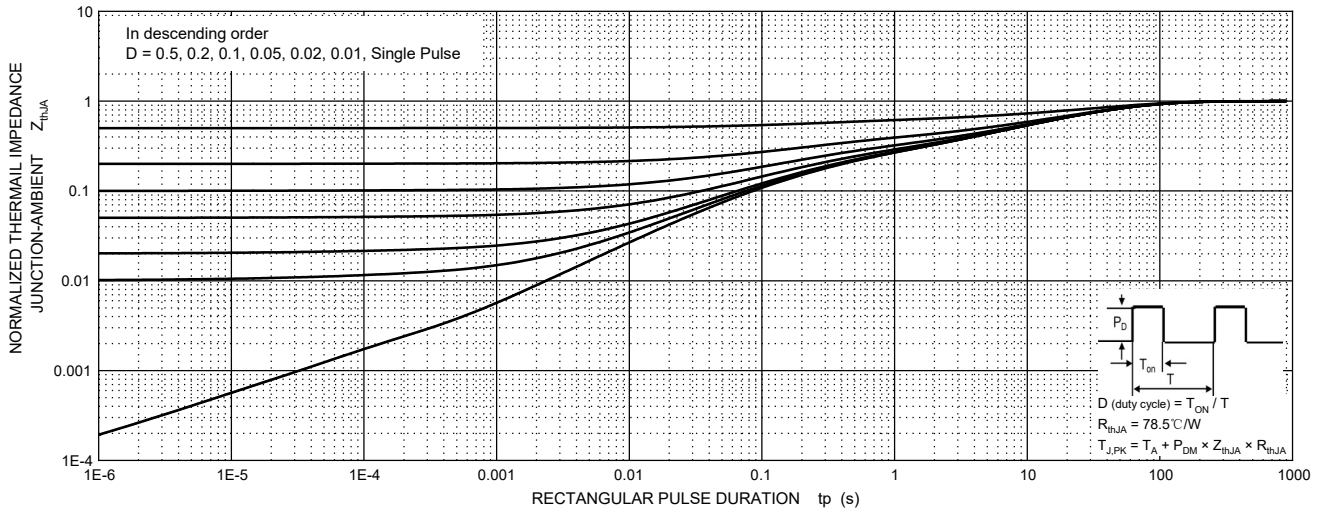
### Typical Capacitances



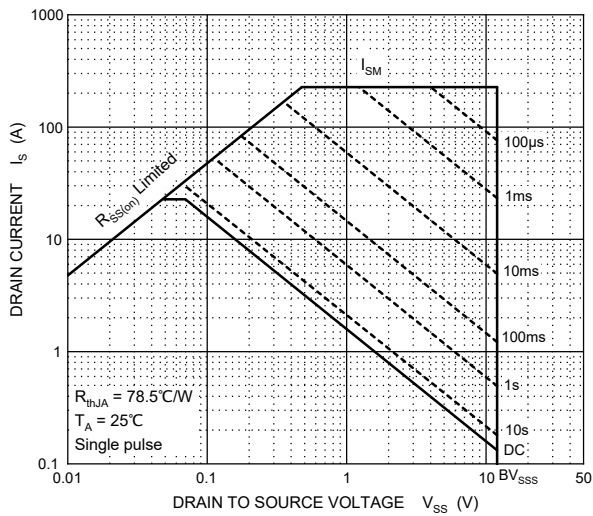
### Gate Charge



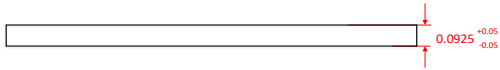
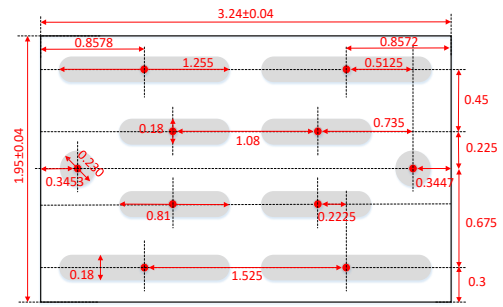
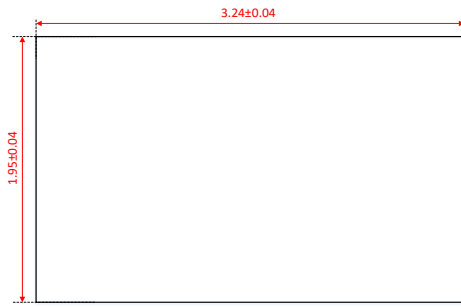
### Transient Thermal Impedance, Junction-Ambient



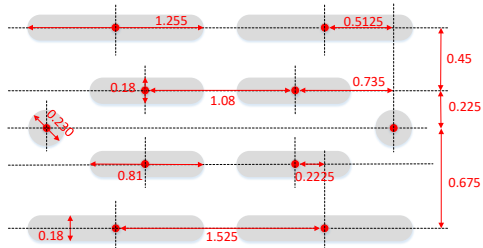
### Maximum Safe Operating Area



## CSPC3220-10 Package Outline Dimensions(Unit:mm)



## CSPC3220-10 Suggested Pad Layout (Unit:mm)



### Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.050$  mm.
3. The pad layout is for reference purposes only.

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