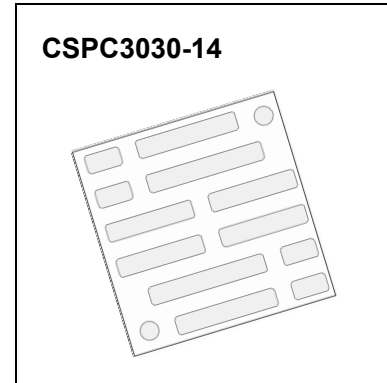




CSP Enhancement Mode Power MOSFET

CJ17133SP Dual N-Channel MOSFET

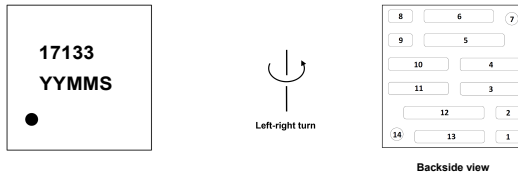
V _{SSS}	R _{SS(on)} TYP	I _S
24V	1.35mΩ@10V	16A
	1.50mΩ@8V	
	2.55mΩ@4.5V	



DESCRIPTION

The CJ17133SP uses advanced trench technology to provide excellent R_{SS(ON)}, low gate charge and operation with gate voltages as low as 4.5V while retaining a 16V V_{GS(MAX)} rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

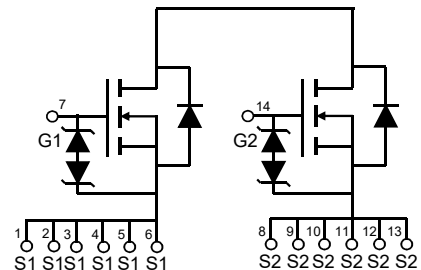
Marking and pin assignment



Marking:

- | | | |
|------------------------|-----------------|---------|
| 1. 17133: Product Code | 1,2,3,4,5,6 | Source1 |
| 2. YYMMS: Date Code | 8,9,10,11,12,13 | Source2 |
| 3. Solid dot: Pin 1 | 7 | Gate1 |
| | 14 | Gate2 |

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

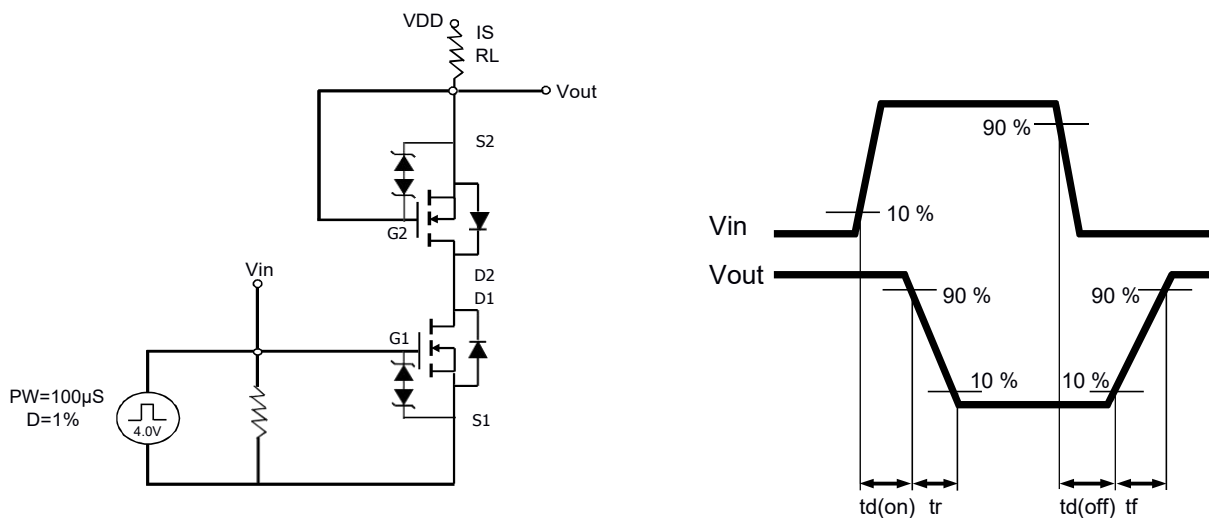
Parameter	Symbol	Limit	Unit
Source to Source Voltage	V _{SSS}	24	V
Gate-Source Voltage	V _{GSS}	±16	V
Source Current(DC)	I _S ^①	16	A
Source Current (Pulsed)	I _{SP} ^①	160	A
Total Power Dissipation	P _T ^①	1.3	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature Range	T _{STG}	-55 To 150	°C

MOSFET ELECTRICAL CHARACTERISTICS

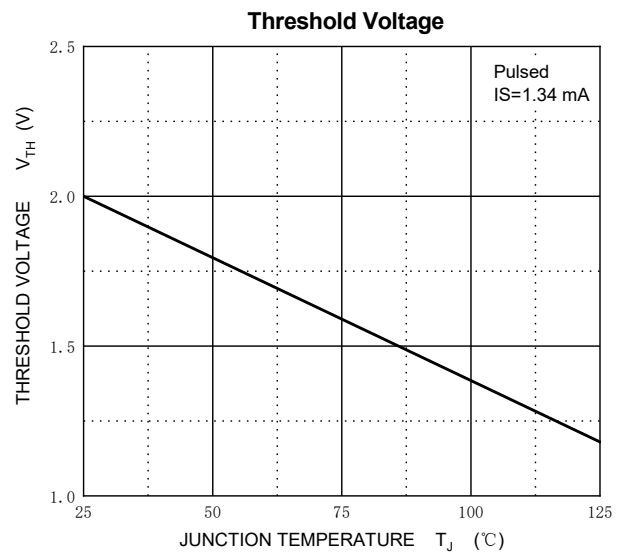
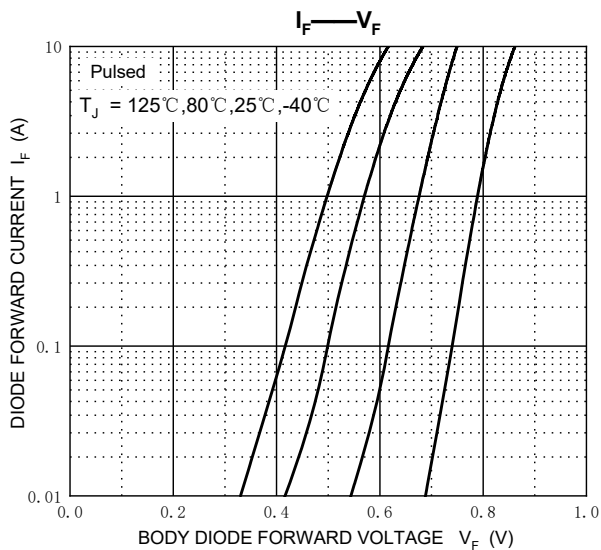
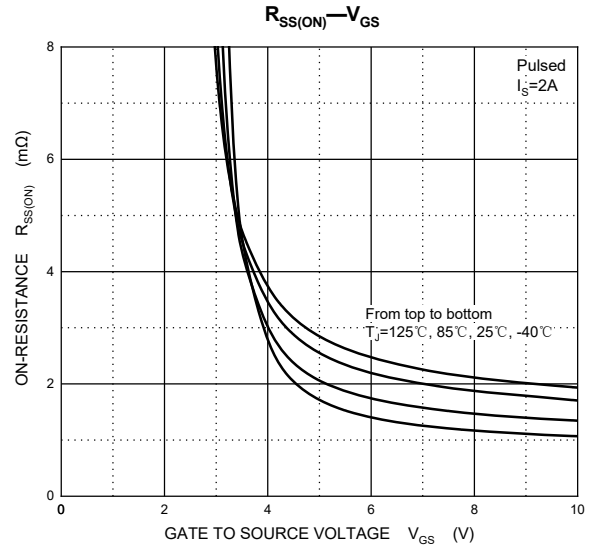
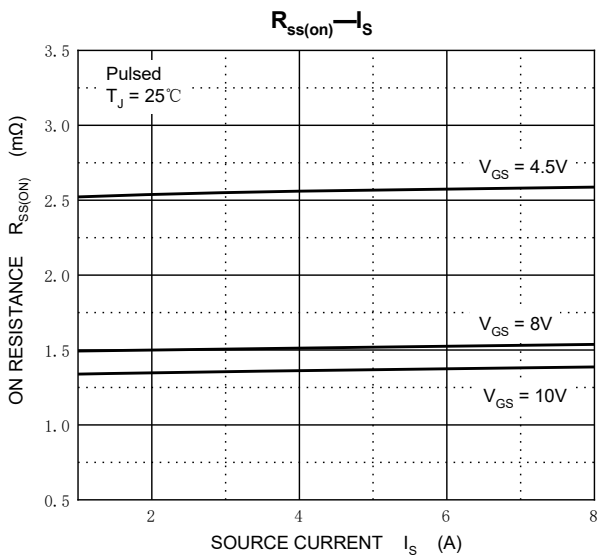
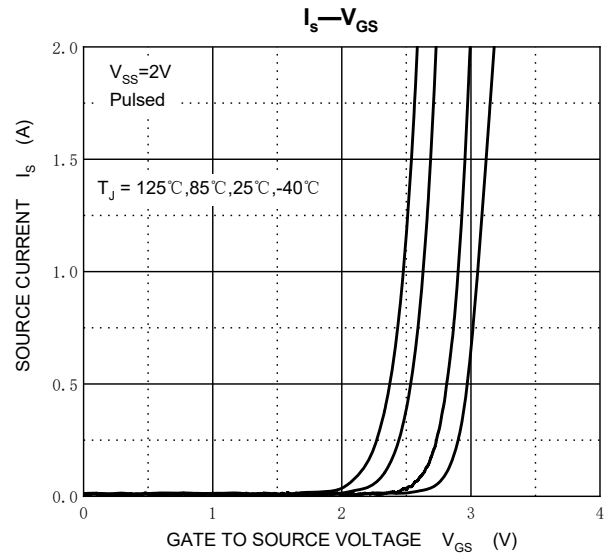
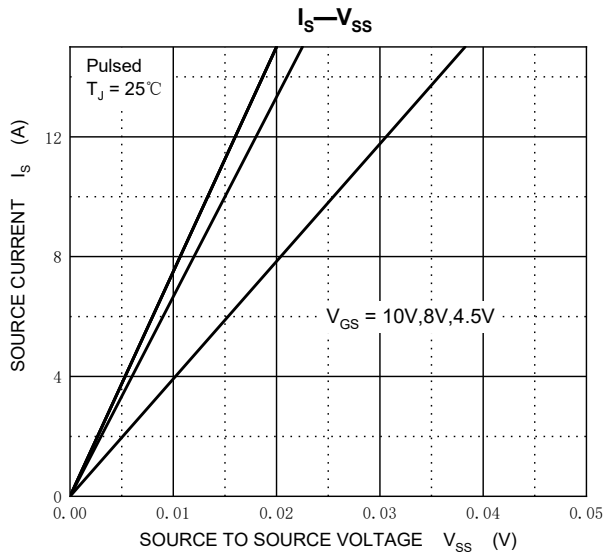
$T_A=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	$I_S=1\text{mA}, V_{GS}=0\text{V}$	24			V
Zero-Gate Voltage Source Current	I_{SSS}	$V_{SS}=24\text{V}, V_{GS}=0\text{V}$			1.0	μA
Gate to Source Leakage Current	I_{GSS1}	$V_{SS}=0\text{V}, V_{GS}=\pm 16\text{V}$			± 10	μA
	I_{GSS2}	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$			1.0	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{SS}=10\text{V}, I_S=1.34\text{ mA}$	1	2	3	V
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=10\text{V}, I_S=2.0\text{A}$	0.8	1.35	1.85	$\text{m}\Omega$
		$V_{GS}=8\text{V}, I_S=2.0\text{A}$	0.9	1.50	2.35	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_S=2.0\text{A}$	1.3	2.55	4.8	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}, V_{SS}=10\text{V}, f=1\text{kHz}$		3570		pF
Output Capacitance	C_{oss}		720	pF		
Reverse Transfer Capacitance	C_{rss}		559	pF		
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=12\text{V}, R_L=1.5\Omega, V_{GS}=10\text{V}$		215		nS
Turn-on Rise Time	t_r		330	nS		
Turn-off Delay Time	$t_{d(off)}$		1.5	μS		
Turn-off Fall Time	t_f		1.1	μS		
Total Gate Charge	Q_g	$V_{DD}=12\text{V}, V_{GS}=10\text{V}, I_D=6\text{A}$		67		nC
Gate1-source1 charge	Q_{g1s1}		10	nC		
Gate1-source2 charge	Q_{g1s2}		20.6	nC		
Diode Forward Voltage	$V_{F(S-S)}^{(4)}$	$V_{GS}=0\text{V}, I_S=2\text{A}$			1.0	V

- Notes: 1. Mounted on FR4 board (25.4mx25.4mmx1.0mm) using minimum recommended pad size (partial coverage of single-sided 36um Copper).
 2. $t = 10\text{ }\mu\text{s}$, Duty Cycle = 1%.
 3. When FET1 is measured, G2 and S2 are short-circuited.
 4. When FET1 is measured, G2 and S2 are biased with $V_{G2S2}=10\text{V}$.

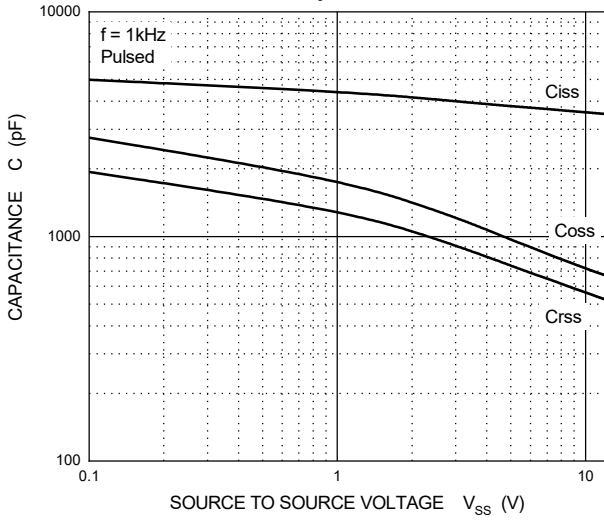


Typical Characteristics

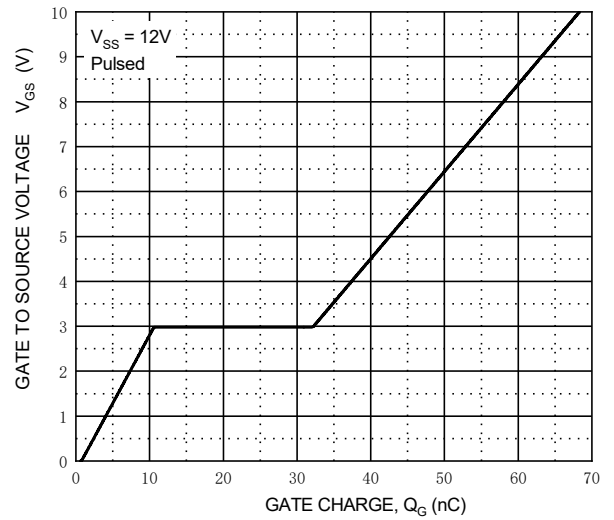


Typical Characteristics

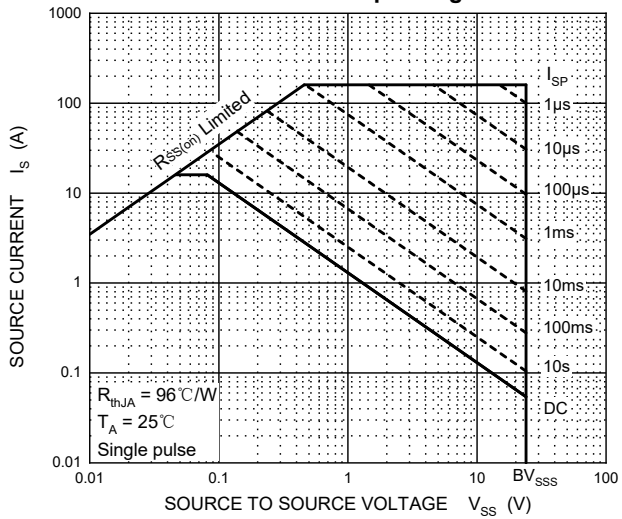
Capacitances



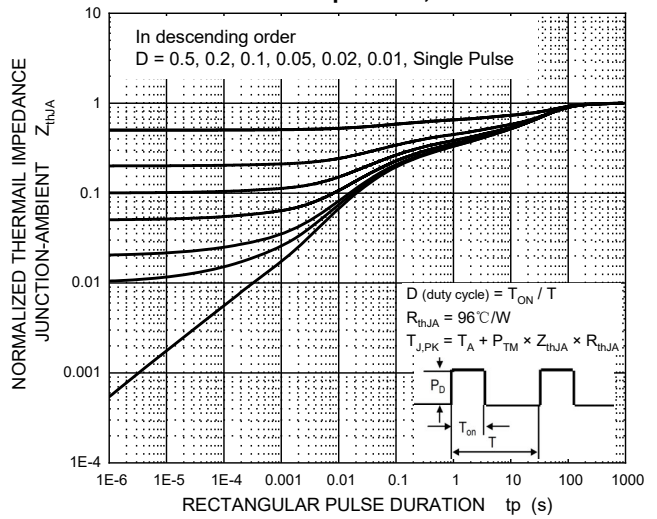
Gate Charge



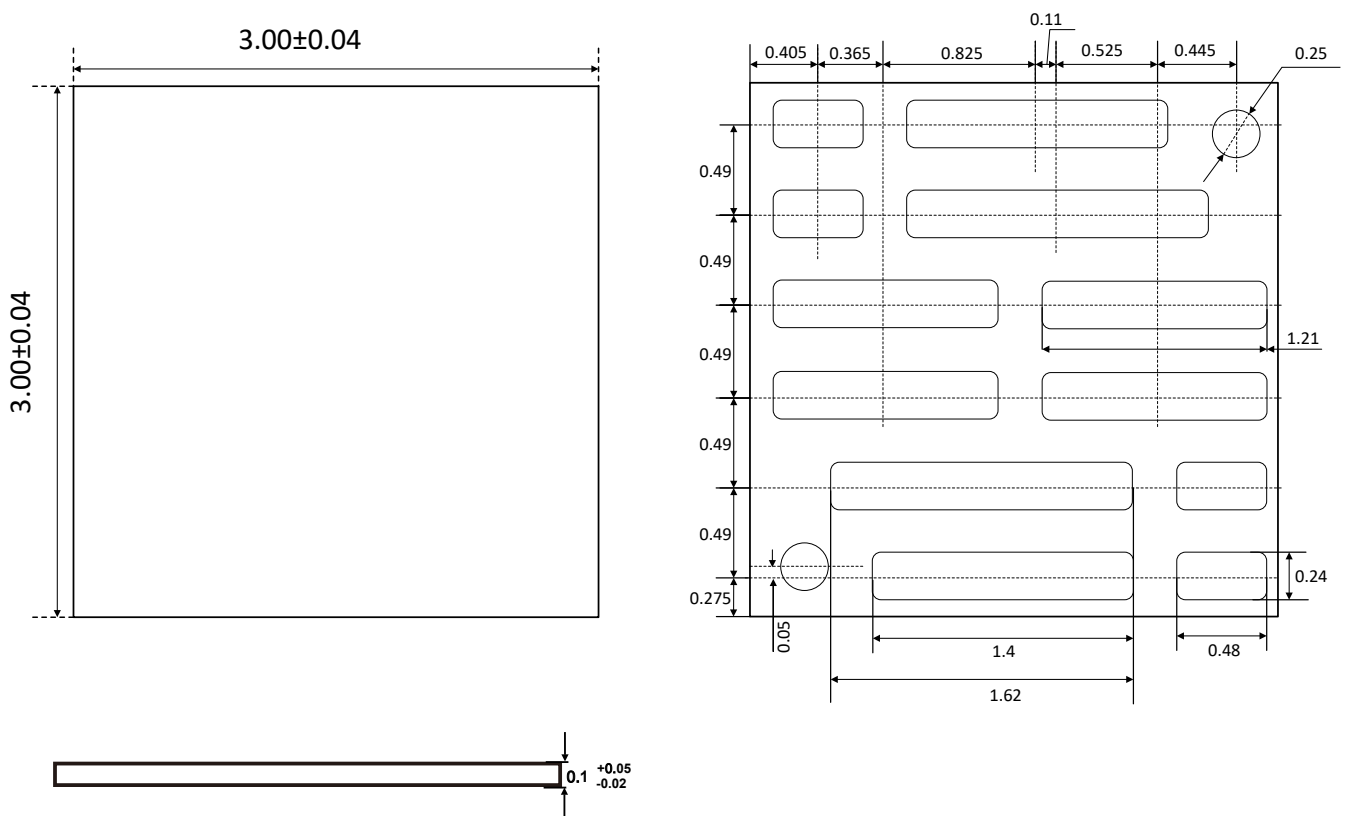
Maximum Safe Operating Area



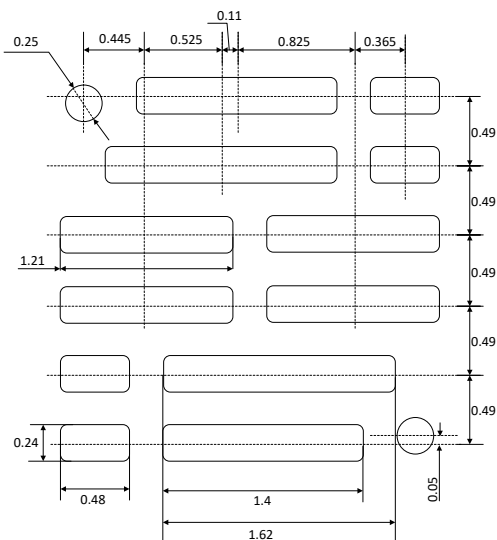
Transient Thermal Impedance, Junction-Ambient



CSPC3030-14 Package Outline Dimensions(Unit:mm)



CSPC3030-14 Suggested Pad Layout (Unit:mm)



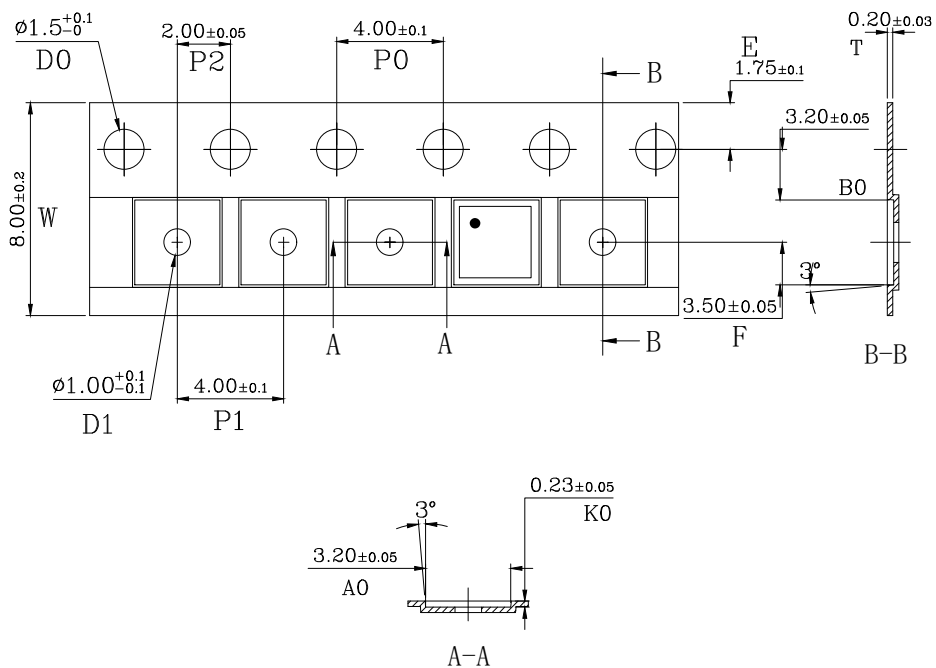
Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.050 mm.
3. The pad layout is for reference purposes only.

NOTICE

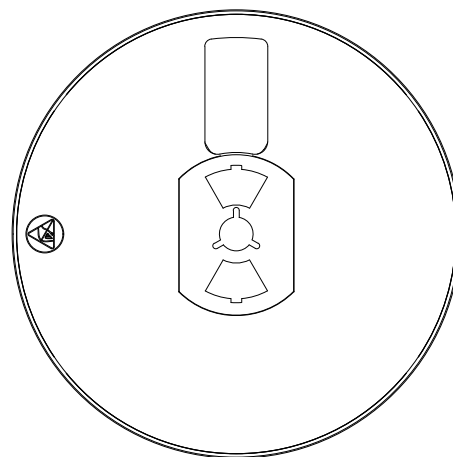
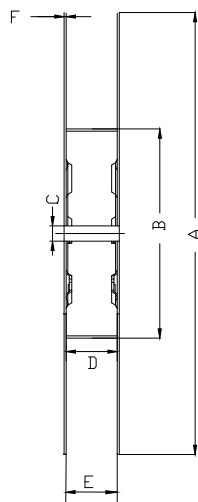
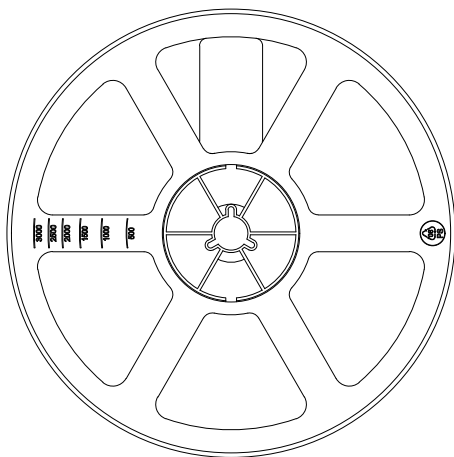
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Tape and Reel



产品尺寸规格(UNT:mm)

规格	W	P1	E	F	D0	D1
尺寸	8.00±0.20	4.00±0.10	1.75±0.10	3.50±0.05	1.50 ^{+0.1} ₋₀	1.00±0.10
规格	A0	B0	K0	T	P0	P2
尺寸	3.20±0.05	3.20±0.05	0.23±0.05	0.20±0.03	4.00±0.10	2.00±0.05



SIZE	8MM
A	178±2.0
B	55±1.0
C	13.0 ^{+0.35} _{-0.15}
D	8.4 ^{+2.5} _{-0.4}
E	8.65 ^{+4.7} _{-0.65}
F	1.5±0.5

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