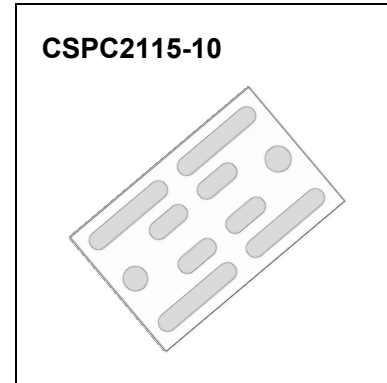




CSP Enhancement Mode Power MOSFET

CJ25223SP-B Dual N-Channel MOSFET

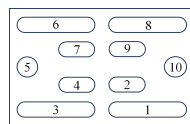
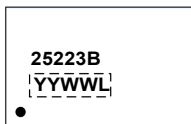
V _{SSS}	R _{SS(on)} TYP	I _S
12V	2.3mΩ@4.5V	13.5A
	2.5mΩ@3.8V	
	3.0mΩ@3.1V	
	4.1mΩ@2.5V	



DESCRIPTION

The CJ25223SP-B uses advanced trench technology to provide excellent R_{SS(ON)}, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V V_{GS(MAX)} rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment

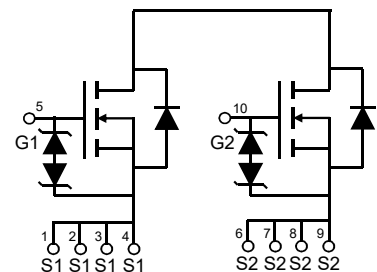


Backside view

Marking:

- | | |
|-------------------------|--------------------|
| 1. 25223B: Product Code | 1, 2, 3, 4 Source1 |
| 2. YYWWL: Date Code | 6, 7, 8, 9 Source2 |
| 3. Solid dot: Pin 1 | 5 Gate1 |
| | 10 Gate2 |

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

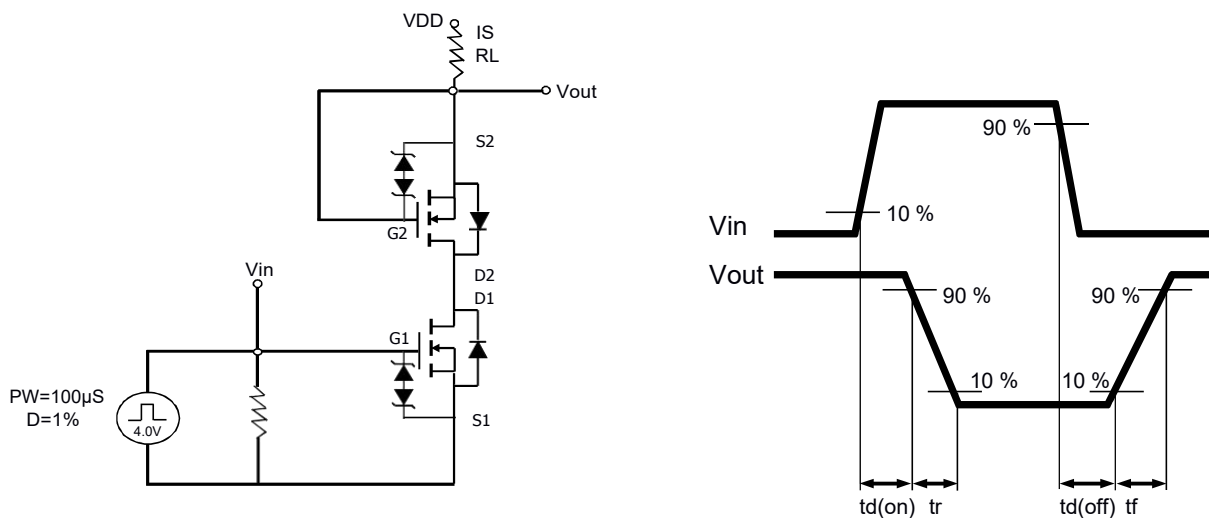
Parameter	Symbol	Limit	Unit
Source to Source Voltage	V _{SSS}	12	V
Gate-Source Voltage	V _{GSS}	±8	V
Source Current(DC)	I _S ^①	13.5	A
Source Current (Pulsed)	I _{SP} ^①	135	A
Total Power Dissipation	P _T ^①	0.58	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature Range	T _{STG}	-55 To 150	°C

MOSFET ELECTRICAL CHARACTERISTICS

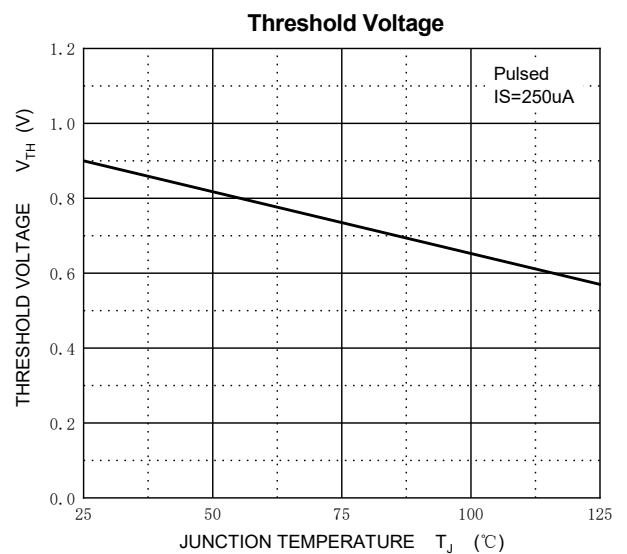
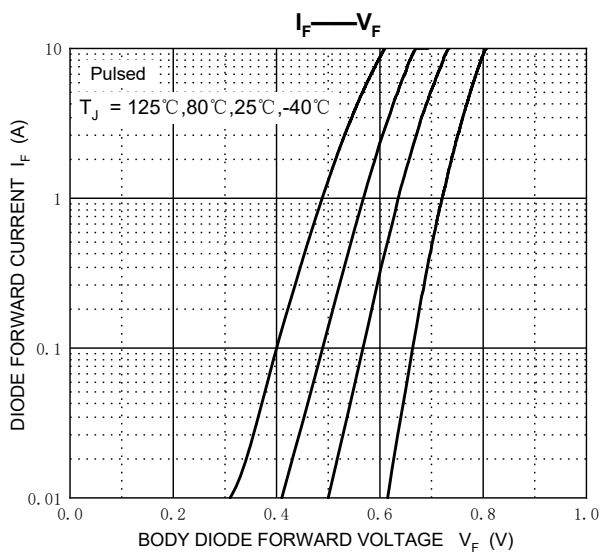
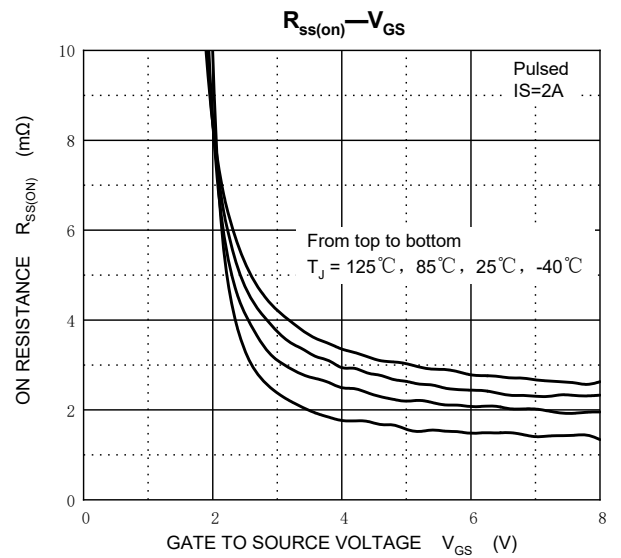
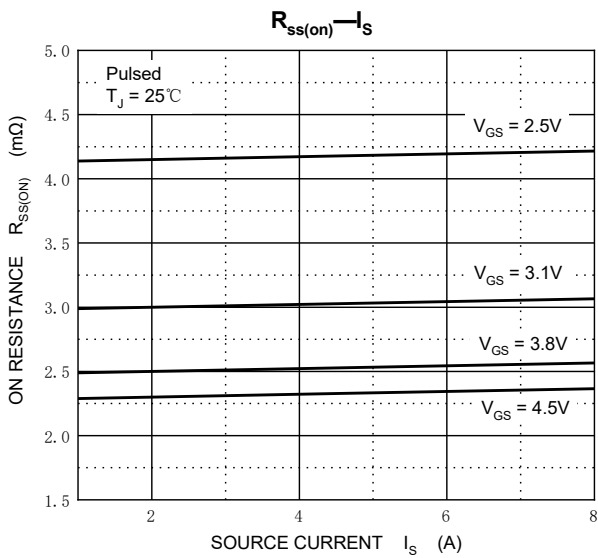
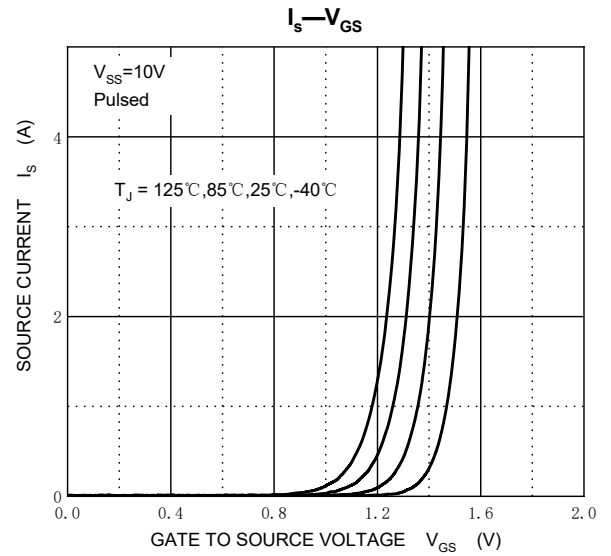
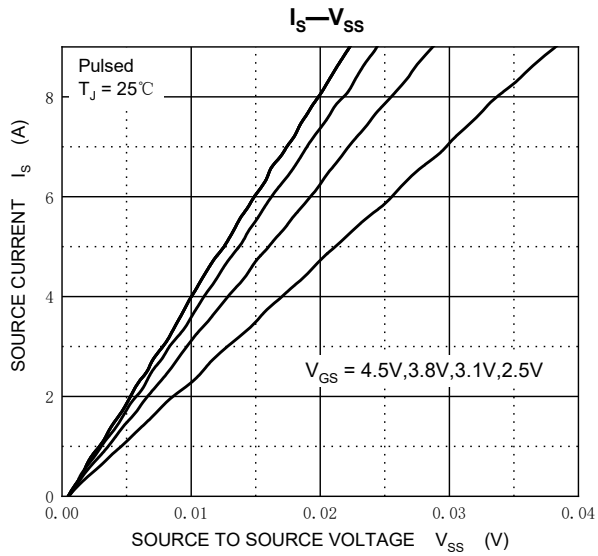
$T_A=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	$I_S=1\text{mA}, V_{GS}=0\text{V}$	12			V
Zero-Gate Voltage Source Current	I_{SSS}	$V_{SS}=12\text{V}, V_{GS}=0\text{V}$			1.0	μA
Gate to Source Leakage Current	I_{GSS}	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$			± 10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{SS}=10\text{V}, I_S=250\text{ }\mu\text{A}$	0.35	0.90	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=4.5\text{V}, I_S=2.0\text{A}$	1.6	2.3	2.9	$\text{m}\Omega$
		$V_{GS}=3.8\text{V}, I_S=2.0\text{A}$	1.7	2.5	3.2	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=2.0\text{A}$	2.1	3.0	3.9	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=2.0\text{A}$	2.8	4.1	5.8	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}, V_{SS}=10\text{V}, f=1\text{kHz}$		1680		pF
Output Capacitance	C_{oss}			357		pF
Reverse Transfer Capacitance	C_{rss}			306		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=6\text{V}, R_L=1.5\Omega, V_{GS}=4\text{V}$		214		nS
Turn-on Rise Time	t_r			763		nS
Turn-off Delay Time	$t_{d(off)}$			1.2		μS
Turn-off Fall Time	t_f			1.9		μS
Total Gate Charge	Q_g	$V_{DD}=6\text{V}, V_{GS}=4\text{V}, I_D=10\text{A}$		22		nC
Gate1-source1 charge	Q_{g1s1}			2.5		nC
Gate1-source2 charge	Q_{g1s2}			9.48		nC
Diode Forward Voltage	$V_{F(S-S)}^{(4)}$	$V_{GS}=0\text{V}, I_S=2\text{A}$			1.0	V

- Notes: 1. Mounted on FR4 board (25.4mx25.4mmx1.0mm) using minimum recommended pad size (partial coverage of single-sided 36um Copper).
 2. $t = 10\text{ }\mu\text{s}$, Duty Cycle = 1 %.
 3. When FET1 is measured, G2 and S2 are short-circuited.
 4. When FET1 is measured, G2 and S2 are biased with $V_{G2S2}=4.5\text{V}$.

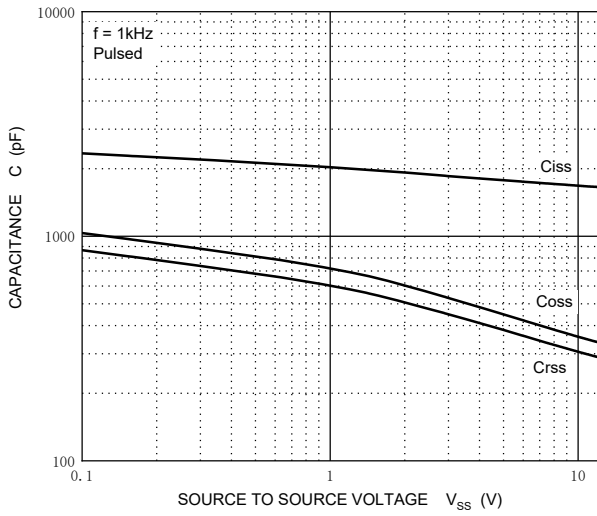


Typical Characteristics

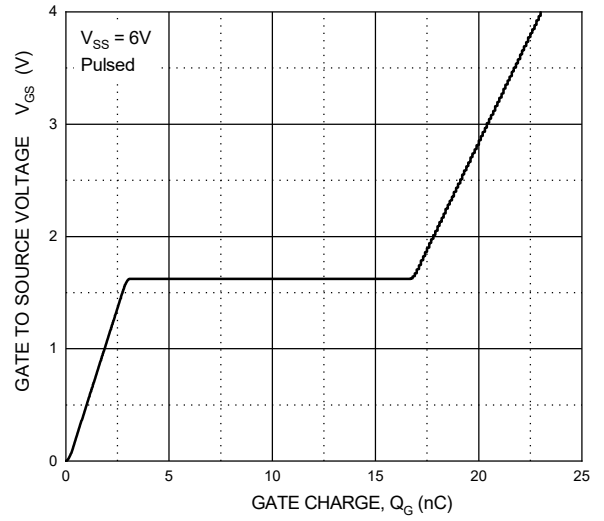


Typical Characteristics

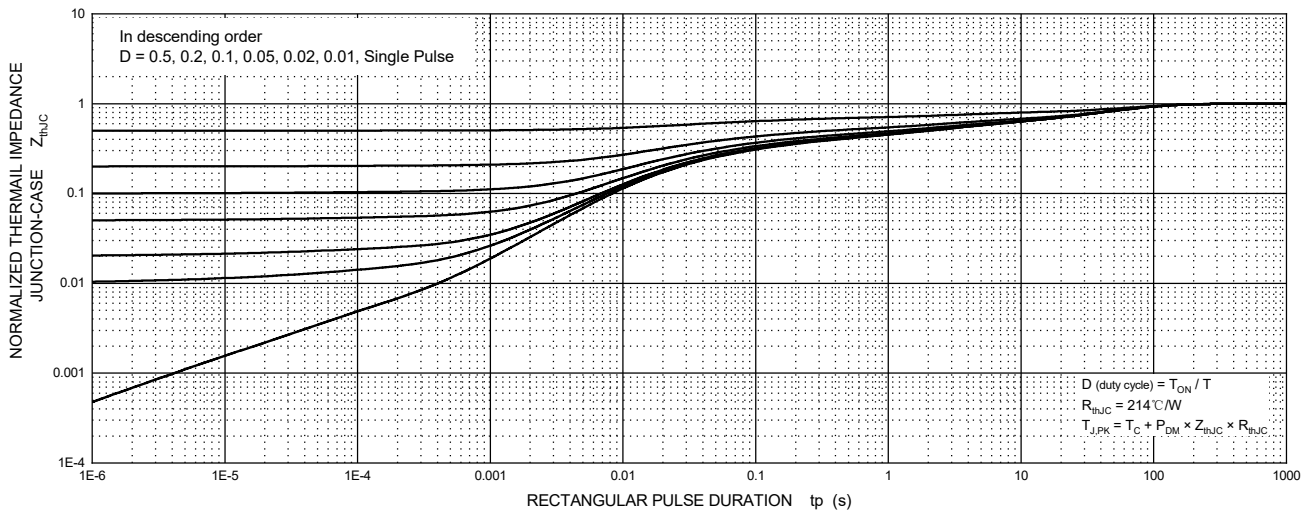
Capacitances



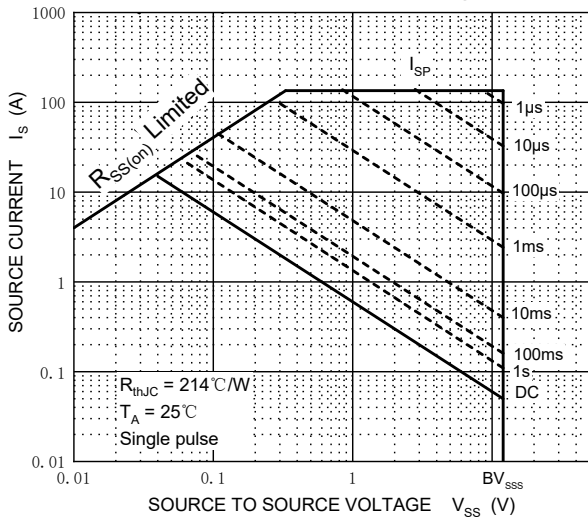
Gate Charge



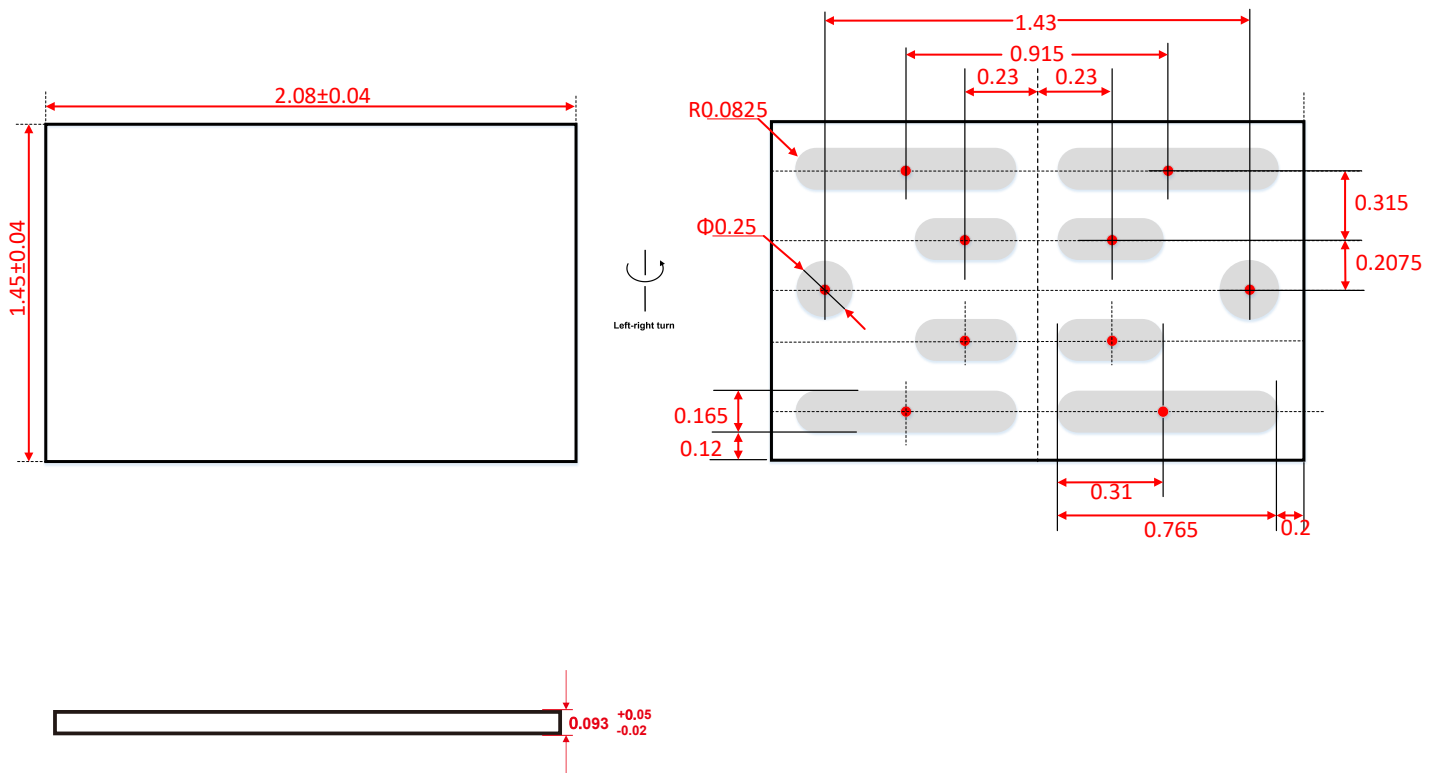
Transient Thermal Impedance, Junction-Case



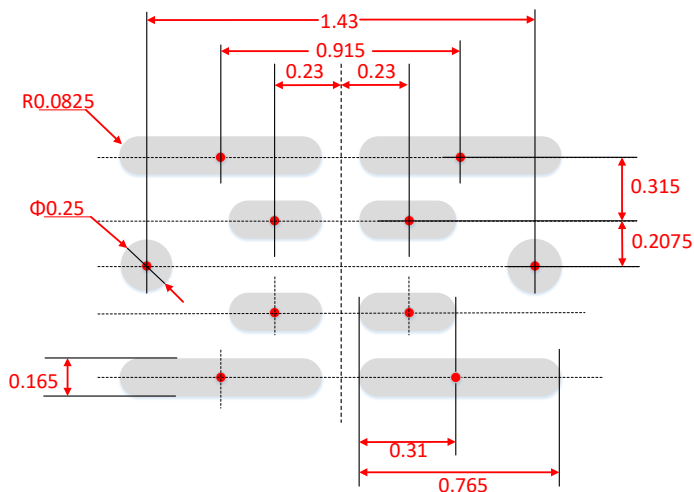
Maximum Safe Operating Area



CSPC2115-10 Package Outline Dimensions(Unit:mm)



CSPC2115-10 Suggested Pad Layout (Unit:mm)



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.050 mm.
3. The pad layout is for reference purposes only.

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