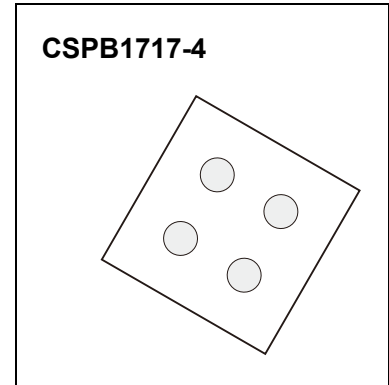




## CSP Enhancement Mode Power MOSFET

### CJ4506SP Dual N-Channel MOSFET

V <sub>SSS</sub>	R <sub>SS(on)</sub> TYP	I <sub>S</sub>
20V	11.2mΩ@4.5V	10A
	11.5mΩ@4.0V	
	11.8mΩ@3.7V	
	12.7mΩ@3.1V	
	14.7mΩ@2.5V	

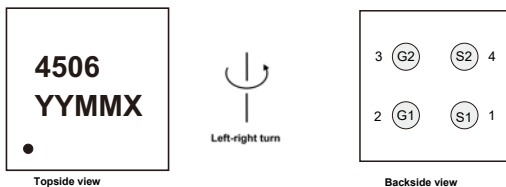


#### DESCRIPTION

The CJ4506SP uses advanced trench technology to provide excellent R<sub>SS(ON)</sub>, low gate charge and operation with gate voltages as low as 2.5V while retaining a 12V V<sub>GS(MAX)</sub> rating. It is ESD protected.

This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

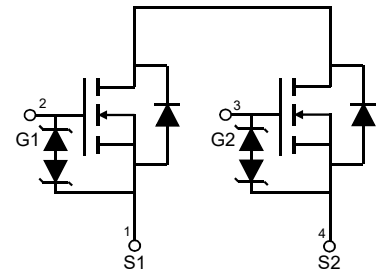
#### Marking and pin assignment



Marking:

- |                       |           |
|-----------------------|-----------|
| 1. 4506: Product Code | 1 Source1 |
| 2. YYMMX: Date Code   | 2 Gate1   |
| 3. Solid dot: Pin 1   | 3 Gate2   |
|                       | 4 Source2 |

#### Equivalent Circuit



#### ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V <sub>SSS</sub>	20	V
Gate-Source Voltage	V <sub>GSS</sub>	±12	V
Source Current(DC)	I <sub>S</sub> <sup>①</sup>	10	A
Source Current (Pulsed)	I <sub>SP</sub> <sup>①</sup>	100	A
Total Power Dissipation	P <sub>T</sub> <sup>①</sup>	2.1	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55 To 150	°C

# MOSFET ELECTRICAL CHARACTERISTICS

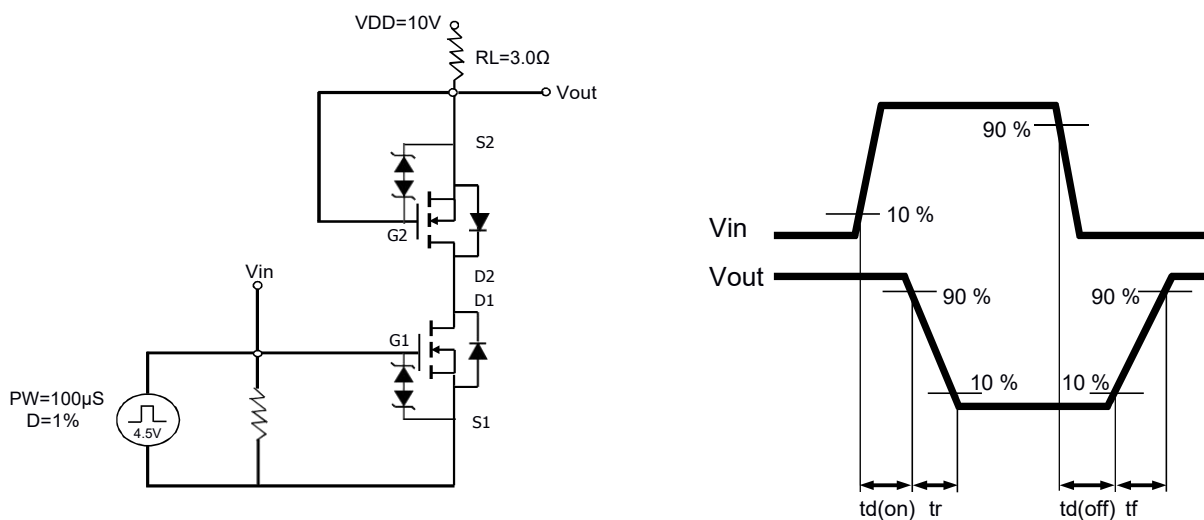
$T_a=25\text{ }^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
Source to Source Breakdown Voltage	$BV_{SSS}$	$I_S=1\text{mA}, V_{GS}=0\text{V}$	20			V
Zero-Gate Voltage Source Current	$I_{SSS}$	$V_{SS}=16\text{V}, V_{GS}=0\text{V}$			1.0	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{SS}=0\text{V}, V_{GS}=\pm 10\text{V}$			$\pm 10$	$\mu\text{A}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{SS}=V_{GS}, I_S=250\mu\text{A}$	0.3	0.88	1.1	V
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=4.5\text{V}, I_S=3\text{A}$	7.8	11.2	13.5	$\text{m}\Omega$
		$V_{GS}=4.0\text{V}, I_S=3\text{A}$	8.0	11.5	14.1	$\text{m}\Omega$
		$V_{GS}=3.7\text{V}, I_S=3\text{A}$	8.2	11.8	15.5	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=3\text{A}$	8.9	12.7	17.0	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=3\text{A}$	10.3	14.7	21.4	$\text{m}\Omega$
Input Capacitance	$C_{iss}$			1746		pF
Output Capacitance	$C_{oss}$	$V_{SS}=10\text{V}, V_{GS}=0\text{V}, f=1\text{kHz}$		260		pF
Reverse Transfer Capacitance	$C_{rss}$			189		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10\text{V}, R_L=3\Omega, V_{GS}=4.5\text{V}$		0.38		$\mu\text{s}$
Turn-on Rise Time	$t_r$			0.56		$\mu\text{s}$
Turn-off Delay Time	$t_{d(off)}$			2.54		$\mu\text{s}$
Turn-off Fall Time	$t_f$			1.01		$\mu\text{s}$
Total Gate Charge	$Q_g$				28	
Gate1-source1 charge	$Q_{g1s1}$	$V_{SS}=10\text{V}, I_S=5\text{A}, V_{GS}=8\text{V}$		3.5		nC
Gate1-source2 charge	$Q_{g1s2}$			6.0		nC
Diode Forward Voltage	$V_{F(S-S)}$	$V_{GS}=0\text{V}, I_S=1\text{A}$			1.0	V

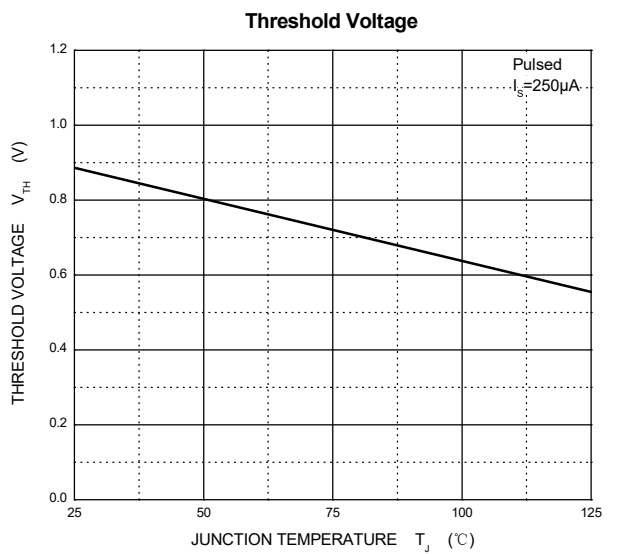
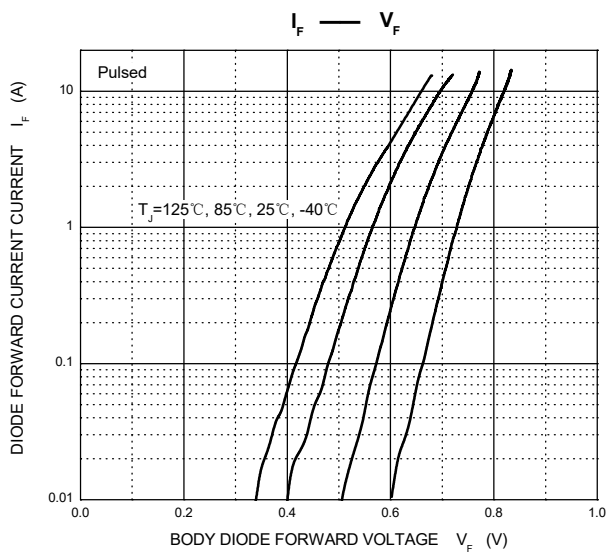
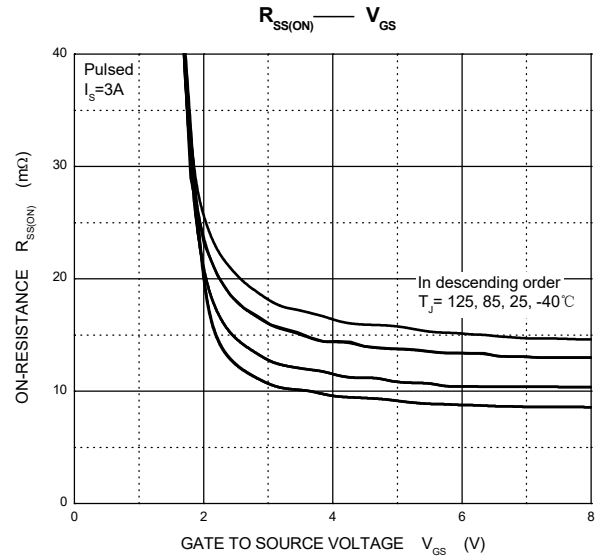
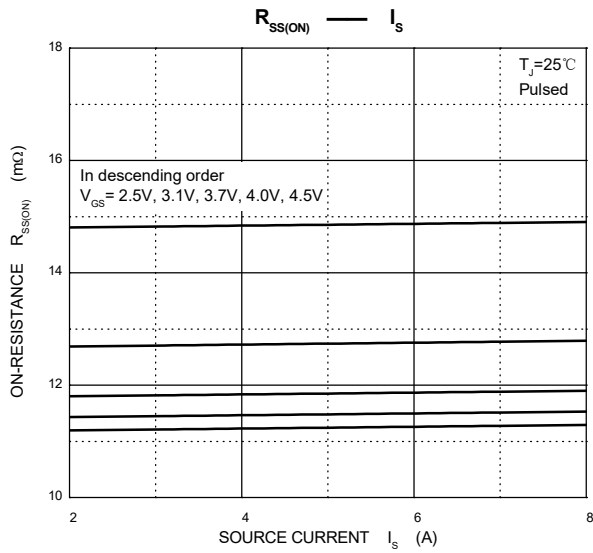
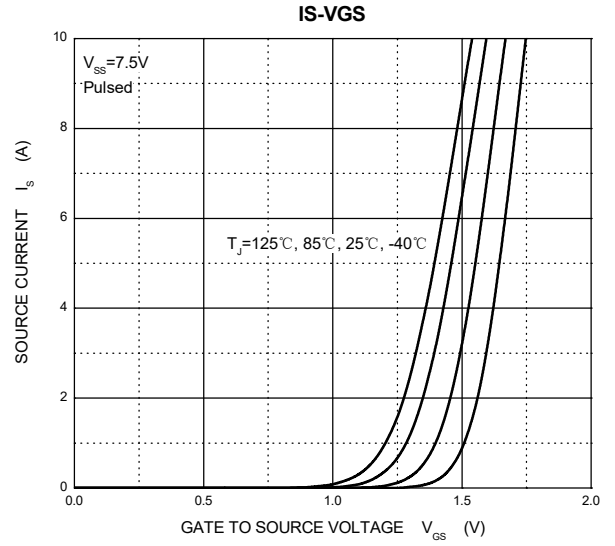
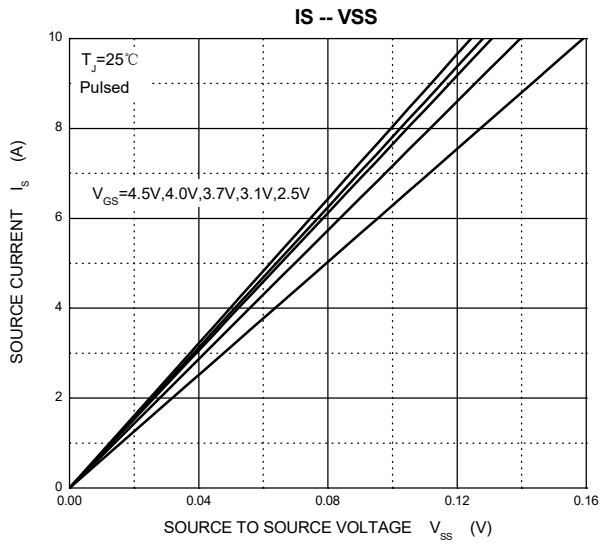
Notes: 1. Mounted on FR4 board (25.4mm×25.4mm×1.0mm) using the minimum recommended pad size (36um Copper ).

2.  $t = 10\text{ ms}$  , Duty Cycle = 1 %.

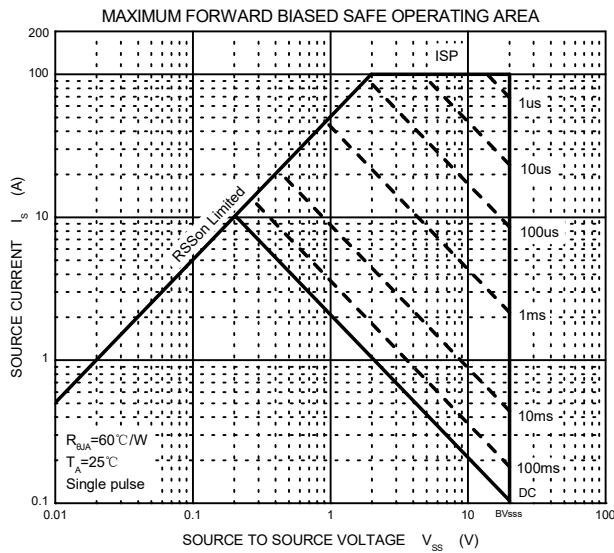
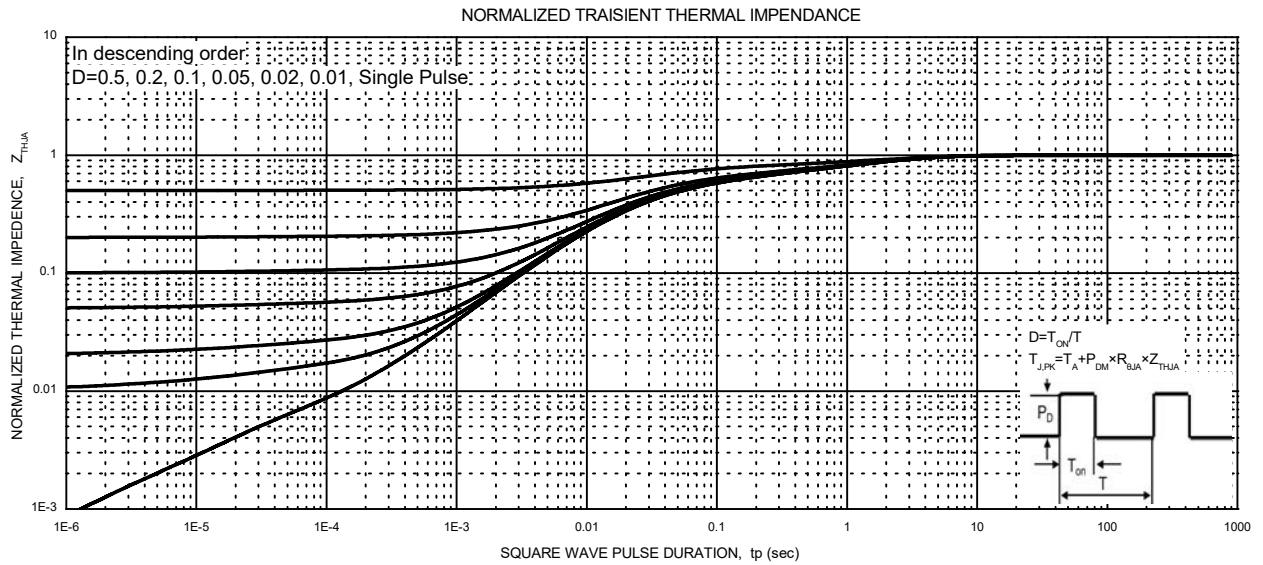
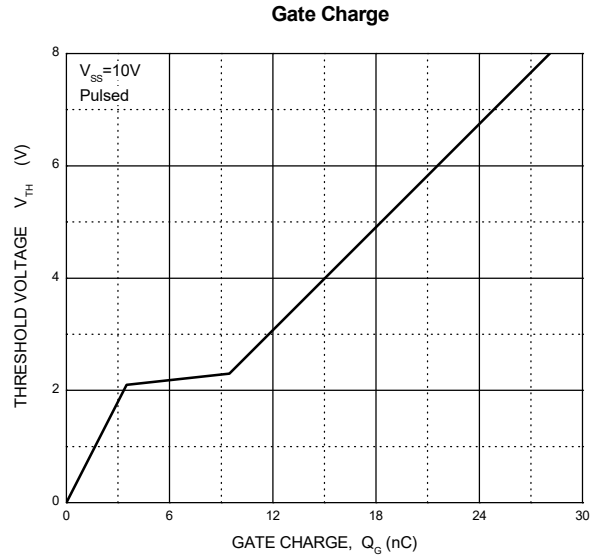
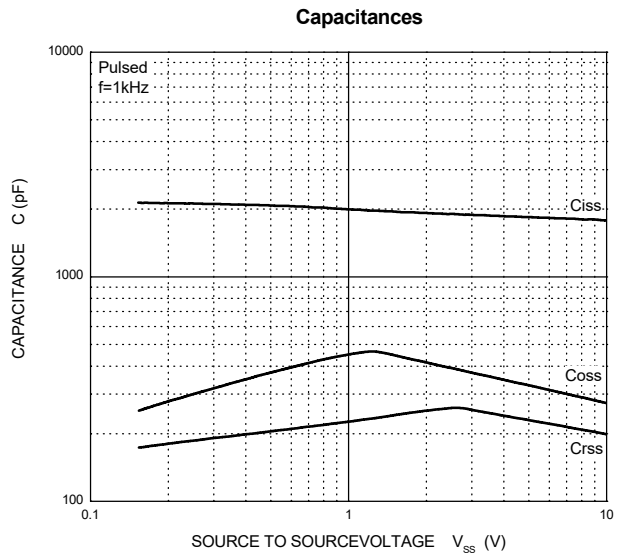
3. When FET1 is measured, G2 and S2 are short-circuited.



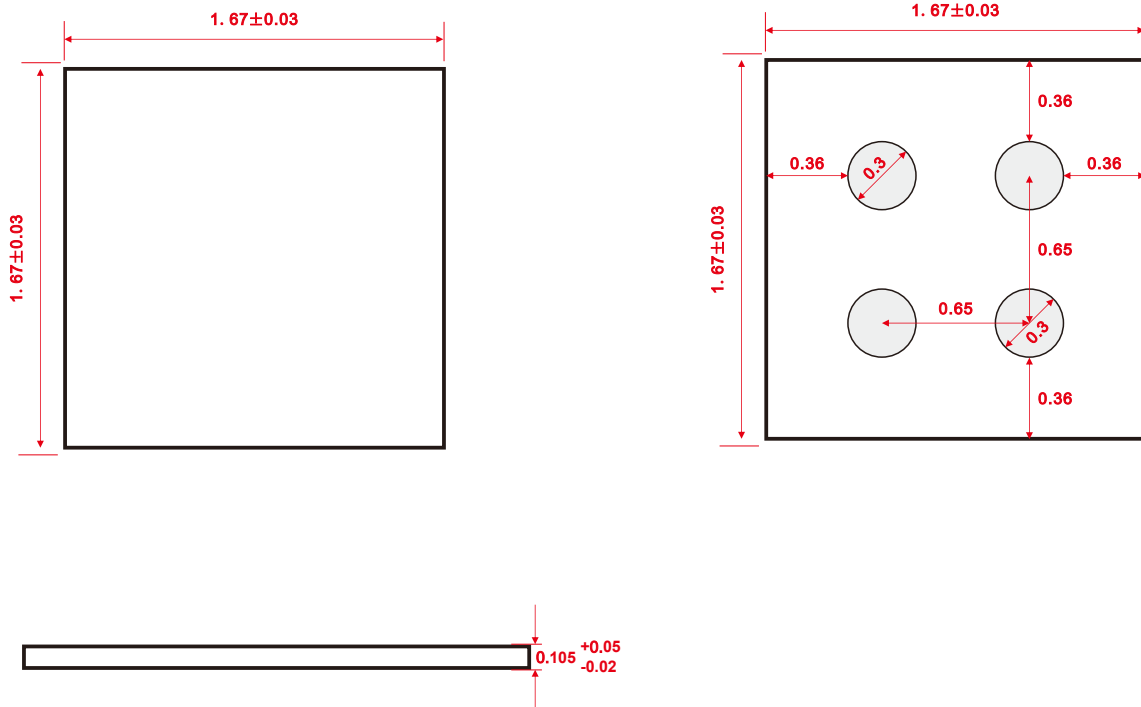
# Typical Characteristics



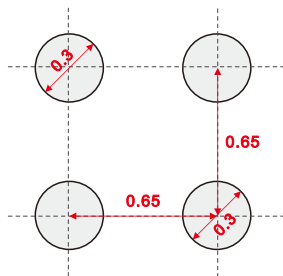
# Typical Characteristics



**CSPB1717-4 Package Outline Dimensions(Unit:mm)**



**CSPB1717-4 Suggested Pad Layout (Unit:mm)**



- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.050$  mm.
  3. The pad layout is for reference purposes only.

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