General Purpose Timers

CJ555 Timer

1 Introduction

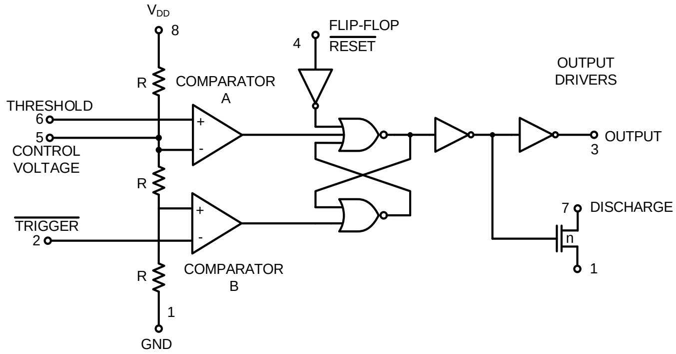
The CJ555 is a CMOS RC timer providing significantly improved performance over the standard SE/NE 555 timer, while at the same time being a direct replacement for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low Threshold, Trigger and Reset currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple Control Voltage for stable operation.

Specifically, the CJ555 is a stable controller capable of producing accurate time delays or frequencies. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555 device, the Control Voltage terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

2 Available Packages

PART NUMBER	PACKAGE
CJ555	SOP8

Note: For all available packages, please refer to the part Orderable Information.



Functional diagram

3 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ555AAN	SOP8	-40~105°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

4 Pin Configuration and Marking Information

4.1 Pin Configuration

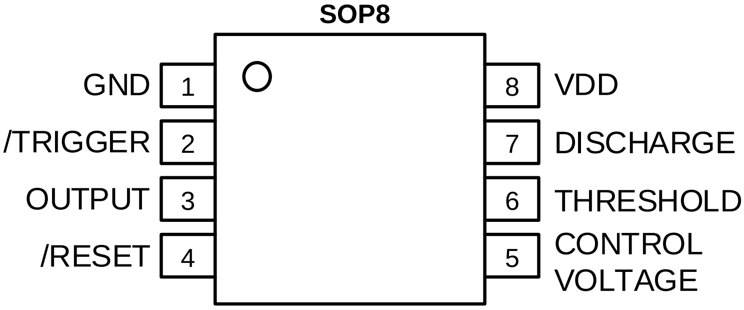


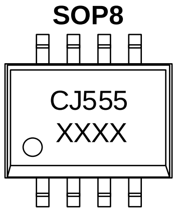
Figure 4-1 Pin configuration

4.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	GND	G	Ground
2	/TRIGGER	I	Trigger voltage input
3	OUTPUT	O	Voltage signal output
4	/RESET	I	Reset voltage input
5	CONTROL VOLTAGE	I	Control voltage input
6	THRESHOLD	I	Threshold voltage input
7	DISCHARGE	-	Discharge switch
8	VDD	P	Power

(1) I-Input, O-Output, P-Power, G-Ground

4.3 Marking Information



XXXX: Code, indicates weekly record information.

5 Specifications

5.1 Absolute Maximum Ratings

T_{amb}=25°C, All voltage referenced to GND, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Power supply voltage	-	-	+18	V
V_{IN}	Input voltage	Trigger, Control Voltage, Threshold, Reset	-0.3	V_{DD}+0.3	V
I_{OUT}	Output current	-	-	100	mA
T_{amb}	Operating temperature	-	-40	105	°C
T_{stg}	Storage temperature	-	-55	125	°C
P_D	Power dissipation	-	-	500	mW
T_L	Soldering temperature	10s	-	245	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

5.2 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Electrical Characteristics

T_{amb} =25°C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	Static supply current	V_{DD}=5V	-	40	200	μA
		V_{DD}=15V	-	60	300	μA
-	Monostable timing accuracy	R_A=10k, C=0.1μF, V_{DD}=5V	-	2	-	%
-	Drift with Supply	V_{DD}=5V to 15V	-	0.5	-	%/V
-	Astable timing accuracy	R_A=R_B=10k, C=0.1μF, V_{DD}=5V	-	2	-	%
-	Drift with Supply	V_{DD}=5V to 15V	-	0.5	-	%/V
V_{TH}	Threshold voltage	V_{DD}=5V	62	67	71	%V_{DD}
		V_{DD}=15V	62	67	71	%V_{DD}
V_{TRIG}	Trigger voltage	V_{DD}=5V	28	32	36	%V_{DD}
		V_{DD}=15V	28	32	36	%V_{DD}
I_{TH}	Threshold current	V_{DD}=15V	-	-	10	nA
I_{TRIG}	Trigger current	V_{DD}=15V	-	-	10	nA
V_{CV}	Control voltage	V_{DD}=15V	62	67	71	%V_{DD}
V_{RST}	Reset voltage	V_{DD}=2V to 15V	0.4	-	1.0	V
I_{RST}	Reset current	V_{DD}=15V	-	-	10	nA
I_{DIS}	Discharge leakage	V_{DD}=15V	-	-	10	nA
V_{OL}	Output voltage	V_{DD}=15V, I_{SINK}=20mA	-	0.4	1.0	V
		V_{DD}=5V, I_{SINK}=3.2mA	-	0.2	0.4	V
V_{OH}		V_{DD}=15V, I_{SOURSE}=0.8mA	14.3	14.6	-	V
		V_{DD}=5V, I_{SOURSE}=0.8mA	4.0	4.3	-	V
V_{DIS}	Discharge output voltage	V_{DD}=5V, I_{SINK}=15mA	-	0.2	0.4	V
V_{DD}	Supply voltage	Functional Operation	2.0	-	18.0	V
t_R	Output rise time	R_L=10M, C_L=10pF, V_{DD}=5V	-	75	-	ns
t_F	Output fall time	R_L=10M, C_L=10pF, V_{DD}=5V	-	75	-	ns
f_{MAX}	Oscillator frequency	V_{DD}=5V, R_A=470Ω, R_B=270Ω, C=200pF	-	1	-	MHz

6 Detailed Description

6.1 Overview

The CJ555 device is, in most instances, a direct replacement for the NE/SE555 device. However, it is possible to effect economies in the external component count using the CJ555. Because the bipolar 555 device produces large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The CJ555 device produces no such transients. See Figure 6-1.

The CJ555 produces supply current spikes of only 2-3mA instead of 300-400mA and supply decoupling is normally not necessary. Secondly, in most instances, the Control Voltage decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications, 2 capacitors can be saved using an CJ555.

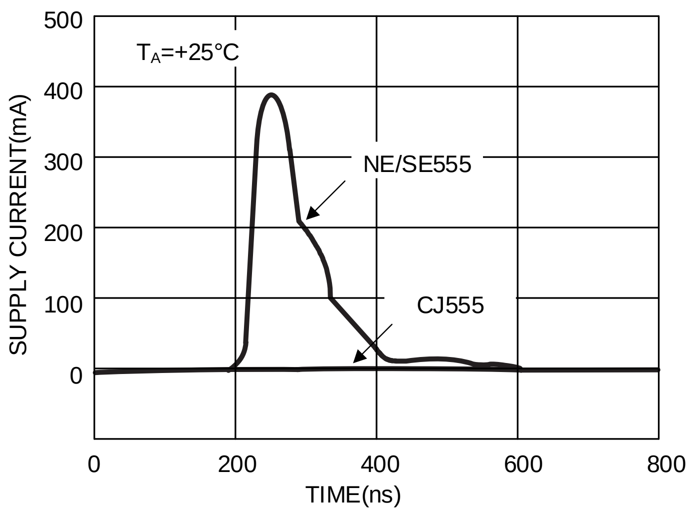


Figure 6-1 Supply current transient compared with a standard bipolar 555 during an output transition

6.2 Functional Block Diagram

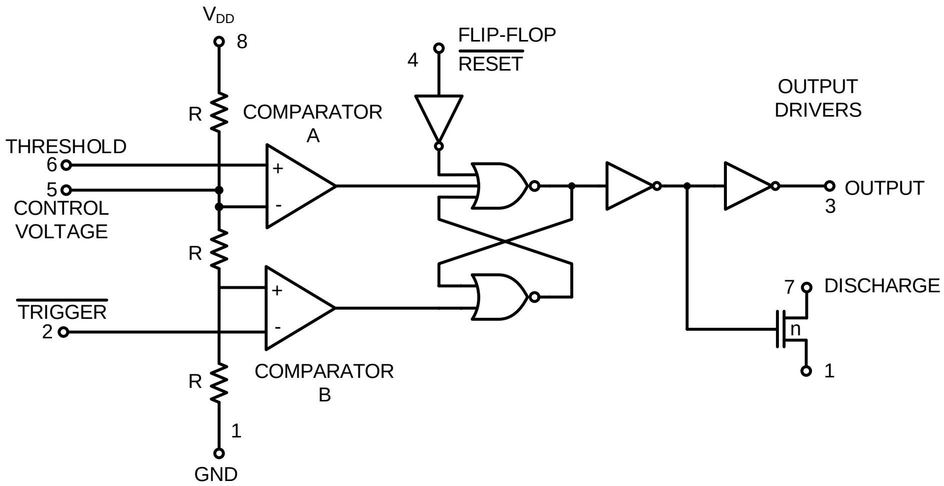


Figure 6-2 Functional diagram

Note:

Unused inputs should be connected to appropriate voltage from truth table.

6.3 Truth Table

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	RESET	OUTPUT	DISCHARGE SWITCH
Don't Care	Don't Care	Low	Low	On
>2/3V_{DD}	>1/3 V_{DD}	High	Low	On
<2/3 V_{DD}	>1/3 V_{DD}	High	Stable	Stable
Don't Care	<1/3 V_{DD}	High	High	Off

Note: Reset will dominate all other inputs: Trigger will dominate over Threshold.

6.4 Power Supply Considerations

Although the supply current consumed by the CJ555 device is very low, the total system supply can be high unless the timing components are high impedance. Therefore, high values for R and low values for C in Figure 6-3 and 6-4 are recommended

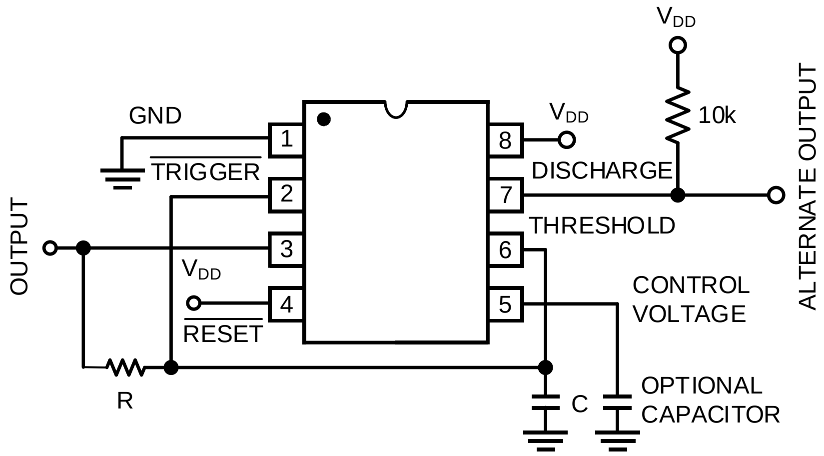


Figure 6-3 Astable operation

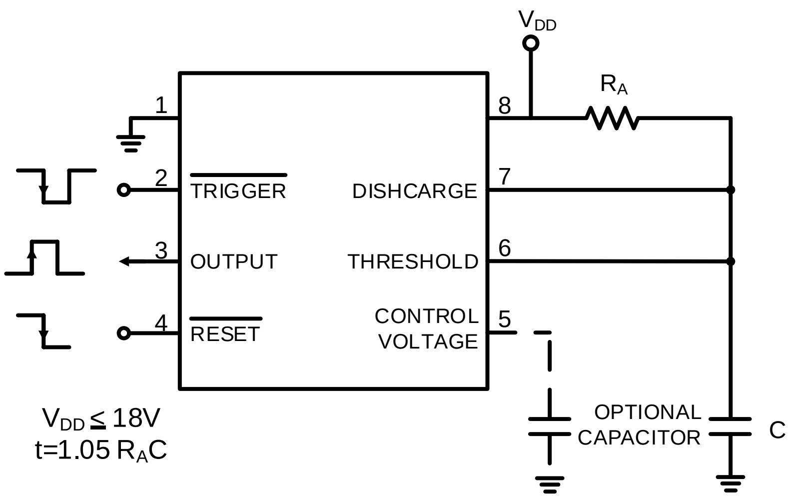


Figure 6-4 Monostable operation

6.5 Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more, the CJ555 will drive at least 2 standard TTL loads.

6.6 Astable Operation

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 6-3. The output swings from rail-to-rail, and is a true 50% duty cycle square wave. Trip points and output swings are symmetrical. Less than a 1% frequency variation is observed over a voltage range of +5V to +15V.

$$F = 1/1.4RC \tag{1}$$

The timer can also be connected as shown in Figure 6-5. In this circuit, the frequency is as shown by Equation 2:

$$F = 1.44/(R_A + 2R_B)C \tag{2}$$

The duty cycle is controlled by the values of R_A and R_B, by Equation 3:

$$D = (R_A + R_B)/(R_A + 2R_B) \tag{3}$$

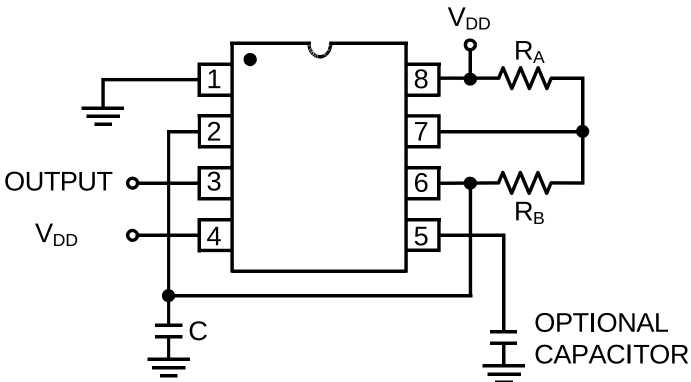


Figure 6-5 Alternate astable configuration

6.7 Monostable Operation

In this mode of operation, the timer functions as a one-shot. Initially, the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative pulse to Pin 2,Trigger, the internal flip-flop is set which releases the low impedance on Discharge; the external capacitor charges and drives the Output High. The voltage across the capacitor increases exponentially with a time constant $t = R_A C$. When the voltage across the capacitor equals 2/3 V_{DD}, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. /Trigger must return to a high state before the OUTPUT can return to a low state.

6.8 Control Voltage

The Control Voltage terminal permits the two trip voltages for the Threshold and /Trigger internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode, or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the Control Voltage pin.

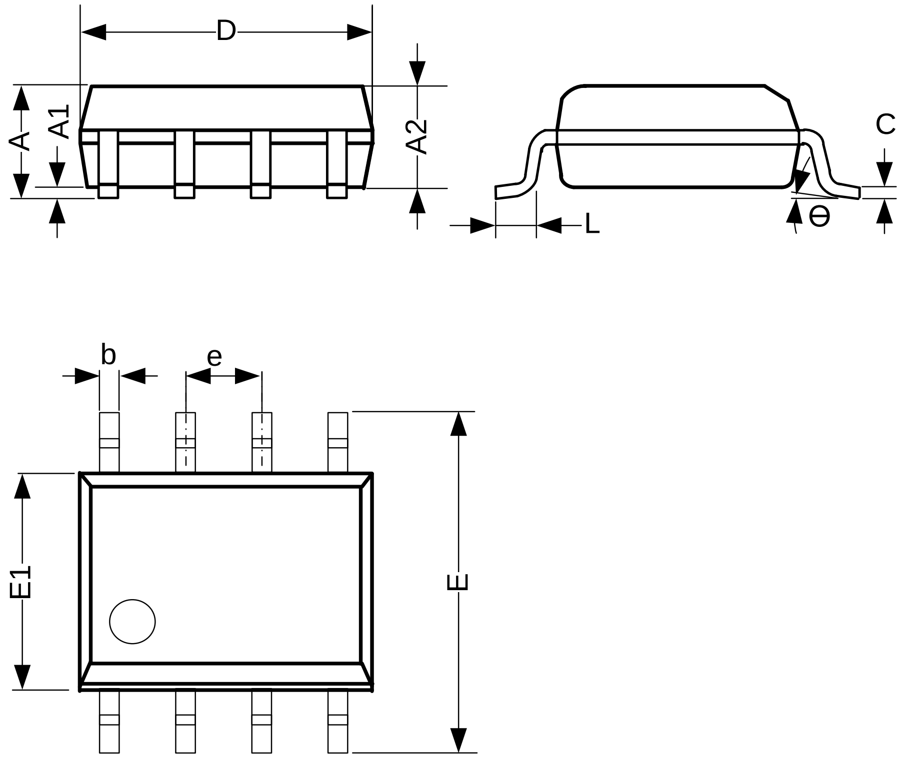
6.9 /RESET

The /Reset terminal is designed to have essentially the same trip voltage as the standard bipolar 555, i.e., 0.6 to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the /Reset function is, however, much improved over the standard bipolar 555 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the Output and Discharge pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

7 Mechanical Information

7.1 SOP8 Mechanical Information

7.1.1 SOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.35	-	1.55
b	0.33	-	0.51
c	0.17	-	0.25
D	4.78	-	5.00
E	5.80	-	6.30
E1	3.80	-	4.00
e	1.27 BSC		
L	0.40	-	1.27
Θ	0°	-	8°
Unit: mm			

8 Notes and Revision History

8.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

8.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

8.3 Revision History

April, 2026: rev -1.1, Change Orderable Information.

DISCLAIMER

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