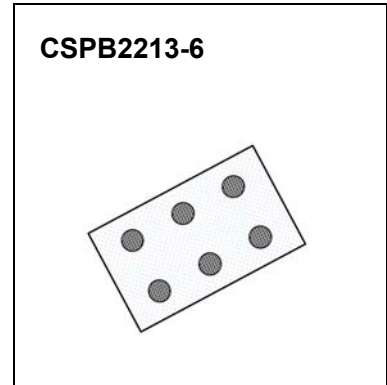




**CSP Enhancement Mode Power MOSFET**

**CJ6207SP Dual N-Channel MOSFET**

V <sub>SSS</sub>	R <sub>SS(on)</sub> TYP	I <sub>S</sub>
12V	4.0mΩ@4.5V	8.5A
	4.2mΩ@3.8V	
	4.9mΩ@3.1V	
	6.8mΩ@2.5V	



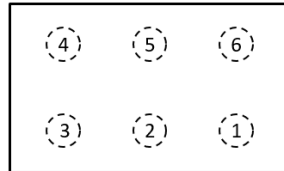
**DESCRIPTION**

The CJ6207SP uses advanced trench technology to provide excellent R<sub>SS(ON)</sub>, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V V<sub>GS(MAX)</sub> rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

**Marking and pin assignment**



Top View



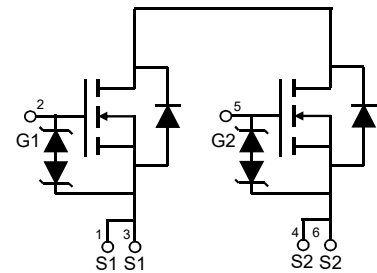
Bottom View

Marking:

- 1. 6207: Product Code
- 2. YYMMX: Date Code
- 3. Solid dot: Pin 1

- 1,3. Source1      2. Gate1
- 4,6. Source2      5. Gate2

**Equivalent Circuit**



**ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V <sub>SSS</sub>	12	V
Gate-Source Voltage	V <sub>GSS</sub>	±8	V
Source Current(DC)	I <sub>S</sub> <sup>①</sup>	8.5	A
Source Current (Pulsed)	I <sub>SP</sub> <sup>①</sup>	85	A
Total Power Dissipation	P <sub>T</sub> <sup>①</sup>	1.39	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55 To 150	°C

# MOSFET ELECTRICAL CHARACTERISTICS

$T_a=25\text{ }^\circ\text{C}$  unless otherwise specified

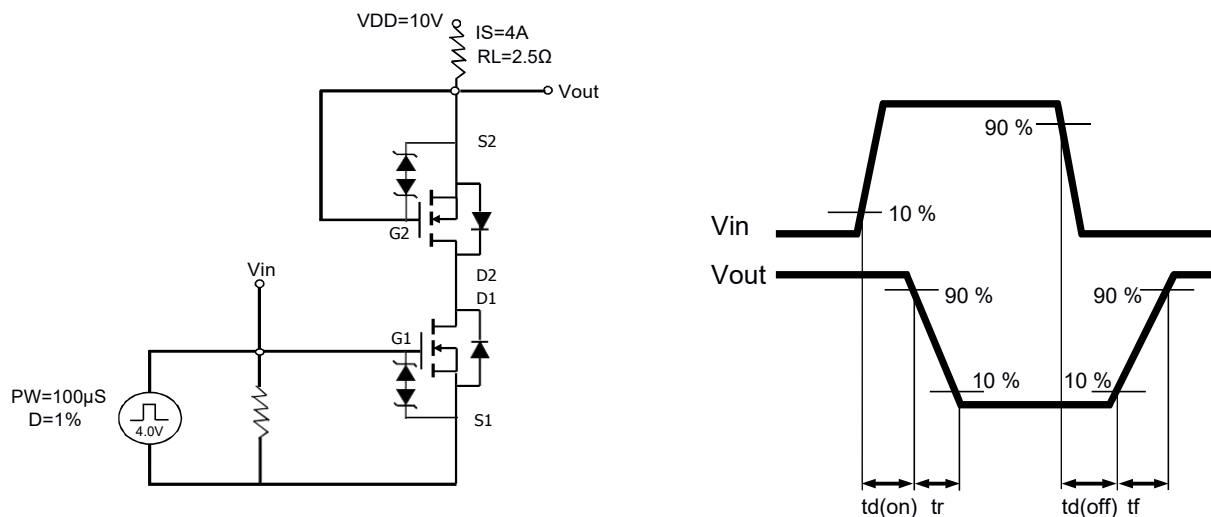
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
Source to Source Breakdown Voltage	$BV_{SSS}$	$I_S=1\text{mA}, V_{GS}=0\text{V}$	12			V
Zero-Gate Voltage Source Current	$I_{SSS}$	$V_{SS}=10\text{V}, V_{GS}=0\text{V}$			1.0	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$			$\pm 10$	$\mu\text{A}$
Gate to Source Threshold Voltage	$V_{TH}$	$V_{SS}=10\text{V}, I_S=1.0\text{ mA}$	0.4	0.95	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=4.5\text{V}, I_S=5\text{A}$	2.6	4.0	6.4	$\text{m}\Omega$
		$V_{GS}=3.8\text{V}, I_S=5\text{A}$	2.8	4.2	6.7	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=5\text{A}$	3.2	4.9	9.7	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=5\text{A}$	3.8	6.8	15.2	$\text{m}\Omega$
Input Capacitance	$C_{iss}$			1290		$\text{pF}$
Output Capacitance	$C_{oss}$	$V_{SS}=10\text{V}, V_{GS}=0\text{V}, f=100\text{kHz}$		343		$\text{pF}$
Reverse Transfer Capacitance	$C_{rss}$			159		$\text{pF}$
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10\text{V}, R_L=2.5\Omega, V_{GS}=4.0\text{V}$		0.5		$\mu\text{s}$
Turn-on Rise Time	$t_r$			1.3		$\mu\text{s}$
Turn-off Delay Time	$t_{d(off)}$			3.3		$\mu\text{s}$
Turn-off Fall Time	$t_f$			3.2		$\mu\text{s}$
Total Gate Charge	$Q_g$	$V_{SS}=10\text{V}, I_S=4\text{A}, V_{GS}=4.5\text{V}$		32		$\text{nC}$
Gate1-source1 charge	$Q_{g1s1}$			8.7		$\text{nC}$
Gate1-source2 charge	$Q_{g1s2}$			6.0		$\text{nC}$
Diode Forward Voltage	$V_{F(S-S)}^{(4)}$	$V_{GS}=0\text{V}, I_S=10\text{A}$			1.5	V

Notes: 1. Mounted on FR4 board (25.4mm×25.4mm×1.0mm) using the minimum recommended pad size (36um Copper).

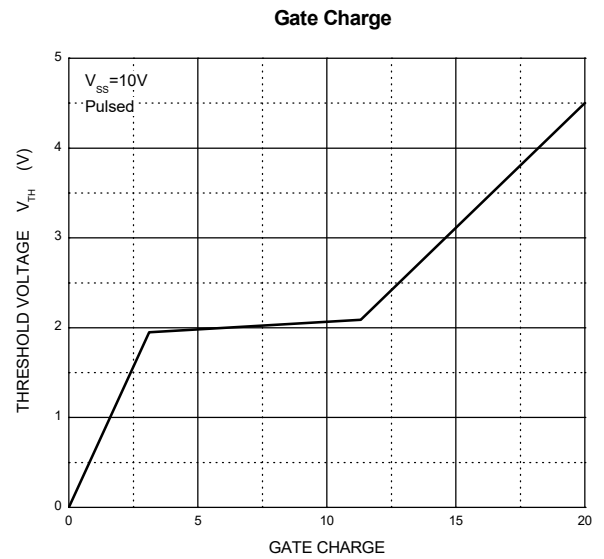
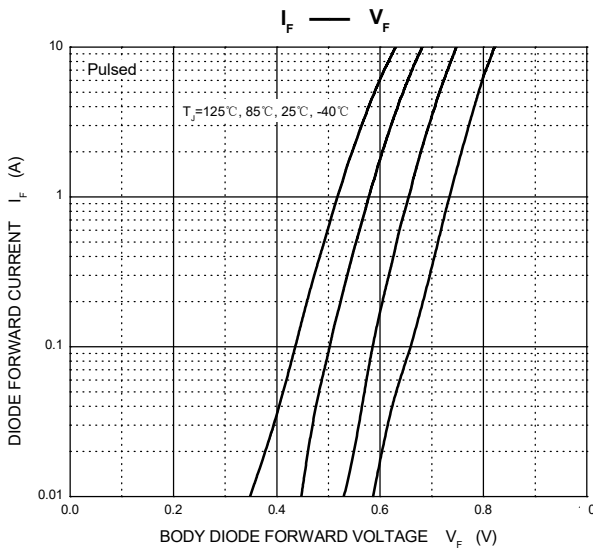
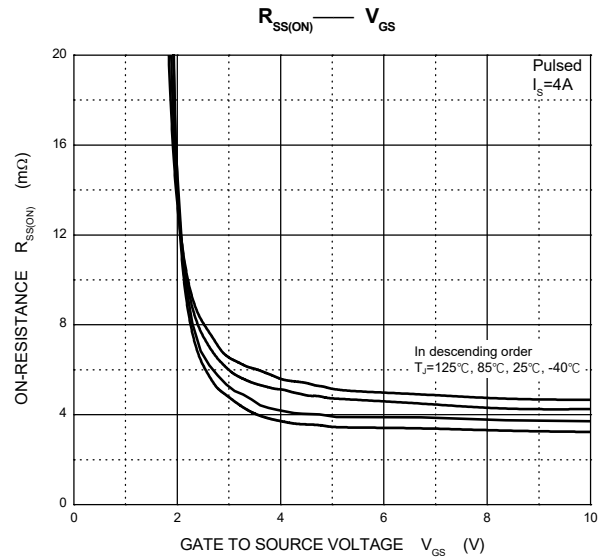
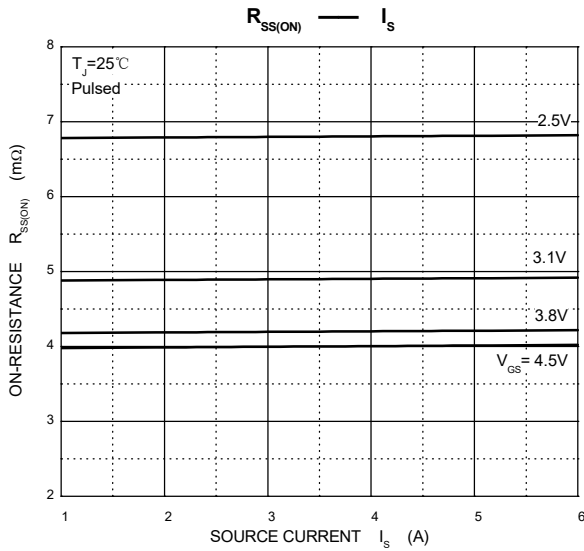
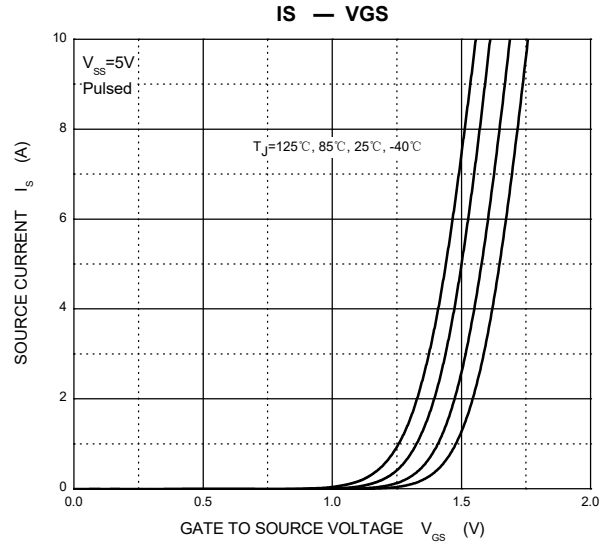
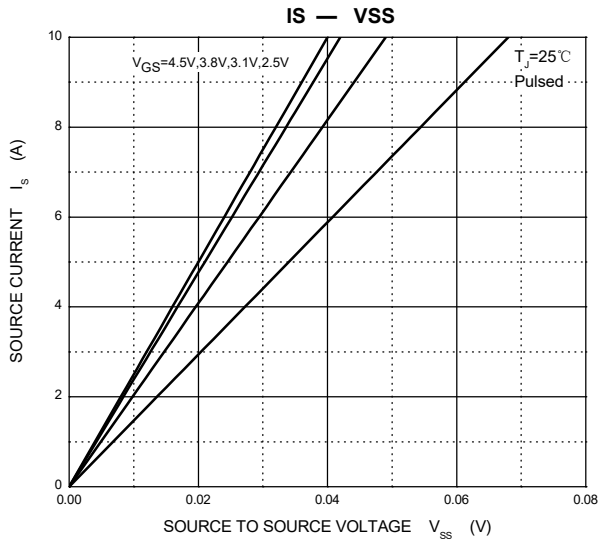
2.  $t = 10\text{ ms}$ , Duty Cycle = 1%.

3. When FET1 is measured, G2 and S2 are short-circuited.

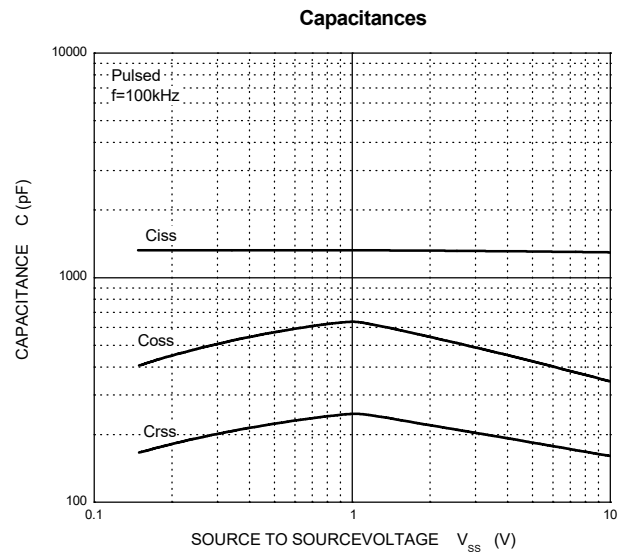
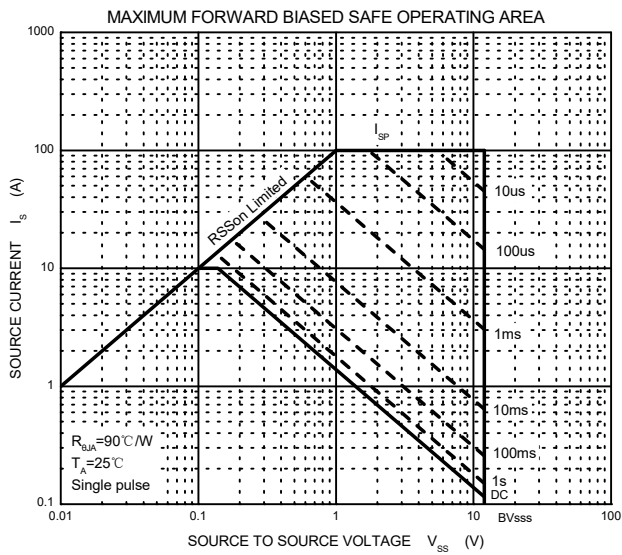
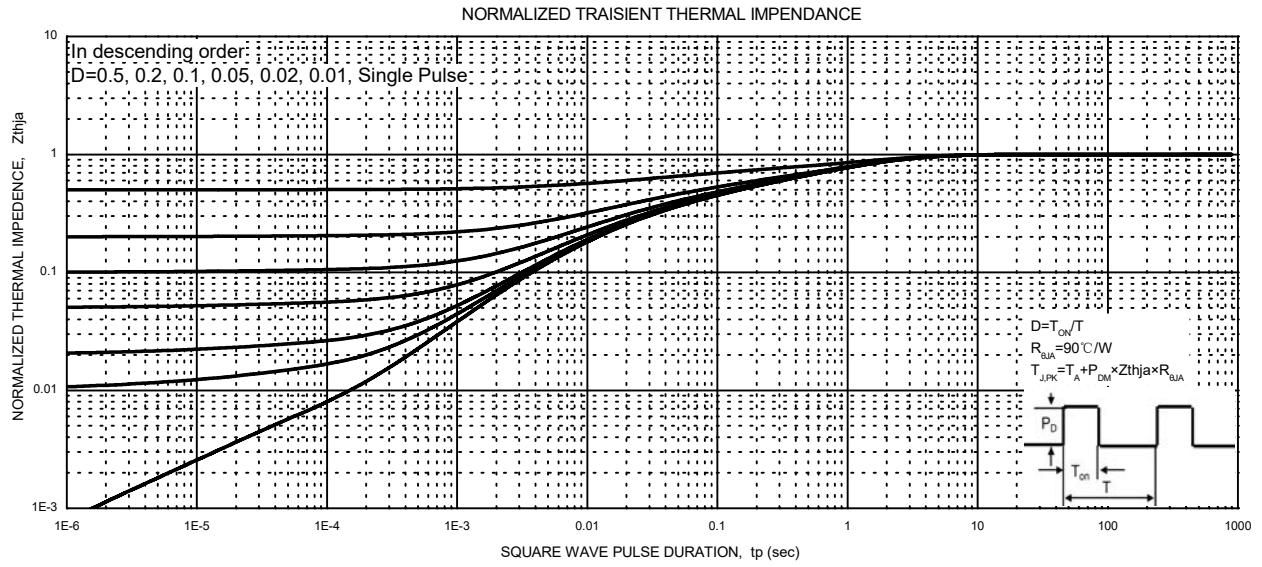
4. When FET1 is measured, FET2 is biased with  $V_{GS2}=4.5\text{V}$ .



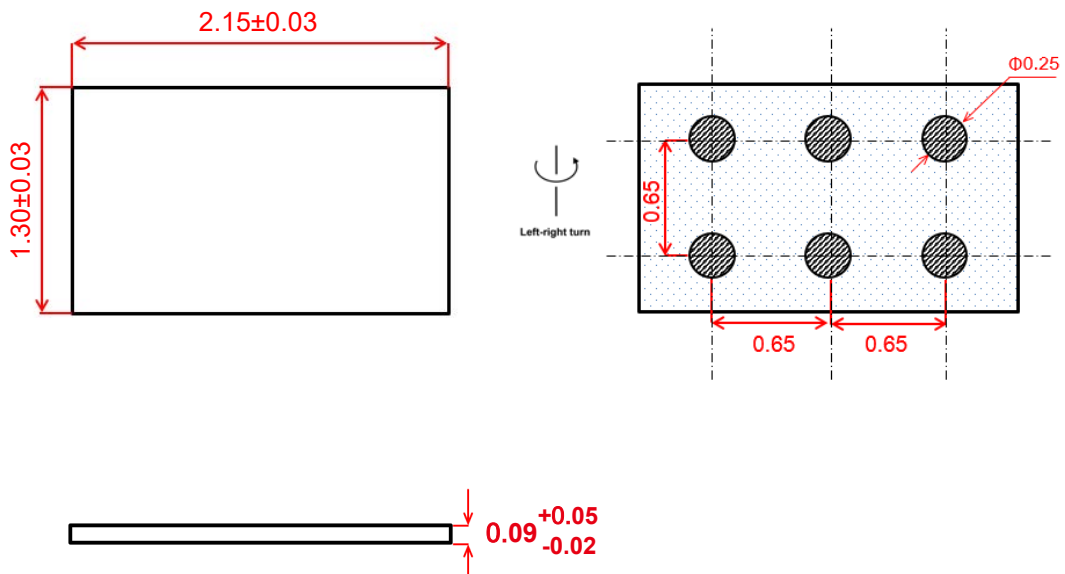
# Typical Characteristics



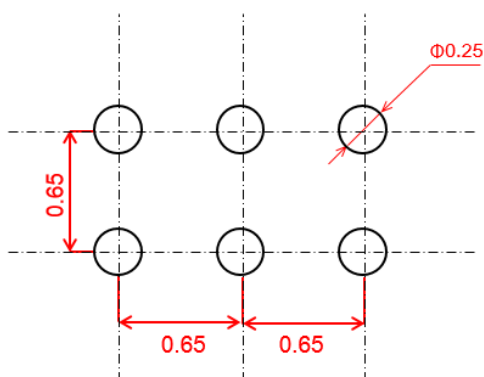
# Typical Characteristics



**CSPB2213-6 Package Outline Dimensions(Unit:mm)**



**CSPB2213-6 Suggested Pad Layout (Unit:mm)**



- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.050$  mm.
  3. The pad layout is for reference purposes only.

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