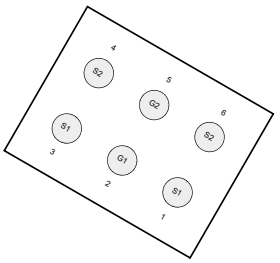
JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

CSP Enhancement Mode Power MOSFET

CJ6617SP Dual N-Channel MOSFET

V_{SSS}	$R_{SS(on)}$TYP	I_S
20V	4.9mΩ@4.5V	12A
	5.1mΩ@4.0V	
	5.2mΩ@3.8V	
	5.7mΩ@3.1V	
	6.6mΩ@2.5V	

CSPB2217-6

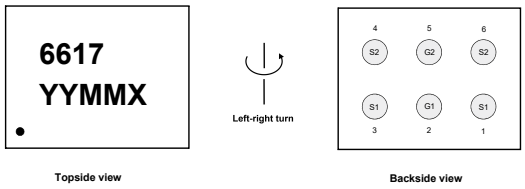


DESCRIPTION

The CJ6617SP uses advanced trench technology to provide excellent RSS(ON) , low gate charge and operation with gate voltages as low as 2.5V while retaining a 12V $V_{GS(MAX)}$ rating. It is ESD protected.

This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment

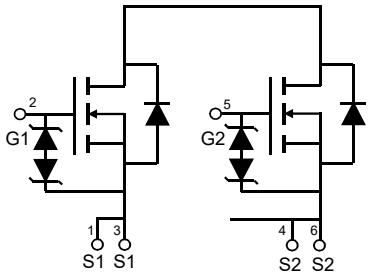


Marking:

1. 6617: Product Code
2. YYMMX: Date Code
3. Solid dot: Pin 1

1,3	Source1
4, 6	Source2
2	Gate1
5	Gate2

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V_{SSS}	20	V
Gate-Source Voltage	V_{GSS}	±12	V
Source Current(DC)	I_S ①	12	A
Source Current (Pulsed)	I_{SP} ①②	120	A
Total Power Dissipation	P_T ①	2.0	W
Channel Temperature	T_{ch}	150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

MOSFET ELECTRICAL CHARACTERISTICS

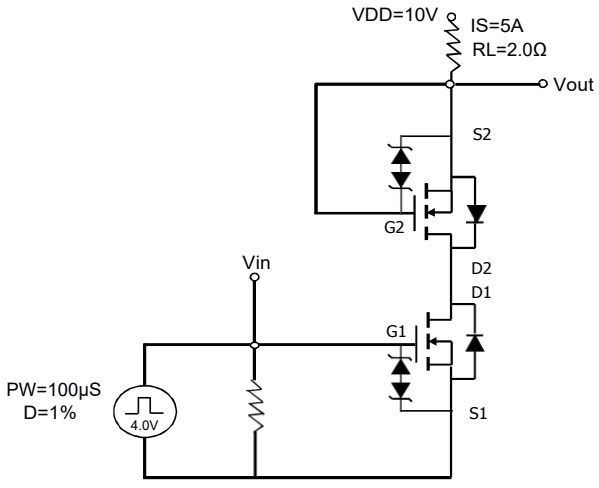
T_a=25 ℃ unless otherwise specified

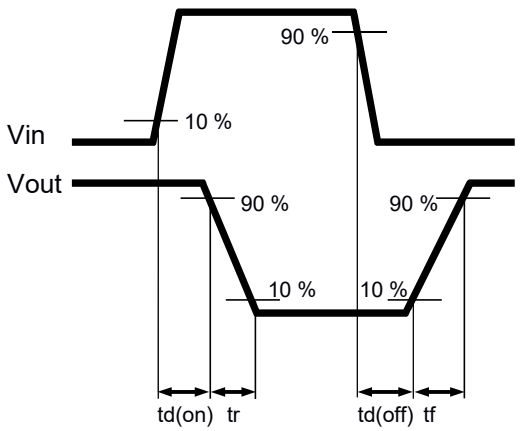
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	I_S=1mA ,V_{GS}=0V	20			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=16V,V_{GS}=0V			100	nA
Gate to Source Leakage Current	I_{GSS}	V_{SS}=0V,V_{GS}= ±10V			±10	μA
		V_{SS}=0V,V_{GS}= ±5V			±1.0	
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{SS}=V_{GS}, I_S=250μA	0.4	0.85	1.2	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS}=4.5V,I_S=3A	2.9	4.9	6.8	mΩ
		V_{GS}=4.0V,I_S=3A	3.0	5.1	7.1	mΩ
		V_{GS}=3.8V,I_S=3A	3.1	5.2	7.3	mΩ
		V_{GS}=3.1V,I_S=3A	3.4	5.7	8.0	mΩ
		V_{GS}=2.5V,I_S=3A	4.0	6.6	9.2	mΩ
Input Capacitance	Ciss	V_{SS}=10V, V_{GS}=0V,f=1kHz		2609		pF
Output Capacitance	Coss			362		pF
Reverse Transfer Capacitance	Crss			295		pF
Turn-on Delay Time	$t_{d(on)}$ ③	V_{DD}=10V,I_S=5A, V_{GS}=4.0V		0.9		μS
Turn-on Rise Time	t_r ③			2.6		μS
Turn-off Delay Time	$t_{d(off)}$ ③			5.7		μS
Turn-off Fall Time	t_f ③			3.9		μS
Total Gate Charge	Q_g ③	V_{SS}=10V,I_S=8A,V_{GS}=6.0V		34.7		nC
Gate1-source1 charge	Q_{g1s1} ③			5.9		nC
Gate1-source2 charge	Q_{g1s2} ③			11.8		nC
Diode Forward Voltage	$V_{F(S-S)}$	V_{GS}=0V,I_S=1A			1.0	V

Notes: 1.Mounted on FR4 board (25.4mm×25.4mm×t1.0mm) using the minimum recommended pad size (36um Copper).

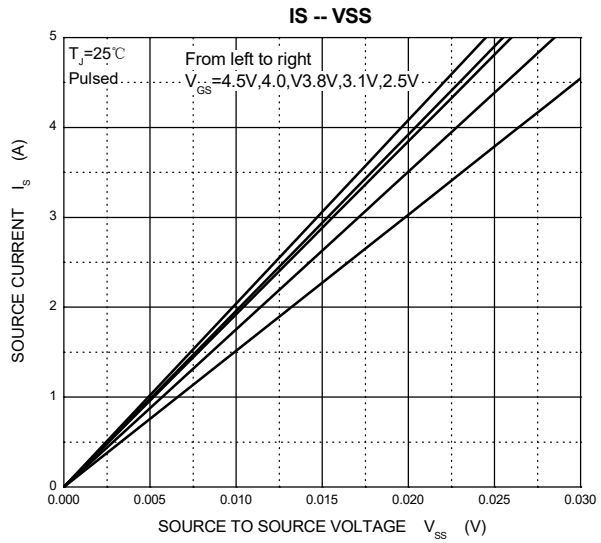
2.t = 10 ms , Duty Cycle = 1 %.

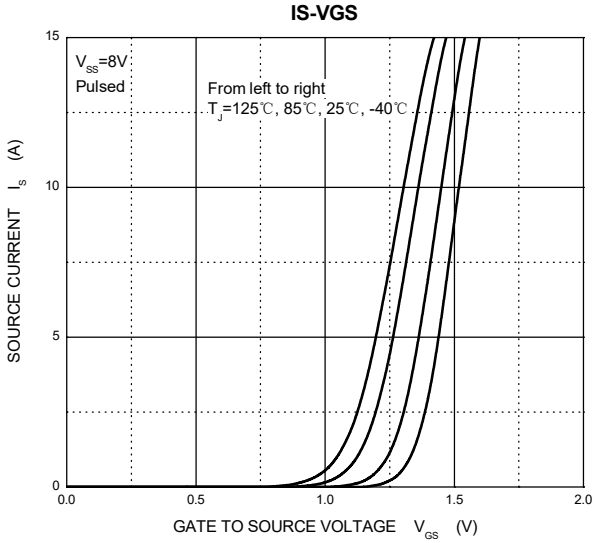
3.When FET1 is measured,G2 and S2 are short-circuited.

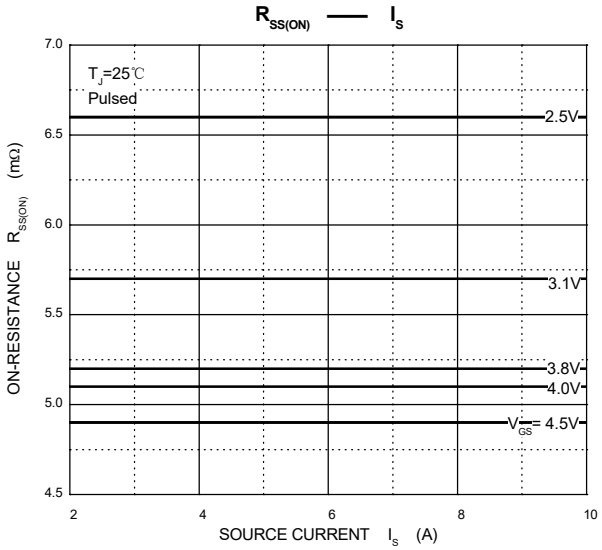


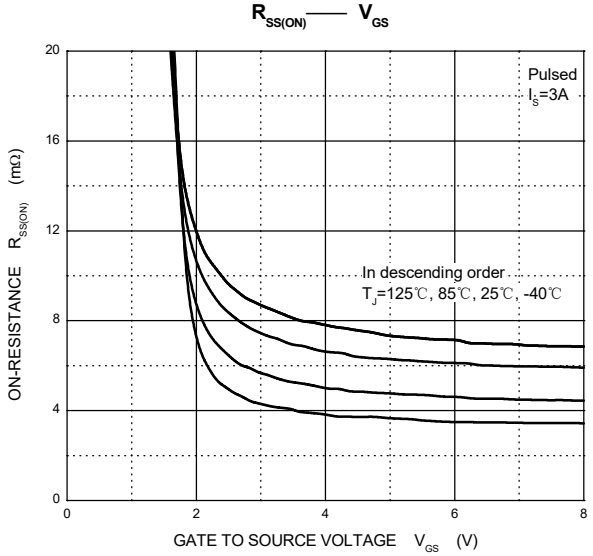


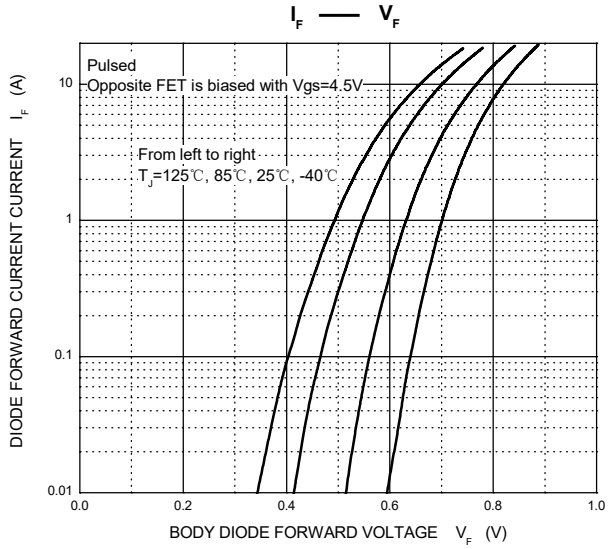
Typical Characteristics

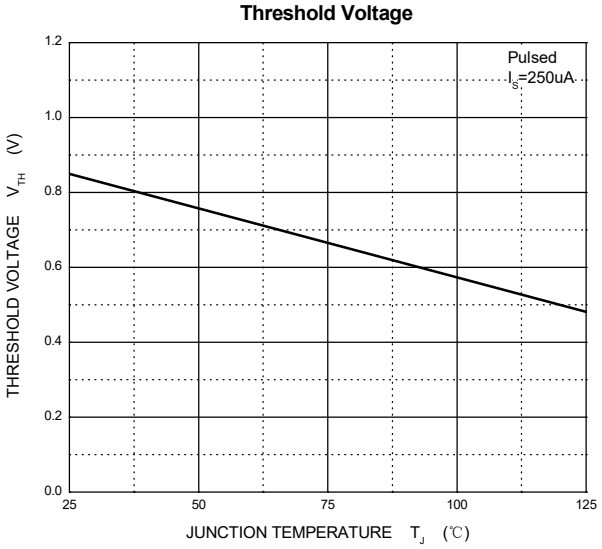






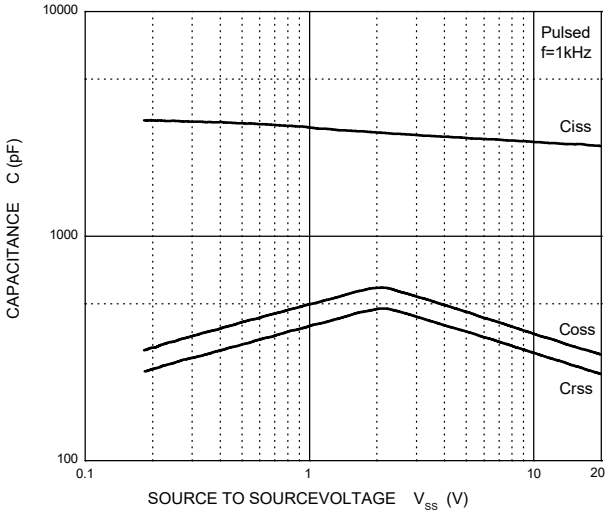




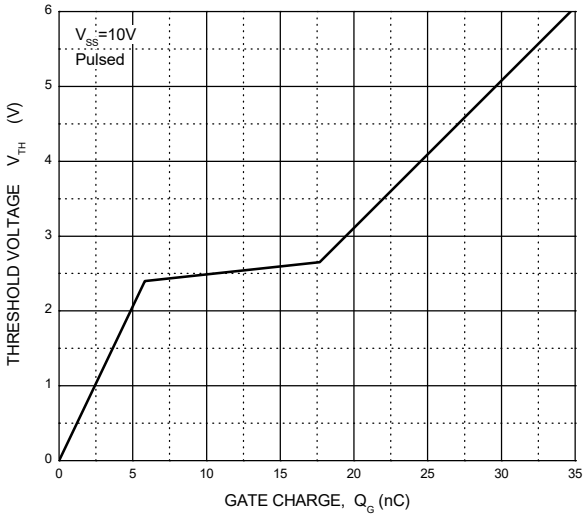


Typical Characteristics

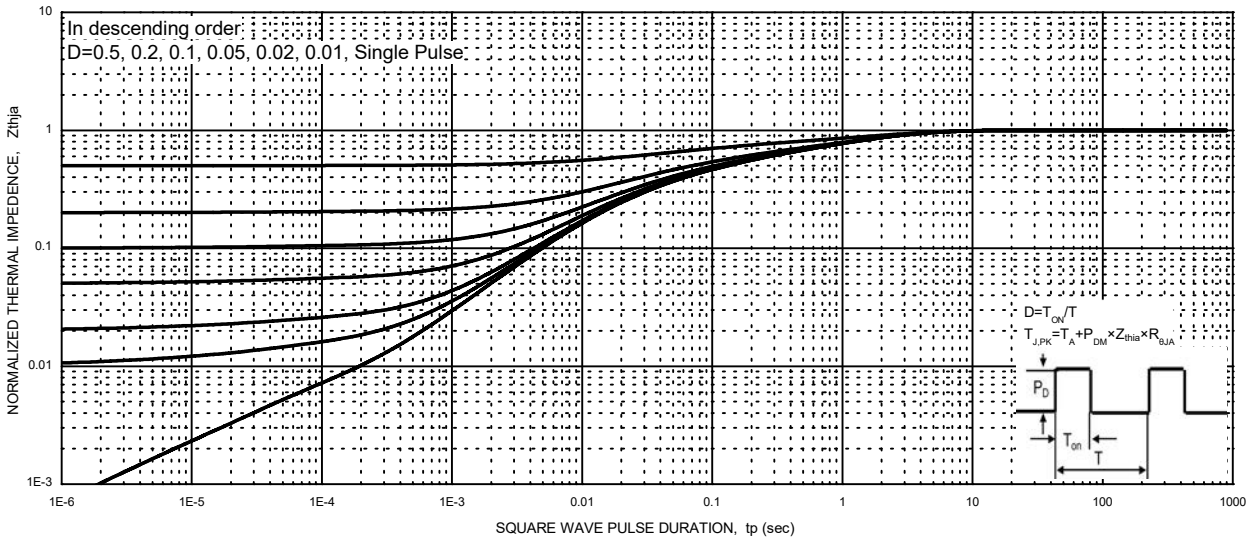
Capacitances



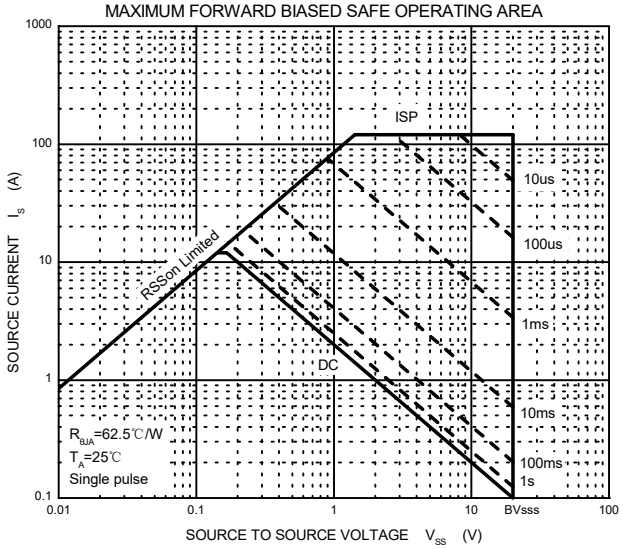
Gate Charge



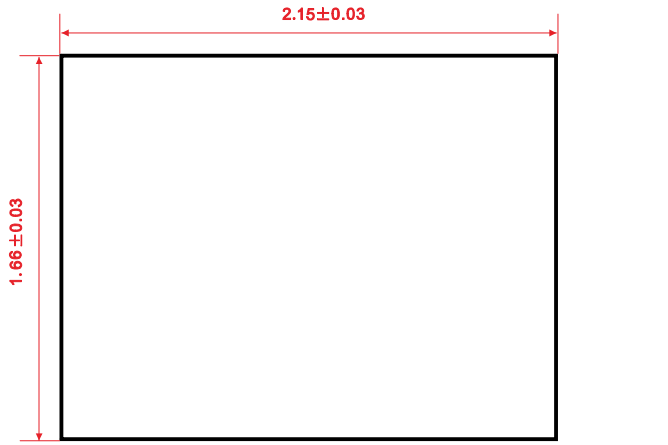
NORMALIZED TRAISIENT THERMAL IMPENDANCE

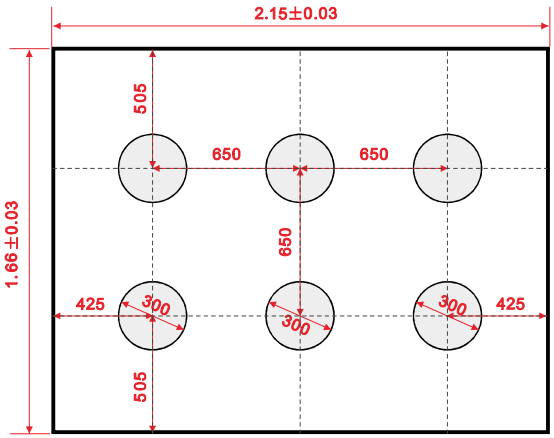


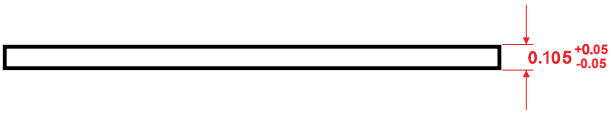
MAXIMUM FORWARD BIASED SAFE OPERATING AREA



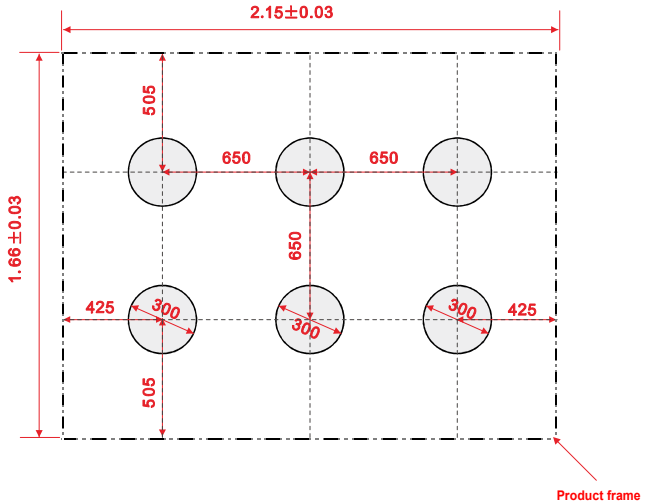
CSPB2217-6 Package Outline Dimensions(Unit:mm)





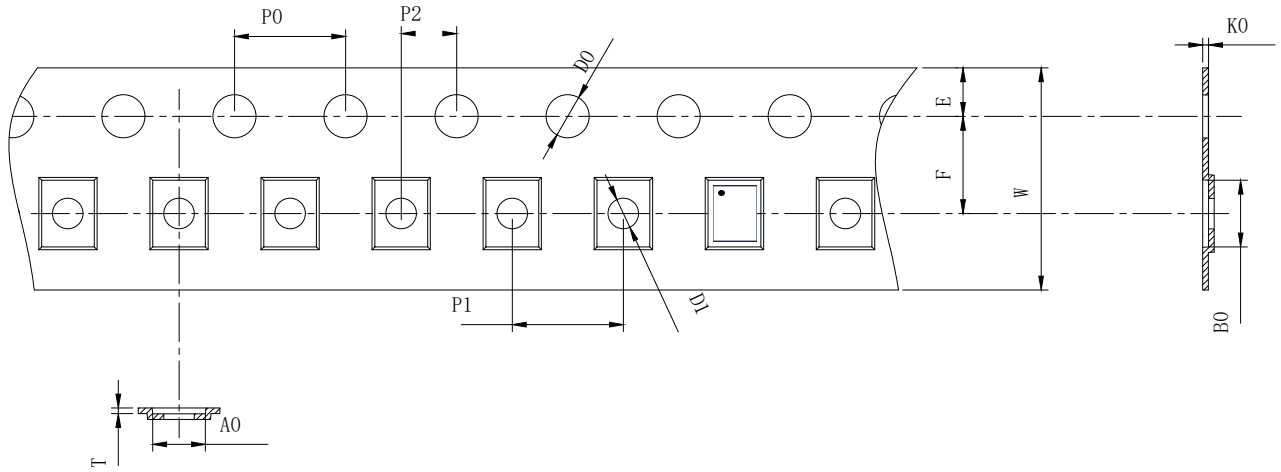


CSPB2217-6 Suggested Pad Layout (Unit:mm)

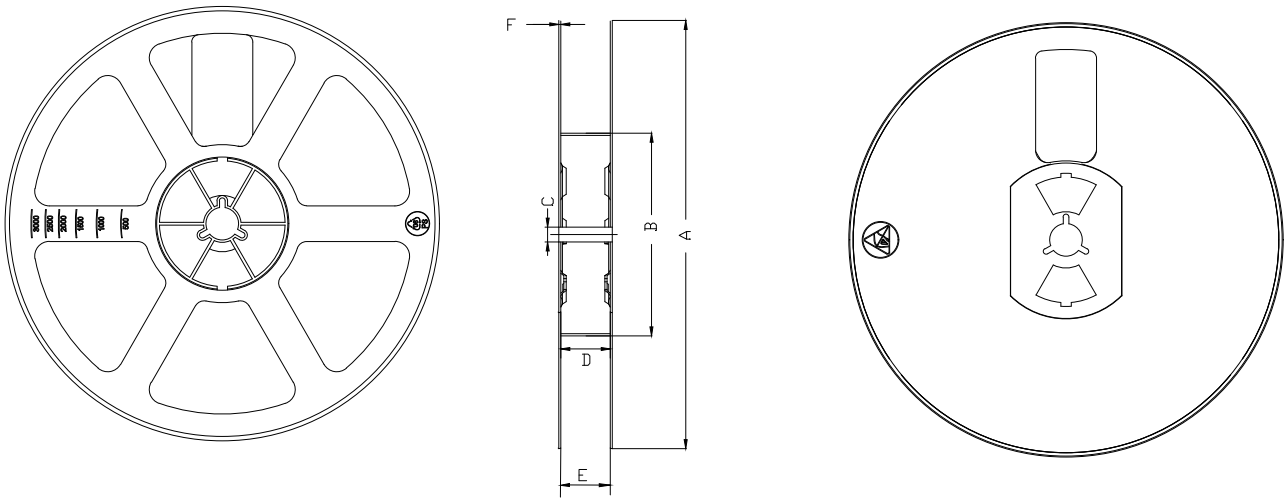


Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

Tape and Reel



产品尺寸规格 (UNIT:mm)						
规格	A0	B0	K0	P0	P1	P2
尺寸	1.90±0.05	2.40±0.05	0.21±0.05	4.0±0.1	4.0±0.1	2.0±0.05
规格	T	E	F	D0	D1	W
尺寸	0.2±0.05	1.75±0.1	3.5±0.05	1.55±0.1	1.10±0.1	$8.0^{+0.3}_{-0.1}$



SIZE	8MM
A	178±2.0
B	55±1.0
C	$13.0^{+0.35}_{-0.15}$
D	$8.4^{+2.5}_{-0.4}$
E	$8.65^{+4.7}_{-0.65}$
F	1.5±0.5

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