Single 2-input AND Gate (Open Drain)

CJ74AHC1G09 Logic

1 Introduction

The CJ74AHC1G09 is a high-speed Si-gate CMOS device.

The CJ74AHC1G09 provides the 2-input AND function with open-drain output.

The output of the CJ74AHC1G09 is an open drain and can be connected to other open-drain outputs to implement active-LOW, wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH level.

2 Available Packages

PART NUMBER	PACKAGE
CJ74AHC1G09	SOT-23-5L
	SOT-353

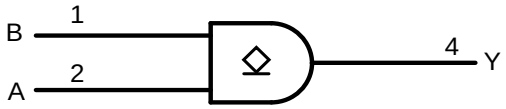
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 2V to 5.5V
- Low power consumption
- Specified from -40°C to +125°C

4 Applications

- Combining power good signals
- Enable digital signals



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74AHC1G09M5N	SOT-23-5L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active
CJ74AHC1G09R5N	SOT-353	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

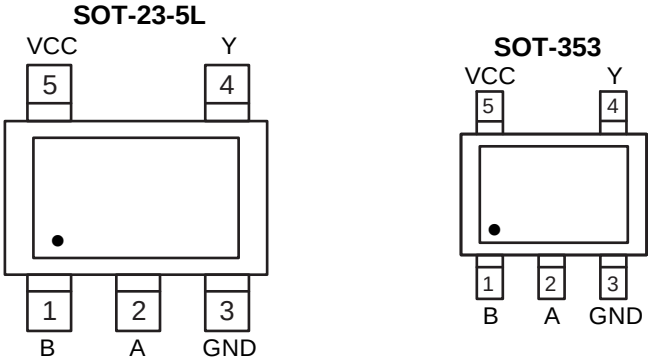


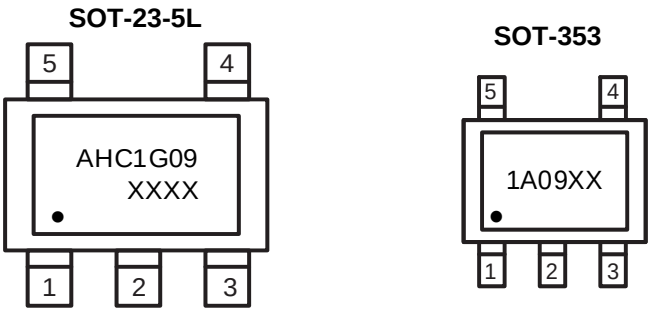
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	B	I	Data input B
2	A	I	Data input A
3	GND	G	Ground (0V)
4	Y	O	Data output Y
5	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX or XX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-	-0.5	+7.0	V
V_I	Input voltage	-	-0.5	+7.0	V
I_{IK}	Input clamping current	V_I < -0.5V	-20	-	mA
I_{OK}	Output clamping current	V_O < -0.5V	-	±20	mA
V_O	Output voltage	Active mode	-0.5	+7.0	V
		High-impedance mode	-0.5	+7.0	V
I_O	Output current	V_O > -0.5V	-	25	mA
I_{CC}	Supply current	-	-	75	mA
I_{GND}	Ground current	-	-75	-	mA
T_{stg}	Storage temperature	-	-65	+150	°C
P_{tot}	Total power dissipation	-	-	250	mW
T_L	Soldering temperature	10s	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	-	2.0	5.0	5.5	V
V_I	Input voltage	-	0	-	5.5	V
V_O	Output voltage	Active mode	0	-	V_{CC}	V
		High-impedance mode	0	-	6.0	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
Δt/ΔV	Input transition rise and fall rate	V_{CC}=3.0V to 3.6V	-	-	100	ns/V
		V_{CC}=4.5V to 5.5V	-	-	20	ns/V

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb} =25°C, voltages are referenced to GND (ground=0V), unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=3.0V		2.1	-	-	V
		V_{CC}=5.5V		3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=3.0V		-	-	0.9	V
		V_{CC}=5.5V		-	-	1.65	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_O=50uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=50uA; V_{CC}=3.0V	-	0	0.1	V
			I_O=50uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=4mA; V_{CC}=3.0V	-	-	0.36	V
			I_O=8mA; V_{CC}=4.5V	-	-	0.36	V
I_I	Input leakage current	V_I=5.5V or GND; V_{CC}=0V to 5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_O= V_{CC} or GND; V_{CC}= 5.5 V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}= 5.5V		-	-	1.0	uA
C_I	Input capacitance	-		-	1.5	10	pF

7.4.2 DC Characteristics 2

T_{amb} =-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=3.0V		2.1	-	-	V
		V_{CC}=5.5V		3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=3.0V		-	-	0.9	V
		V_{CC}=5.5V		-	-	1.65	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_O=50uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=50uA; V_{CC}=3.0V	-	-	0.1	V
			I_O=50uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=4mA; V_{CC}=3.0V	-	-	0.44	V
			I_O=8mA; V_{CC}=4.5V	-	-	0.44	V
I_I	Input leakage current	V_I=5.5V or GND; V_{CC}=0V to 5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_O= V_{CC} or GND; V_{CC}= 5.5 V		-	-	±2.5	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}= 5.5V		-	-	10	uA
C_I	Input capacitance	-		-	-	10	pF

7.4.3 DC Characteristics 3

T_{amb} =-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=3.0V		2.1	-	-	V
		V_{CC}=5.5V		3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=3.0V		-	-	0.9	V
		V_{CC}=5.5V		-	-	1.65	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=50uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=50uA; V_{CC}=3.0V	-	-	0.1	V
			I_O=50uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=4mA; V_{CC}=3.0V	-	-	0.55	V
			I_O=8mA; V_{CC}=4.5V	-	-	0.55	V
I_I	Input leakage current	V_I=5.5V or GND; V_{CC}=0V to 5.5V		-	-	±2.0	uA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O= V_{CC} or GND; V_{CC}= 5.5 V		-	-	±10.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}= 5.5V		-	-	20	uA
C_I	Input capacitance	-		-	-	10	pF

7.4.4 AC Characteristics 1

T_{amb} =25°C, voltages are referenced to GND (ground=0V), unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{pd}	A, B to Y propagation delay	See Figure 8-5	C_L=15Pf V_{CC}=3.0V to 3.6V	-	4.6	7.5	ns
			C_L=50pF V_{CC}=3.0V to 3.6V	-	6.5	11.0	ns
			C_L=15pF V_{CC}=4.5V to 5.5V	-	3.2	5.5	ns
			C_L=50pF V_{CC}=4.5V to 5.5V	-	4.6	7.5	ns
C_{PD}	Power dissipation capacitance	C_L=50pF; f_i=1MHz; V_I= GND to V_{CC}		-	5	-	pF

Note:

(1) t_{pd} is the same as t_{PZL} and t_{PLZ}.

(2) Typical values are measured at V_{CC}=3.3V or 5V.

(3) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}xV_{CC}^2xf_ixN)+\sum(C_LxV_{CC}^2xf_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_LxV_{CC}^2xf_o)$= dissipation due to the output if the combination of the pull up voltage and resistance results in V_{CC} at the output.

7.4.5 AC Characteristics 2

T_{amb} =-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{pd}	A, B to Y propagation delay	See Figure 8-5	C_L=15Pf V_{CC}=3.0V to 3.6V	1.0	-	8.5	ns
			C_L=50pF V_{CC}=3.0V to 3.6V	1.5	-	12.0	ns
			C_L=15pF V_{CC}=4.5V to 5.5V	1.0	-	6.5	ns
			C_L=50pF V_{CC}=4.5V to 5.5V	1.5	-	8.0	ns

Note:

(1) t_{pd} is the same as t_{PZL} and t_{PLZ}.

(2) Typical values are measured at V_{CC}=3.3V or 5V.

7.4.6 AC Characteristics 3

T_{amb} =-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{pd}	A, B to Y propagation delay	See Figure 8-5	C_L=15Pf V_{CC}=3.0V to 3.6V	1.0	-	9.0	ns
			C_L=50pF V_{CC}=3.0V to 3.6V	1.5	-	12.5	ns
			C_L=15pF V_{CC}=4.5V to 5.5V	1.0	-	7.0	ns
			C_L=50pF V_{CC}=4.5V to 5.5V	1.5	-	8.5	ns

Note:

(1) t_{pd} is the same as t_{PZL} and t_{PLZ}.

(2) Typical values are measured at V_{CC}=3.3V or 5V.

8 Detailed Description

8.1 Overview

The CJ74AHC1G09 is a high-speed Si-gate CMOS device.

The CJ74AHC1G09 provides the 2-input AND function with open-drain output.

The output of the CJ74AHC1G09 is an open drain and can be connected to other open-drain outputs to implement active-LOW, wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH level.

8.2 Functional Block Diagram

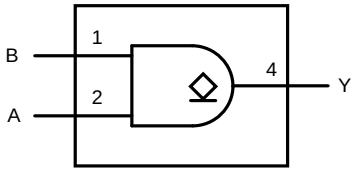


Figure 8-1 Logic symbol

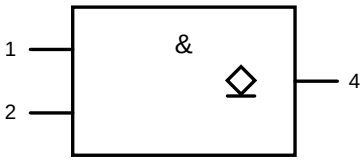


Figure 8-2 IEC logic symbol

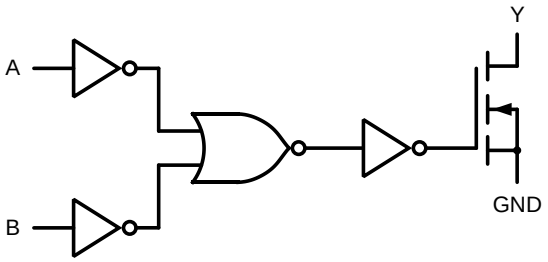


Figure 8-3 Logic diagram

8.3 Function Table(1)

INPUT		OUTPUT
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	Z

(1) H=HIGH voltage level; L=LOW voltage level; X=Don't care; Z=high-impedance OFF-state.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

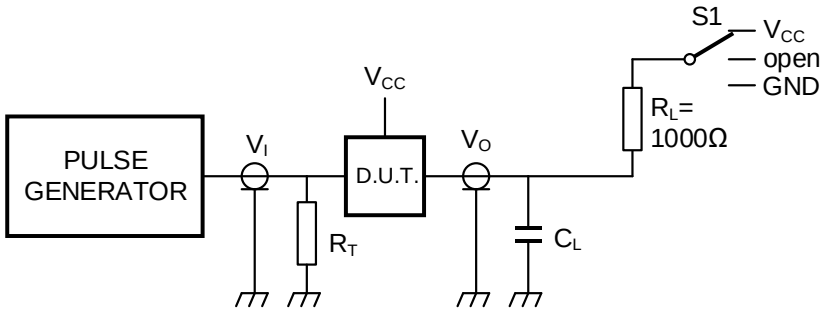


Figure 8-4 Load circuit for switching times

Definitions for test circuit:

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

8.4.2 AC Testing Waveforms

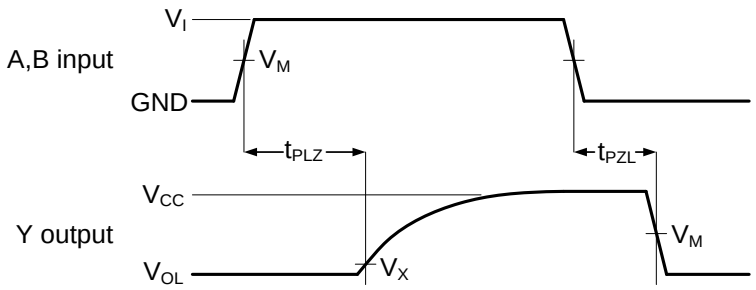


Figure 8-5 The data input (A, B) to output (Y) propagation delays

8.4.3 Measurement Points

INPUT	OUTPUT	
V_M	V_M	V_X
0.5xV_{CC}	0.5xV_{CC}	V_{OL}+0.3V

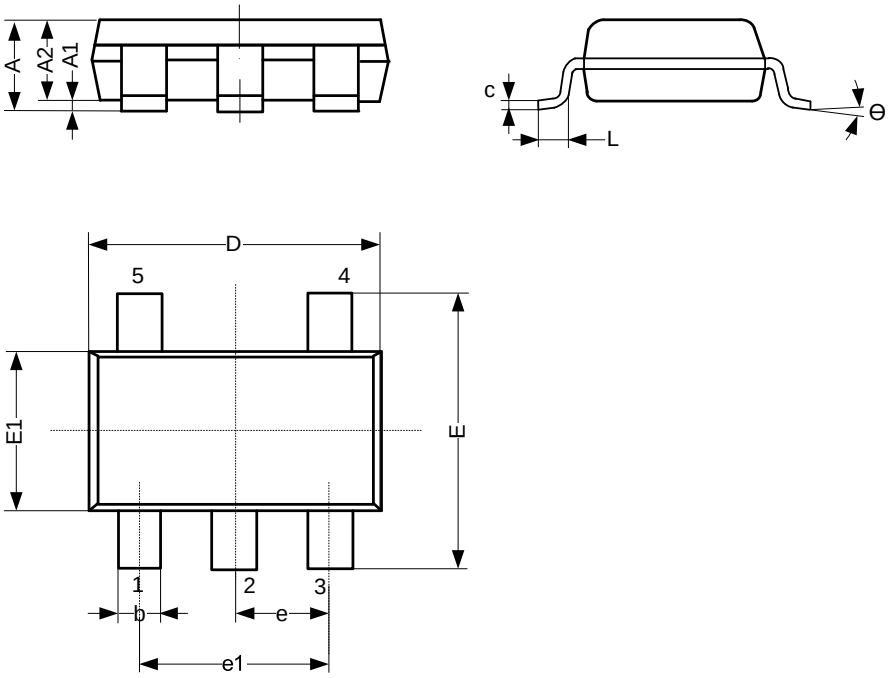
8.4.4 Test Data

INPUT		LOAD		S1		
V_I	t_r , t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
GND to V_{CC}	≤ 3.0ns	1000Ω	15pF	GND	V_{CC}	Open
GND to V_{CC}	≤ 3.0ns	1000Ω	50pF	GND	V_{CC}	Open

9 Mechanical Information

9.1 SOT-23-5L Mechanical Information

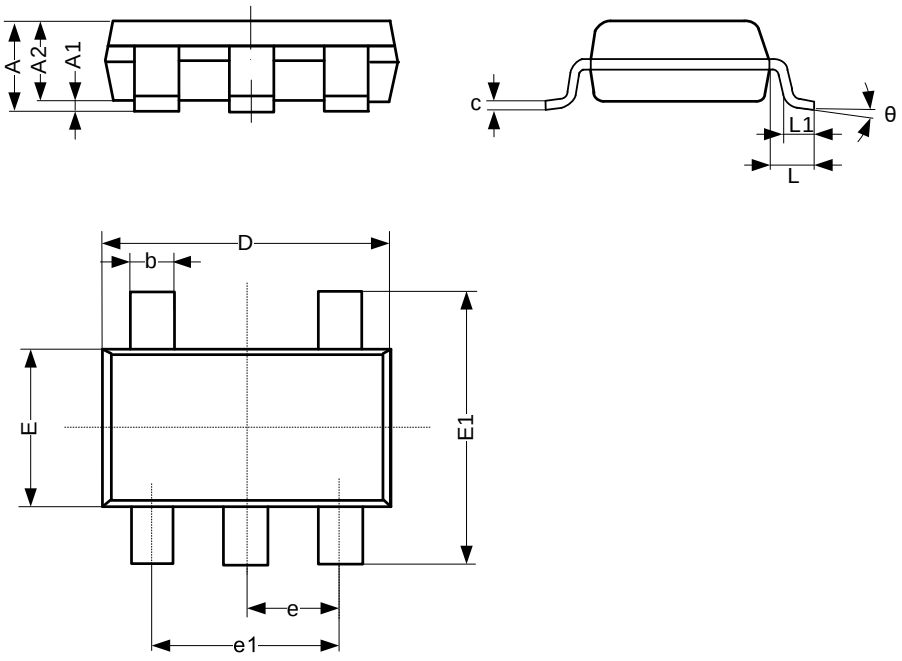
9.1.1 SOT-23-5L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.26
A1	0.00	-	0.12
A2	1.00	-	1.20
b	0.30	-	0.50
c	0.10	-	0.20
D	2.82	-	3.02
E	2.60	-	3.00
E1	1.50	-	1.70
e	0.95 BSC		
e1	1.80	-	2.00
L	0.30	-	0.60
θ	0°	-	8°
Unit: mm			

9.2 SOT-353 Mechanical Information

9.2.1 SOT-353 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.90	-	1.10
A1	0.00	-	0.10
A2	0.90	-	1.00
b	0.15	-	0.35
c	0.11	-	0.175
D	2.00	-	2.20
E	1.15	-	1.35
E1	2.15	-	2.45
e	0.65 BSC		
e1	1.20	-	1.40
L	-	0.525	-
L1	0.26	-	0.46
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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