

4-bit Dual Supply Translating Transceiver: 3-state

CJ74AVC4T774 Logic

1 Introduction

The CJ74AVC4T774 is a 4-bit, dual supply transceiver that enables bidirectional level translation. It features eight 1-bit input-output ports (An and Bn), four direction control inputs (DIR1, DIR2, DIR3 and DIR4), an output enable input (/OE) and dual supply pins (V_{CC(A)} and V_{CC(B)}). Both V_{CC(A)} and V_{CC(B)} can be supplied at any voltage between 0.8V and 3.6V making the device suitable for translating between any of the low voltage nodes (0.8V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V). Pins An, /OE and DIRn are referenced to V_{CC(A)} and pins Bn are referenced to V_{CC(B)}. A HIGH on DIRn allows transmission from An to Bn and a LOW on DIRn allows transmission from Bn to An. The output enable input (/OE) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either V_{CC(A)} or V_{CC(B)} are at GND level, both An and Bn are in the high-impedance OFF-state.

2 Available Packages

PART NUMBER	PACKAGE
CJ74AVC4T774	TSSOP16
	QFN3.5x2.5-16L

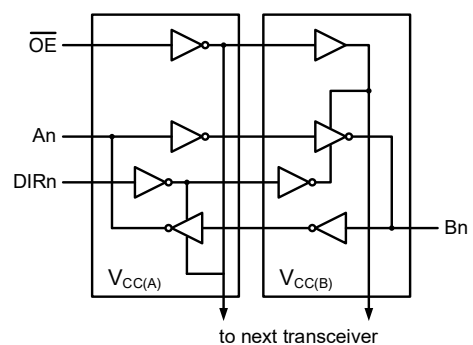
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range:
 - $V_{CC(A)}$: 0.8V to 3.6V
 - $V_{CC(B)}$: 0.8V to 3.6V
- Suspend mode
- Inputs accept voltages up to 3.6V
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from -40°C to $+125^{\circ}\text{C}$

4 Applications

- Personal electronic
- Industrial
- Enterprise
- Telecom



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74AVC4T774BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active
CJ74AVC4T774QEN	QFN3.5x2.5-16L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

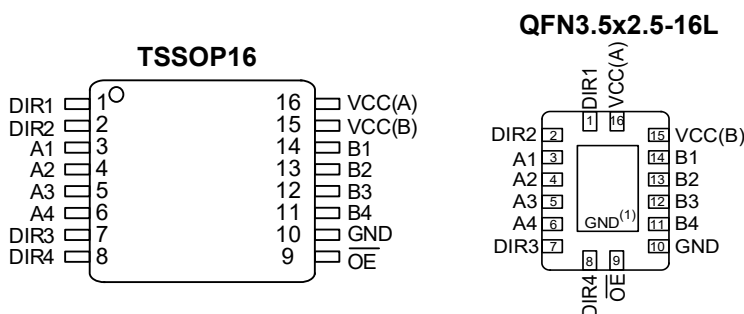


Figure 6-1 Pin configuration

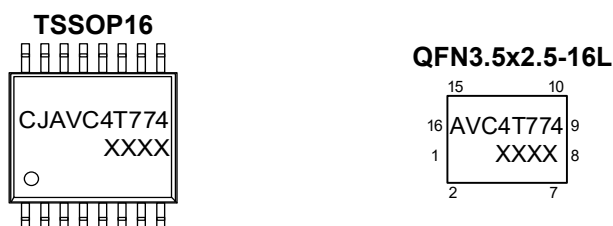
Note: (1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However if it is soldered the solder land should remain floating or be connected to GND.

6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	DIR1	I	Direction control input
2	DIR2	I	Direction control input
3	A1	I/O	Data input or output
4	A2	I/O	Data input or output
5	A3	I/O	Data input or output
6	A4	I/O	Data input or output
7	DIR3	I	Direction control input
8	DIR4	I	Direction control input
9	$\overline{\text{OE}}$	I	Output enable input (active LOW)
10	GND	G	Ground (0V)
11	B4	I/O	Data input or output
12	B3	I/O	Data input or output
13	B2	I/O	Data input or output
14	B1	I/O	Data input or output
15	VCC(B)	P	Supply voltage B (Bn inputs are referenced to VCC(B))
16	VCC(A)	P	Supply voltage A (An, $\overline{\text{OE}}$ and DIRn inputs are referenced to VCC(A))

(1) I-Input, O-Output, P-Power, G-Ground.

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

$T_{amb}=25^{\circ}\text{C}$, all voltage referenced to GND, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-	-0.5	+4.6	V
$V_{CC(B)}$	Supply voltage B	-	-0.5	+4.6	V
I_{IK}	Input clamping current	$V_I < 0\text{V}$	-50	-	mA
V_I	Input voltage	-(1)	-0.5	+4.6	V
I_{OK}	Output clamping current	$V_O < 0\text{V}$	-50	-	mA
V_O	Output voltage	Active mode ^{(1) (2) (3)}	-0.5	$V_{CCO}+0.5$	V
		Suspend or 3-state mode ⁽¹⁾	-0.5	+4.6	V
I_O	Output current	$V_O=0\text{V}$ to V_{CCO} ⁽²⁾	-	± 50	mA
I_{CC}	Supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	Ground current	-	-100	-	mA
T_{stg}	Storage temperature	-	-65	+150	$^{\circ}\text{C}$
P_{tot}	Total power dissipation	-	-	500	mW
T_L	Soldering temperature	10s	-	260	$^{\circ}\text{C}$

(1) The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

(2) V_{CCO} is the supply voltage associated with the output port.

(3) $V_{CCO}+0.5\text{V}$ should not exceed 4.6V.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-	0.8	-	3.6	V
$V_{CC(B)}$	Supply voltage B	-	0.8	-	3.6	V
V_I	Input voltage	-	0	-	3.6	V
V_O	Output voltage	Active mode ⁽¹⁾	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	3.6	V
T_{amb}	Ambient temperature	-	-40	-	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input transition rise and fall rate	$V_{CCI}=0.8\text{V}$ to 3.6V ⁽²⁾	-	-	10	ns/V

(1) V_{CCO} is the supply voltage associated with the output port.

(2) V_{CCI} is the supply voltage associated with the input port.

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	± 1000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

$T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified. ⁽¹⁾⁽²⁾

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH-level output voltage	$V_I=V_{IH}$ or V_{IL}	$I_O=-1.5\text{mA}$; $V_{CC(A)}=V_{CC(B)}=0.8\text{V}$	-	0.69	-	V
V_{OL}	LOW-level output voltage	$V_I=V_{IH}$ or V_{IL}	$I_O=1.5\text{mA}$; $V_{CC(A)}=V_{CC(B)}=0.8\text{V}$	-	0.07	-	V
I_I	Input leakage current	DIRn, $\overline{OE}$ input; $V_I=0\text{V}$ or 3.6V ; $V_{CC(A)}=V_{CC(B)}=0.8\text{V}$ to 3.6V		-	-	± 1	μA
I_{OZ}	OFF-state output current	A or B port; $V_O=0\text{V}$ or V_{CCO} ; $V_{CC(A)}=V_{CC(B)}=3.6\text{V}^{(3)}$		-	-	± 2.5	μA
		Suspend mode A port; $V_O=0\text{V}$ or V_{CCO} ; $V_{CC(A)}=3.6\text{V}$; $V_{CC(B)}=0\text{V}^{(3)}$		-	-	± 2.5	μA
		Suspend mode B port; $V_O=0\text{V}$ or V_{CCO} ; $V_{CC(A)}=0\text{V}$; $V_{CC(B)}=3.6\text{V}^{(3)}$		-	-	± 2.5	μA
I_{OFF}	Power-off leakage current	A port; V_I or $V_O=0\text{V}$ to 3.6V ; $V_{CC(A)}=0\text{V}$; $V_{CC(B)}=0.8\text{V}$ to 3.6V		-	-	± 1	μA
		B port; V_I or $V_O=0\text{V}$ to 3.6V ; $V_{CC(B)}=0\text{V}$; $V_{CC(A)}=0.8\text{V}$ to 3.6V		-	-	± 1	μA
C_I	Input capacitance	DIRn, $\overline{OE}$ input; $V_I=0\text{V}$ or 3.3V ; $V_{CC(A)}=V_{CC(B)}=3.3\text{V}$		-	2.0	-	pF
$C_{I/O}$	Input/output capacitance	A and B port; $V_O=3.3\text{V}$ or 0V ; $V_{CC(A)}=V_{CC(B)}=3.3\text{V}$		-	4.0	-	pF

(1) V_{CCO} is the supply voltage associated with the output port.

(2) V_{CCI} is the supply voltage associated with the data input port.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

7.4.2 DC Characteristics 2

$T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified. ⁽¹⁾⁽²⁾

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	Data input	$V_{CCI}=0.8\text{V}$	$0.70V_{CCI}$	-	-	V
			$V_{CCI}=1.1\text{V}$ to 1.95V	$0.65V_{CCI}$	-	-	V
			$V_{CCI}=2.3\text{V}$ to 2.7V	1.6	-	-	V
			$V_{CCI}=3.0\text{V}$ to 3.6V	2	-	-	V
		DIRn, $\overline{OE}$ input	$V_{CC(A)}=0.8\text{V}$	$0.70V_{CC(A)}$	-	-	V
			$V_{CC(A)}=1.1\text{V}$ to 1.95V	$0.65V_{CC(A)}$	-	-	V
			$V_{CC(A)}=2.3\text{V}$ to 2.7V	1.6	-	-	V
			$V_{CC(A)}=3.0\text{V}$ to 3.6V	2	-	-	V
V_{IL}	LOW-level input voltage	Data input	$V_{CCI}=0.8\text{V}$	-	-	$0.30V_{CCI}$	V
			$V_{CCI}=1.1\text{V}$ to 1.95V	-	-	$0.35V_{CCI}$	V
			$V_{CCI}=2.3\text{V}$ to 2.7V	-	-	0.7	V
			$V_{CCI}=3.0\text{V}$ to 3.6V	-	-	0.8	V
		DIRn, $\overline{OE}$ input	$V_{CC(A)}=0.8\text{V}$	-	-	$0.30V_{CC(A)}$	V
			$V_{CC(A)}=1.1\text{V}$ to 1.95V	-	-	$0.35V_{CC(A)}$	V

			$V_{CC(A)}=2.3V$ to $2.7V$	-	-	0.7	V
			$V_{CC(A)}=3.0V$ to $3.6V$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I=V_{IH}$ or V_{IL}	$I_O=-100\mu A$; $V_{CC(A)}=V_{CC(B)}=0.8V$ to $3.6V$	$V_{CCO}-0.1$	-	-	V
			$I_O=-3mA$; $V_{CC(A)}=V_{CC(B)}=1.1V$	0.85	-	-	V
			$I_O=-6mA$; $V_{CC(A)}=V_{CC(B)}=1.4V$	1.05	-	-	V
			$I_O=-8mA$; $V_{CC(A)}=V_{CC(B)}=1.65V$	1.2	-	-	V
			$I_O=-9mA$; $V_{CC(A)}=V_{CC(B)}=2.3V$	1.75	-	-	V
			$I_O=-12mA$; $V_{CC(A)}=V_{CC(B)}=3.0V$	2.3	-	-	V
			$I_O=-12mA$; $V_{CC(A)}=V_{CC(B)}=3.0V$	2.3	-	-	V
V_{OL}	LOW-level output voltage	$V_I=V_{IH}$ or V_{IL}	$I_O=100\mu A$; $V_{CC(A)}=V_{CC(B)}=0.8V$ to $3.6V$	-	-	0.1	V
			$I_O=3mA$; $V_{CC(A)}=V_{CC(B)}=1.1V$	-	-	0.25	V
			$I_O=6mA$; $V_{CC(A)}=V_{CC(B)}=1.4V$	-	-	0.35	V
			$I_O=8mA$; $V_{CC(A)}=V_{CC(B)}=1.65V$	-	-	0.45	V
			$I_O=9mA$; $V_{CC(A)}=V_{CC(B)}=2.3V$	-	-	0.55	V
			$I_O=12mA$; $V_{CC(A)}=V_{CC(B)}=3.0V$	-	-	0.7	V
I_I	Input leakage current	DIRn, OE input; $V_I=0V$ or $3.6V$; $V_{CC(A)}=V_{CC(B)}=0.8V$ to $3.6V$		-	-	± 1	μA
I_{OZ}	OFF-state output current	A or B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=V_{CC(B)}=3.6V^{(3)}$		-	-	± 5	μA
		Suspend mode A port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=3.6V$; $V_{CC(B)}=0V^{(3)}$		-	-	± 5	μA
		Suspend mode B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=0V$; $V_{CC(B)}=3.6V^{(3)}$		-	-	± 5	μA
				-	-	± 5	μA
I_{OFF}	Power-off leakage current	A port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(A)}=0V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	± 5	μA
		B port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(B)}=0V$; $V_{CC(A)}=0.8V$ to $3.6V$		-	-	± 5	μA
I_{CC}	Supply current	A port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	10	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	8	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-	-	8	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-2	-	-	μA
		B port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	10	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	8	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-2	-	-	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-	-	8	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ;		-	-	20	μA
				-	-	20	μA

		$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$				
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ; $V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	16	μA
ΔI_{CC}	Additional supply current	$V_I=3.0V$; $V_{CC(A)}=V_{CC(B)}=3.6V$	-	-	500	μA

- (1) V_{CCO} is the supply voltage associated with the output port.
(2) V_{CCI} is the supply voltage associated with the data input port.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

7.4.3 DC Characteristics 3

$T_{amb}=-40^{\circ}C$ to $+125^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.⁽¹⁾⁽²⁾

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	Data input	$V_{CCI}=0.8V$	$0.70V_{CCI}$	-	-	V
			$V_{CCI}=1.1V$ to $1.95V$	$0.65V_{CCI}$	-	-	V
			$V_{CCI}=2.3V$ to $2.7V$	1.6	-	-	V
			$V_{CCI}=3.0V$ to $3.6V$	2	-	-	V
		DIRn, OE input	$V_{CC(A)}=0.8V$	$0.70V_{CC(A)}$	-	-	V
			$V_{CC(A)}=1.1V$ to $1.95V$	$0.65V_{CC(A)}$	-	-	V
			$V_{CC(A)}=2.3V$ to $2.7V$	1.6	-	-	V
			$V_{CC(A)}=3.0V$ to $3.6V$	2	-	-	V
V_{IL}	LOW-level input voltage	Data input	$V_{CCI}=0.8V$	-	-	$0.30V_{CCI}$	V
			$V_{CCI}=1.1V$ to $1.95V$	-	-	$0.35V_{CCI}$	V
			$V_{CCI}=2.3V$ to $2.7V$	-	-	0.7	V
			$V_{CCI}=3.0V$ to $3.6V$	-	-	0.8	V
		DIRn, OE input	$V_{CC(A)}=0.8V$	-	-	$0.30V_{CC(A)}$	V
			$V_{CC(A)}=1.1V$ to $1.95V$	-	-	$0.35V_{CC(A)}$	V
			$V_{CC(A)}=2.3V$ to $2.7V$	-	-	0.7	V
			$V_{CC(A)}=3.0V$ to $3.6V$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I=V_{IH}$ or V_{IL}	$I_O=-100\mu A$; $V_{CC(A)}=V_{CC(B)}=0.8V$ to $3.6V$	$V_{CCO}-0.1$	-	-	V
			$I_O=-3mA$; $V_{CC(A)}=V_{CC(B)}=1.1V$	0.85	-	-	V
			$I_O=-6mA$; $V_{CC(A)}=V_{CC(B)}=1.4V$	1.05	-	-	V
			$I_O=-8mA$; $V_{CC(A)}=V_{CC(B)}=1.65V$	1.2	-	-	V
			$I_O=-9mA$; $V_{CC(A)}=V_{CC(B)}=2.3V$	1.75	-	-	V
			$I_O=-12mA$; $V_{CC(A)}=V_{CC(B)}=3.0V$	2.3	-	-	V
V_{OL}	LOW-level output voltage	$V_I=V_{IH}$ or V_{IL}	$I_O=100\mu A$; $V_{CC(A)}=V_{CC(B)}=0.8V$ to $3.6V$	-	-	0.1	V

			$I_o=3mA;$ $V_{CC(A)}=V_{CC(B)}=1.1V$	-	-	0.25	V
			$I_o=6mA;$ $V_{CC(A)}=V_{CC(B)}=1.4V$	-	-	0.35	V
			$I_o=8mA;$ $V_{CC(A)}=V_{CC(B)}=1.65V$	-	-	0.45	V
			$I_o=9mA;$ $V_{CC(A)}=V_{CC(B)}=2.3V$	-	-	0.55	V
			$I_o=12mA;$ $V_{CC(A)}=V_{CC(B)}=3.0V$	-	-	0.7	V
I_i	Input leakage current	DIRn, OE input; $V_i=0V$ or $3.6V$; $V_{CC(A)}=V_{CC(B)}=0.8V$ to $3.6V$		-	-	± 5	μA
I_{oz}	OFF-state output current	A or B port; $V_o=0V$ or V_{CCO} ; $V_{CC(A)}=V_{CC(B)}=3.6V^{(3)}$		-	-	± 30	μA
		Suspend mode A port; $V_o=0V$ or V_{CCO} ; $V_{CC(A)}=3.6V$; $V_{CC(B)}=0V^{(3)}$		-	-	± 30	μA
		Suspend mode B port; $V_o=0V$ or V_{CCO} ; $V_{CC(A)}=0V$; $V_{CC(B)}=3.6V^{(3)}$		-	-	± 30	μA
I_{OFF}	Power-off leakage current	A port; V_i or $V_o=0V$ to $3.6V$; $V_{CC(A)}=0V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	± 30	μA
		B port; V_i or $V_o=0V$ to $3.6V$; $V_{CC(B)}=0V$; $V_{CC(A)}=0.8V$ to $3.6V$		-	-	± 30	μA
I_{CC}	Supply current	A port; $V_i=0V$ or V_{CCI} ; $I_o=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	55	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	50	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-	-	50	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-12	-	-	μA
		B port; $V_i=0V$ or V_{CCI} ; $I_o=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	55	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	50	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-12	-	-	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-	-	50	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_o=0A$; $V_i=0V$ or V_{CCI} ; $V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	70	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_o=0A$; $V_i=0V$ or V_{CCI} ; $V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$		-	-	65	μA
				-	-		
				-	-		
ΔI_{CC}	Additional supply current	$V_i=3.0V$; $V_{CC(A)}=V_{CC(B)}=3.6V$		-	-	650	μA

- (1) V_{CCO} is the supply voltage associated with the output port.
(2) V_{CCI} is the supply voltage associated with the data input port.
(3) For I/O ports, the parameter I_{oz} includes the input leakage current.

7.4.4 Typical Total Supply Current ($I_{CC(A)}+I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							UNIT
	0V	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
0V	0	0.1	0.1	0.1	0.1	0.1	0.1	uA
0.8V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	uA
1.2V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	uA
1.5V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	uA
1.8V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	uA
2.5V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	uA
3.3V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	uA

7.4.5 AC Characteristics 1

$T_{amb}=25^{\circ}\text{C}$, $V_{CC(A)}=V_{CC(B)}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(A)}=V_{CC(B)}$						UNIT
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
C_{PD}	Power dissipation capacitance	A port: (direction An to Bn); Output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction An to Bn); Output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction Bn to An); Output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction Bn to An); Output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction An to Bn); Output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction An to Bn); Output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction Bn to An); Output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction Bn to An); Output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

Note:

(1) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =load capacitance in pF;

V_{CC} =supply voltage in V;

N =number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of the outputs.

(2) $f_i=10\text{MHz}$; $V_i=\text{GND to } V_{CC}$; $t_r=t_f=1\text{ns}$; $C_L=0\text{pF}$; $R_L=\infty\Omega$.

7.4.6 AC Characteristics 2

$T_{amb}=25^{\circ}\text{C}$, $V_{CC(A)}=0.8\text{V}$, voltages are referenced to GND (ground=0V), unless otherwise specified. ⁽¹⁾

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$						UNIT
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
t_{pd}	Propagation delay	An to Bn	14.5	7.3	6.5	6.2	5.9	6.0	ns

		Bn to An	14.5	12.7	12.4	12.3	12.1	12.0	ns
t_{dis}	Disable time	$\overline{OE}$ to An	14.3	14.3	14.3	14.3	14.3	14.3	ns
		$\overline{OE}$ to Bn	17.0	9.9	9.0	9.4	9.0	9.7	ns
t_{en}	Enable time	$\overline{OE}$ to An	18.2	18.2	18.2	18.2	18.2	18.2	ns
		$\overline{OE}$ to Bn	19.2	10.7	9.8	9.6	9.7	10.2	ns

(1) t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

7.4.7 AC Characteristics 3

$T_{amb}=25^{\circ}C$, $V_{CC(B)}=0.8V$, voltages are referenced to GND (ground=0V), unless otherwise specified.⁽¹⁾

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(A)}$						UNIT
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
t_{pd}	Propagation delay	An to Bn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		Bn to An	14.5	7.3	6.5	6.2	5.9	6.0	ns
t_{dis}	Disable time	$\overline{OE}$ to An	14.3	5.5	4.1	4.0	3.0	3.5	ns
		$\overline{OE}$ to Bn	17.0	13.8	13.4	13.1	12.9	12.7	ns
t_{en}	Enable time	$\overline{OE}$ to An	18.2	5.6	4.0	3.2	2.4	2.2	ns
		$\overline{OE}$ to Bn	19.2	14.6	14.1	13.9	13.7	13.6	ns

(1) t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

7.4.8 AC Characteristics 4

$T_{amb}=-40^{\circ}C$ to $+85^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.⁽¹⁾

SYMBOL	PARAMETER	CONDITIONS	V _{CC(B)}										UNIT
			1.2V±0.1V		1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{CC(A)} =1.1V to 1.3V													
t _{pd}	Propagation Delay	An to Bn	2.0	10.5	1.3	7.8	1.2	6.9	1.0	5.9	0.8	5.7	ns
		Bn to An	2.0	10.5	1.5	9.9	1.5	9.7	1.4	9.4	1.4	9.3	ns
t _{dis}	Disable time	$\overline{OE}$ to An	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns
		$\overline{OE}$ to Bn	2.0	11.1	2.0	8.6	1.0	8.0	0.7	7.0	1.0	8.0	ns
t _{en}	Enable time	$\overline{OE}$ to An	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	ns
		$\overline{OE}$ to Bn	2.0	15.0	2.0	11.0	2.0	9.4	1.0	7.8	1.0	7.4	ns
V _{CC(A)} =1.4V to 1.6V													
t _{pd}	Propagation Delay	An to Bn	1.5	9.9	1.0	7.1	1.0	6.0	0.5	4.8	0.5	4.3	ns
		Bn to An	1.3	7.8	1.0	7.1	0.9	6.9	0.8	6.6	0.6	6.5	ns
t _{dis}	Disable time	$\overline{OE}$ to An	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	ns
		$\overline{OE}$ to Bn	2.0	10.2	1.5	7.5	0.9	7.2	0.4	6.2	0.4	6.1	ns
t _{en}	Enable time	$\overline{OE}$ to An	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$\overline{OE}$ to Bn	2.0	14.4	1.4	7.9	1.3	7.7	1.1	6.4	1.1	5.6	ns

V _{CC(A)} =1.65V to 1.95V													
t _{pd}	Propagation Delay	An to Bn	1.5	9.7	0.9	6.9	0.8	5.7	0.5	4.5	0.3	4.0	ns
		Bn to An	1.2	6.9	1.0	6.0	0.8	5.7	0.5	5.5	0.5	5.3	ns
t _{dis}	Disable time	$\overline{OE}$ to An	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	ns
		$\overline{OE}$ to Bn	2.0	9.9	1.5	7.0	0.8	6.9	0.2	5.8	0.2	5.9	ns
t _{en}	Enable time	$\overline{OE}$ to An	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	ns
		$\overline{OE}$ to Bn	1.5	13.9	1.2	7.2	1.2	6.9	0.8	5.4	0.6	5.0	ns
V _{CC(A)} =2.3V to 2.7V													
t _{pd}	Propagation Delay	An to Bn	1.4	9.4	0.8	6.6	0.5	5.5	0.4	4.2	0.2	3.7	ns
		Bn to An	1.0	5.9	0.5	4.8	0.5	4.5	0.4	4.2	0.3	3.9	ns
t _{dis}	Disable time	$\overline{OE}$ to An	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	ns
		$\overline{OE}$ to Bn	2.0	9.3	1.5	6.7	0.7	6.3	0.2	5.0	0.2	5.7	ns
t _{en}	Enable time	$\overline{OE}$ to An	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	ns
		$\overline{OE}$ to Bn	1.5	13.6	1.0	6.8	1.0	6.0	0.8	4.6	0.6	4.2	ns
V _{CC(A)} =3.0V to 3.6V													
t _{pd}	Propagation Delay	An to Bn	1.4	9.3	0.6	6.5	0.5	5.3	0.3	3.9	0.2	3.5	ns
		Bn to An	0.8	5.7	0.5	4.3	0.3	4.0	0.2	3.7	0.2	3.5	ns
t _{dis}	Disable time	$\overline{OE}$ to An	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	ns
		$\overline{OE}$ to Bn	2.0	9.0	1.5	6.4	0.7	6.1	0.2	4.8	0.2	5.6	ns
t _{en}	Enable time	$\overline{OE}$ to An	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	ns
		$\overline{OE}$ to Bn	1.5	13.4	1.0	6.7	1.0	5.9	0.7	4.4	0.5	4.0	ns

(1) t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

7.4.9 AC Characteristics 5

$T_{amb}=-40^{\circ}C$ to $+125^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified. ⁽¹⁾

SYMBOL	PARAMETER	CONDITIONS	V _{CC(B)}										UNIT
			1.2V±0.1V		1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{CC(A)} =1.1V to 1.3V													
t _{pd}	Propagation Delay	An to Bn	2.0	12.1	1.3	9.0	1.2	8.0	1.0	6.8	0.8	6.6	ns
		Bn to An	2.0	12.1	1.5	11.4	1.5	11.2	1.4	10.9	1.4	10.7	ns
t _{dis}	Disable time	$\overline{OE}$ to An	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	ns
		$\overline{OE}$ to Bn	2.0	12.8	2.0	9.9	1.0	9.2	0.7	8.1	1.0	9.2	ns
t _{en}	Enable time	$\overline{OE}$ to An	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	ns
		$\overline{OE}$ to Bn	2.0	17.3	2.0	12.7	2.0	10.9	1.0	9.0	1.0	8.6	ns
V _{CC(A)} =1.4V to 1.6V													
t _{pd}	Propagation Delay	An to Bn	1.5	11.4	1.0	8.2	1.0	6.9	0.5	5.6	0.5	5.0	ns
		Bn to An	1.3	9.0	1.0	8.2	0.9	8.0	0.8	7.6	0.6	7.5	ns

t _{dis}	Disable time	$\overline{OE}$ to An	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	ns
		$\overline{OE}$ to Bn	2.0	11.8	1.5	8.7	0.9	8.3	0.4	7.2	0.4	7.1	ns
t _{en}	Enable time	$\overline{OE}$ to An	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	ns
		$\overline{OE}$ to Bn	2.0	16.6	1.4	9.1	1.3	8.9	1.1	7.4	1.1	6.5	ns
V _{CC(A)} =1.65V to 1.95V													
t _{pd}	Propagation Delay	An to Bn	1.5	11.2	0.9	8.0	0.8	6.6	0.5	5.2	0.3	4.6	ns
		Bn to An	1.2	8.0	1.0	6.9	0.8	6.6	0.5	6.4	0.5	6.1	ns
t _{dis}	Disable time	$\overline{OE}$ to An	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	ns
		$\overline{OE}$ to Bn	2.0	11.4	1.5	8.1	0.8	8.0	0.2	6.7	0.2	6.8	ns
t _{en}	Enable time	$\overline{OE}$ to An	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns
		$\overline{OE}$ to Bn	1.5	16.0	1.2	8.3	1.2	8.0	0.8	6.3	0.6	5.8	ns
V _{CC(A)} =2.3V to 2.7V													
t _{pd}	Propagation Delay	An to Bn	1.4	10.9	0.8	7.6	0.5	6.4	0.4	4.9	0.2	4.3	ns
		Bn to An	1.0	6.8	0.5	5.6	0.5	5.2	0.4	4.9	0.3	4.5	ns
t _{dis}	Disable time	$\overline{OE}$ to An	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	ns
		$\overline{OE}$ to Bn	2.0	10.7	1.5	7.8	0.7	7.3	0.2	5.8	0.2	6.6	ns
t _{en}	Enable time	$\overline{OE}$ to An	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	ns
		$\overline{OE}$ to Bn	1.5	15.7	1.0	7.9	1.0	6.9	0.8	5.3	0.6	4.9	ns
V _{CC(A)} =3.0V to 3.6V													
t _{pd}	Propagation Delay	An to Bn	1.4	10.7	0.6	7.5	0.5	6.1	0.3	4.5	0.2	4.1	ns
		Bn to An	0.8	6.6	0.5	5.0	0.3	4.6	0.2	4.3	0.2	4.1	ns
t _{dis}	Disable time	$\overline{OE}$ to An	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	ns
		$\overline{OE}$ to Bn	2.0	10.4	1.5	7.4	0.7	7.1	0.2	5.6	0.2	6.5	ns
t _{en}	Enable time	$\overline{OE}$ to An	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	ns
		$\overline{OE}$ to Bn	1.5	15.5	1.0	7.8	1.0	6.8	0.7	5.1	0.5	4.6	ns

(1) t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

8 Detailed Description

8.1 Overview

The CJ74AVC4T774 is a 4-bit, dual supply transceiver that enables bidirectional level translation. It features eight 1-bit input-output ports (A_n and B_n), four direction control inputs (DIR1, DIR2, DIR3 and DIR4), an output enable input ($\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8V and 3.6V making the device suitable for translating between any of the low voltage nodes (0.8V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V). Pins A_n , $\overline{OE}$ and DIRn are referenced to $V_{CC(A)}$ and pins B_n are referenced to $V_{CC(B)}$. A HIGH on DIRn allows transmission from A_n to B_n and a LOW on DIRn allows transmission from B_n to A_n . The output enable input ($\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A_n and B_n are in the high-impedance OFF-state.

8.2 Functional Block Diagram

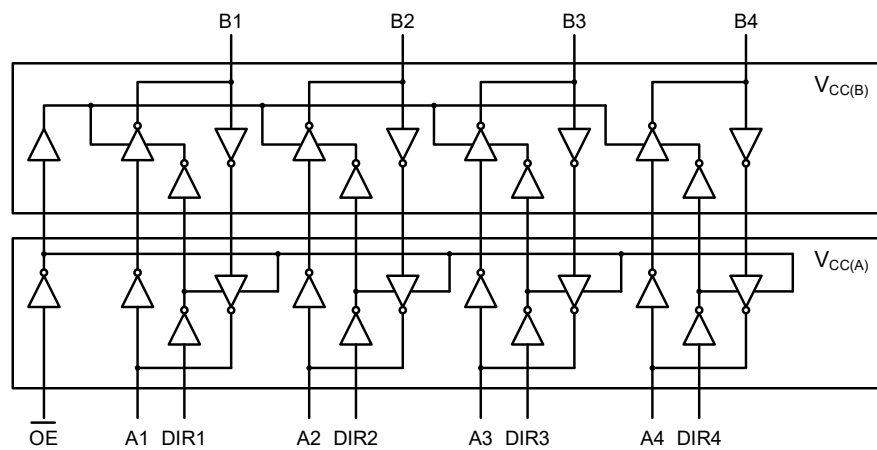


Figure 8-1 Logic symbol

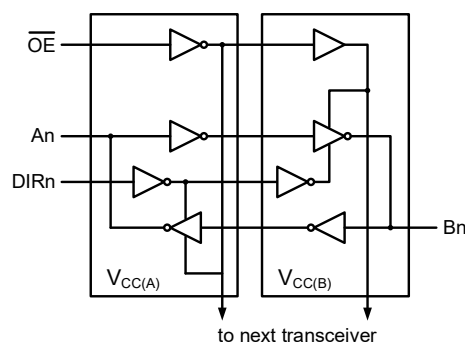


Figure 8-2 Logic diagram (one 1-bit transceiver)

8.3 Function Table

SUPPLY VOLTAGE	INPUT					INPUT/OUTPUT	
$V_{CC(A)}, V_{CC(B)}$	$\overline{OE}$	DIR1	DIR2	DIR3	DIR4	An	Bn
0.8V to 3.6V	L	L	X	X	X	A1=B1	input B1
0.8V to 3.6V	L	H	X	X	X	input A1	B1=A1
0.8V to 3.6V	L	X	L	X	X	A2=B2	input B2
0.8V to 3.6V	L	X	H	X	X	input A2	B2=A2
0.8V to 3.6V	L	X	X	L	X	A3=B3	input B3
0.8V to 3.6V	L	X	X	H	X	input A3	B3=A3
0.8V to 3.6V	L	X	X	X	L	A4=B4	input B4
0.8V to 3.6V	L	X	X	X	H	input A4	B4=A4
0.8V to 3.6V	H	X	X	X	X	Z	Z
GND	X	X	X	X	X	Z	Z

Note:

- (1) H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.
- (2) The An, DIRn and $\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The Bn input circuit is referenced to $V_{CC(B)}$.
- (3) If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

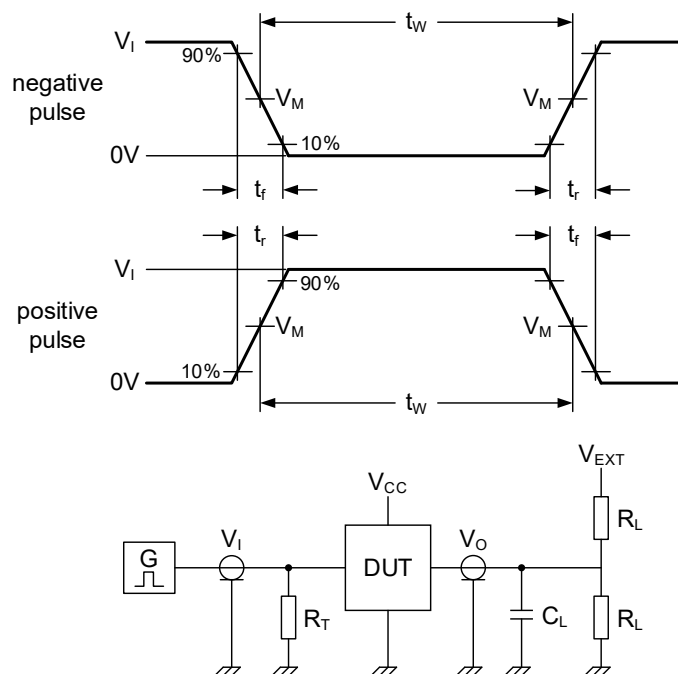


Figure 8-3 Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} =External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

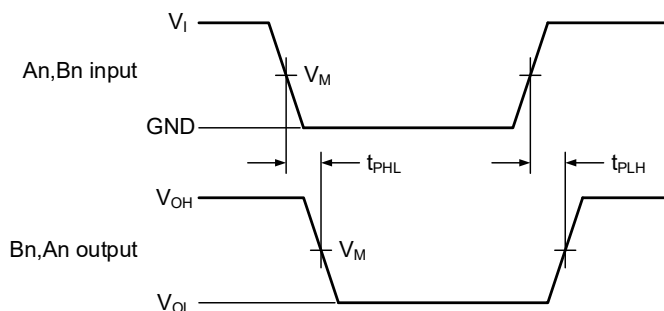


Figure 8-4 The data input (An, Bn) to output (Bn, An) propagation delay times

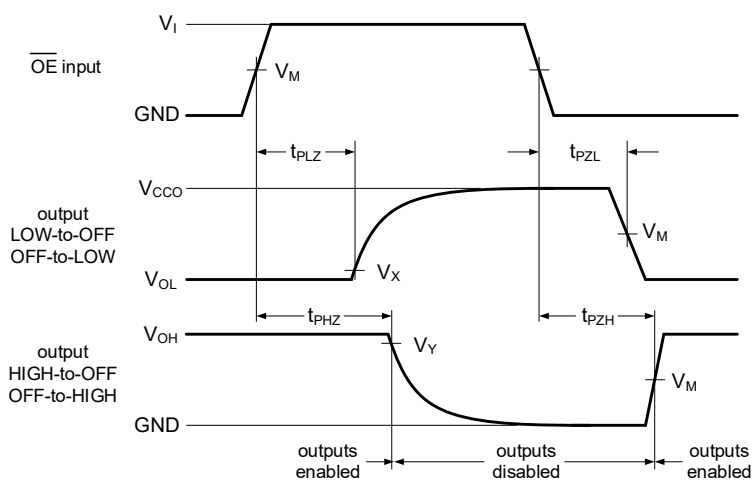


Figure 8-5 Enable and disable times

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT ⁽¹⁾	OUTPUT ⁽²⁾		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.1V$	$V_{OH}-0.1V$
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.15V$	$V_{OH}-0.15V$
3.0V to 3.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.3V$	$V_{OH}-0.3V$

(1) V_{CCI} is the supply voltage associated with the data input port.

(2) V_{CCO} is the supply voltage associated with the output port.

8.4.4 Test Data

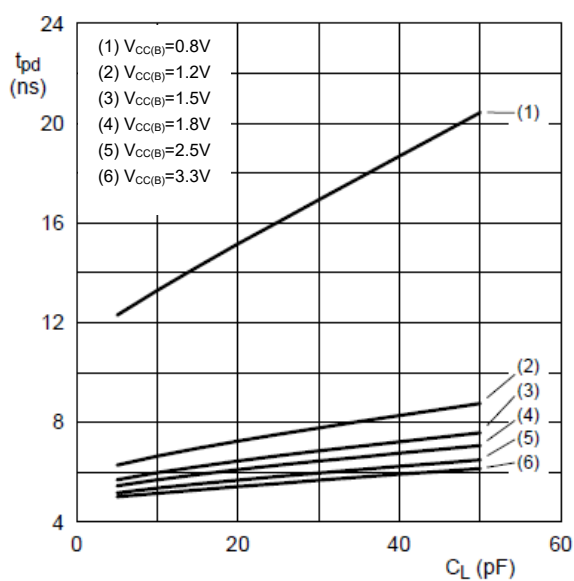
SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	$V_I^{(1)}$	$\Delta t/\Delta V^{(2)}$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	$t_{PZL}, t_{PLZ}^{(3)}$
0.8V to 1.6V	V_{CCI}	$\leq 1.0ns/V$	15pF	2k Ω	Open	GND	$2V_{CCO}$
1.65V to 2.7V	V_{CCI}	$\leq 1.0ns/V$	15pF	2k Ω	Open	GND	$2V_{CCO}$
3.0V to 3.6V	V_{CCI}	$\leq 1.0ns/V$	15pF	2k Ω	Open	GND	$2V_{CCO}$

(1) V_{CCI} is the supply voltage associated with the data input port.

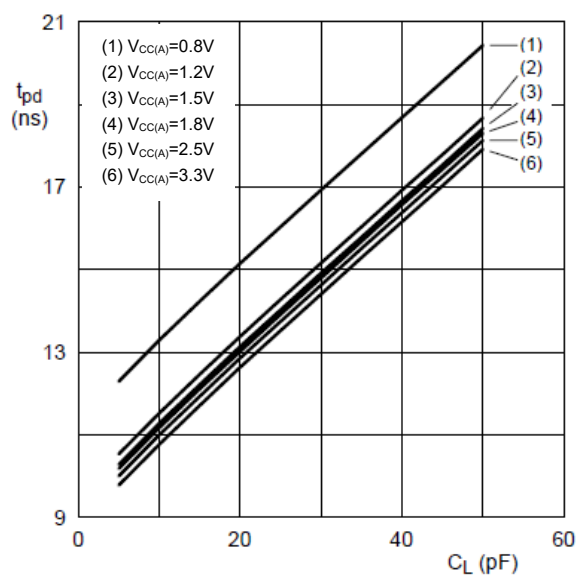
(2) $dV/dt \geq 1.0V/ns$.

(3) V_{CCO} is the supply voltage associated with the output port.

9 Characteristic Curve

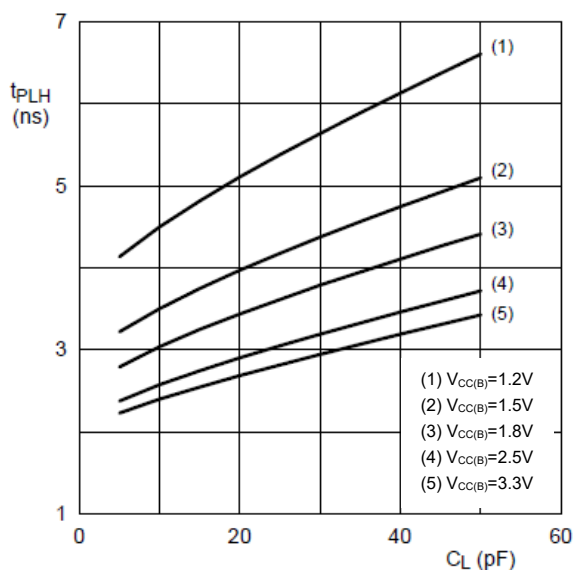


a. Propagation delay (A to B); $V_{CC(A)}=0.8V$

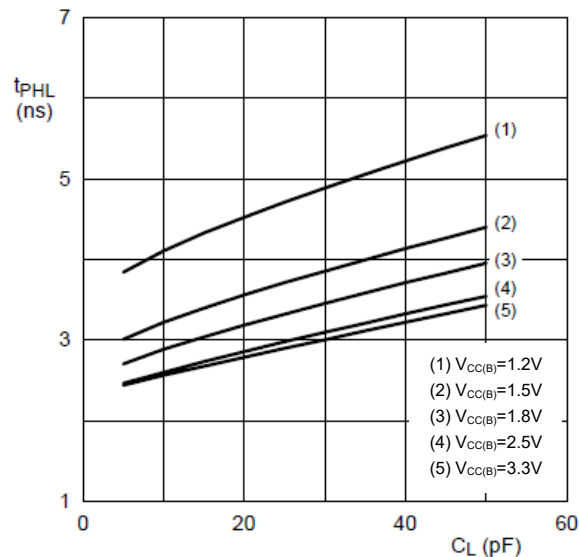


b. Propagation delay (A to B); $V_{CC(B)}=0.8V$

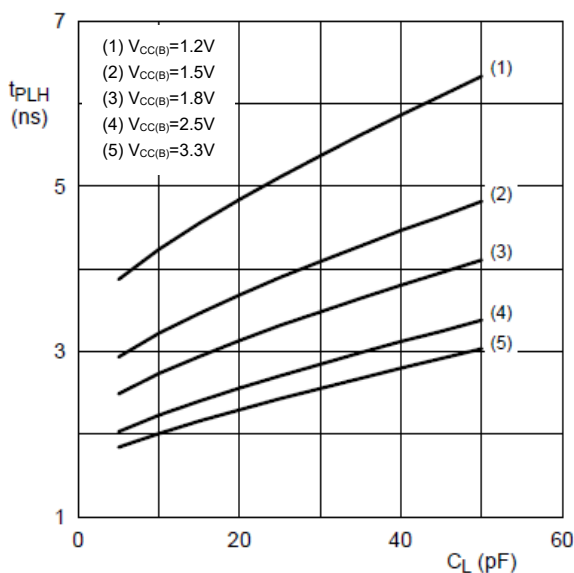
Figure 9-1 Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$



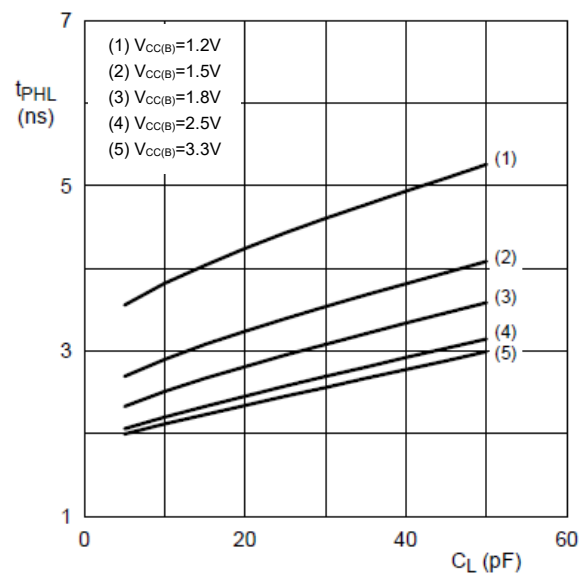
a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.2V$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.2V$

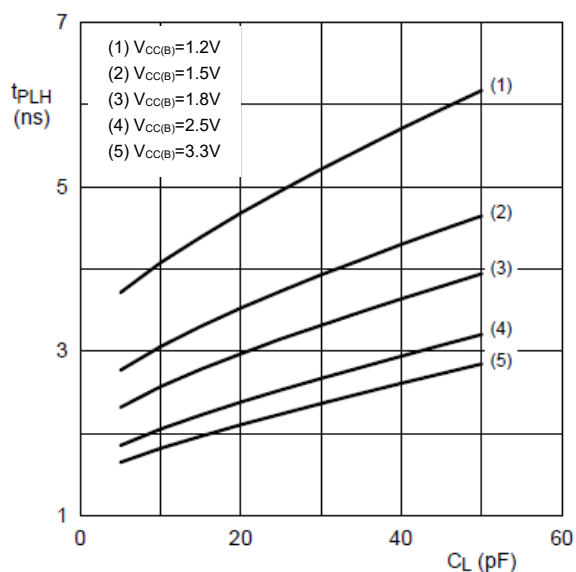


c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.5V$

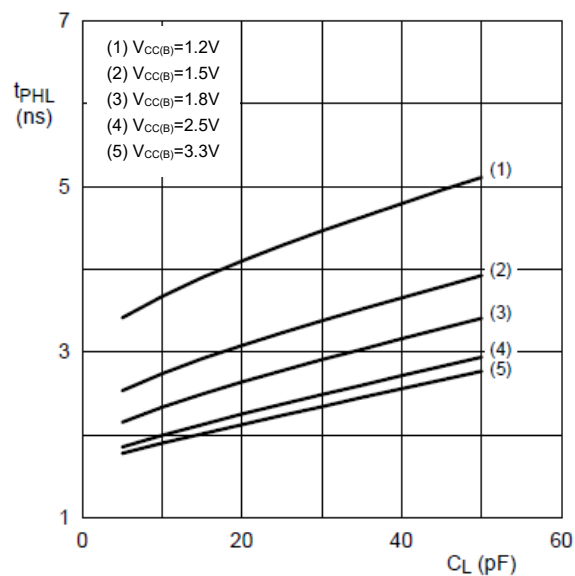


d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.5V$

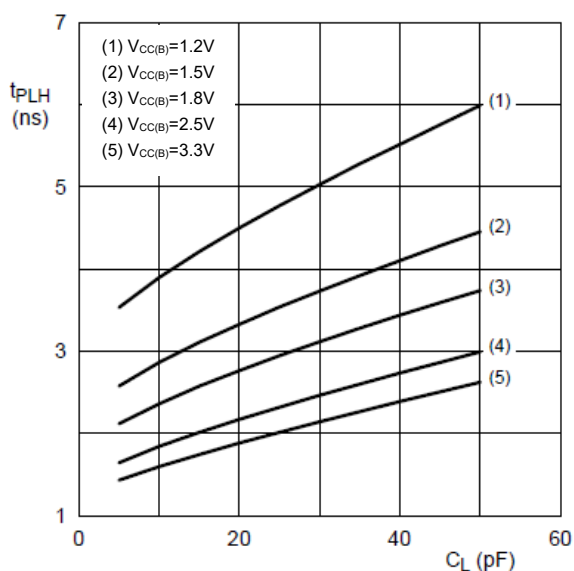
Figure 9-2 Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$



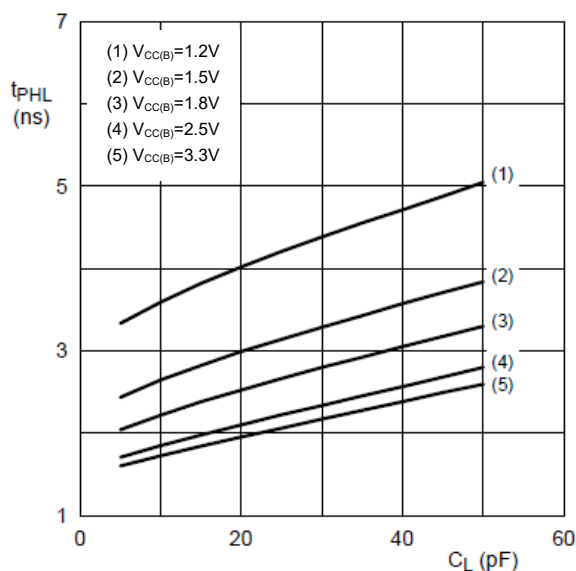
a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.8V$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.8V$

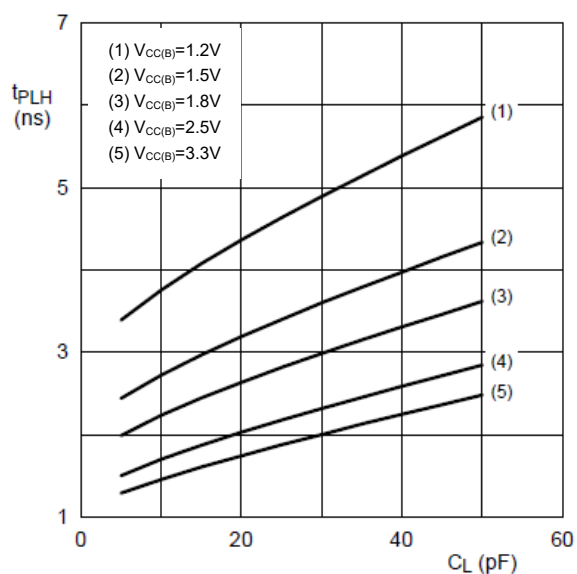


c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=2.5V$

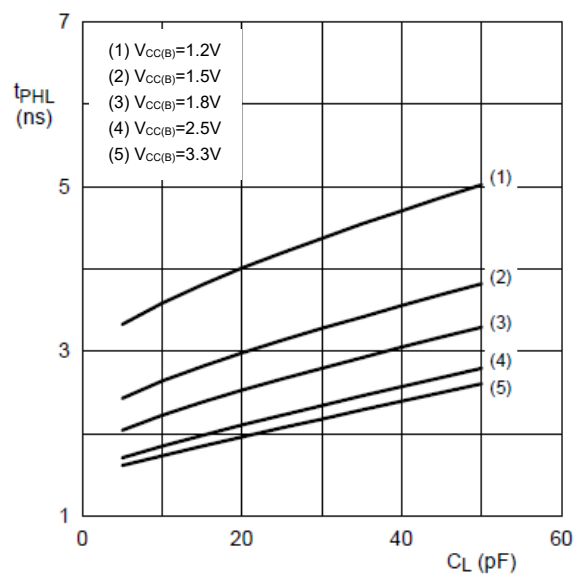


d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=2.5V$

Figure 9-3 Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$



a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 3.3V$



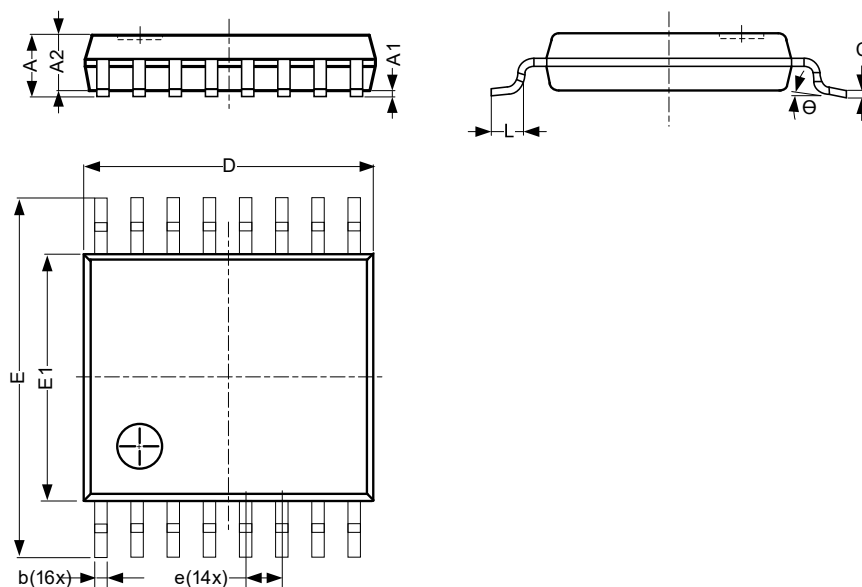
b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 3.3V$

Figure 9-4 Typical propagation delay versus load capacitance; $T_{amb} = 25^\circ C$

10 Mechanical Information

10.1 TSSOP16 Mechanical Information

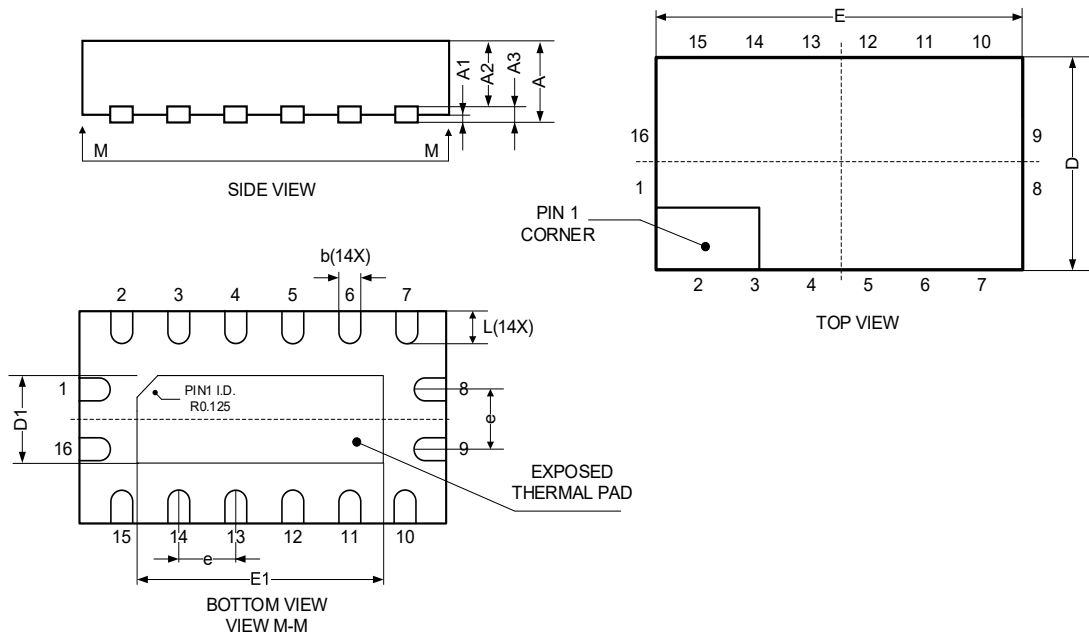
10.1.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
θ	0°	-	8°
Unit: mm			

10.2 QFN3.5x2.5-16L Mechanical Information

10.2.1 QFN3.5x2.5-16L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.80	-	1.00
A1	0.00	-	0.05
A2	0.60	-	0.70
A3	-	0.20	-
D	2.40	-	2.60
E	3.40	-	3.60
e	0.50 BSC		
b	0.18	-	0.30
L	0.30	-	0.50
D1	0.85	-	1.15
E1	1.85	-	2.15
Unit: mm			

11 Notes and Revision History

11.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

11.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

11.3 Revision History

July, 2025: rev - 1.1, Change marking information.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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