**4-bit Bus Switch**

# CJ74CBTLV3125 Logic

## 1 Introduction

CJ74CBTLV3125 is a 4-bit bus single-channel analog switch circuit. Each bit is controlled by the separate enable port (/1OE to /4OE) and enable ports are all Schmitt designed. To ensure the high-impedance OFF-state during power-up or power-down, it is recommended that /nOE connect an external pull-up resistor to $V_{CC}$. When the circuit is in power down state ($V_{CC}$=0V), the control port and the switch port are in high resistance state, which can effectively prevent backflow and circuit damage.

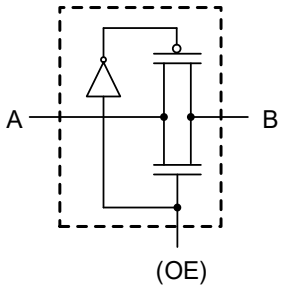
## 2 Available Packages

| PART NUMBER | PACKAGE |
|---|---|
| CJ74CBTLV3125 | SOP14 |
| | TSSOP14 |
| | SSOP16 |

**Note:** For all available packages, please refer to the part Orderable Information.

## 3 Features

- Power supply voltage: 2.3V to 3.6V
- ON resistance typical: 2.8Ω ($V_{CC}$=3.3V)
- Rail-to-rail analog switch
- Power down ($V_{CC}$=0V) anti-backflow function
- Specified from -40°C to +125°C




Simplified schematic

## 4 Orderable Information

| DEVICE | PACKAGE | OP TEMP | ECO PLAN | MSL | PACKING OPTION | SORT |
|---|---|---|---|---|---|---|
| CJ74CBTLV3125ADN | SOP14 | -40~125°C | RoHS & Green | Level 3 168HR | Tape and Reel 4000 Units / Reel | Active |
| CJ74CBTLV3125BDN | TSSOP14 | -40~125°C | RoHS & Green | Level 3 168HR | Tape and Reel 5000 Units / Reel | Active |
| CJ74CBTLV3125SEA | SSOP16 | -40~125°C | RoHS & Green | Level 3 168HR | Tape and Reel 4000 Units / Reel | Active |

**Note:**

**ECO PLAN:** For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

**MSL:** Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

**SORT:** Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

# 5 Pin Configuration and Marking Information

## 5.1 Pin Configuration

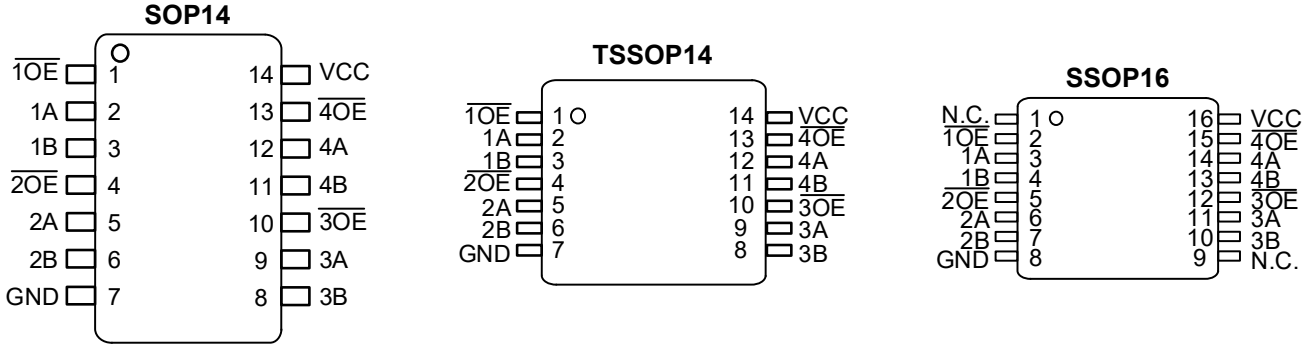


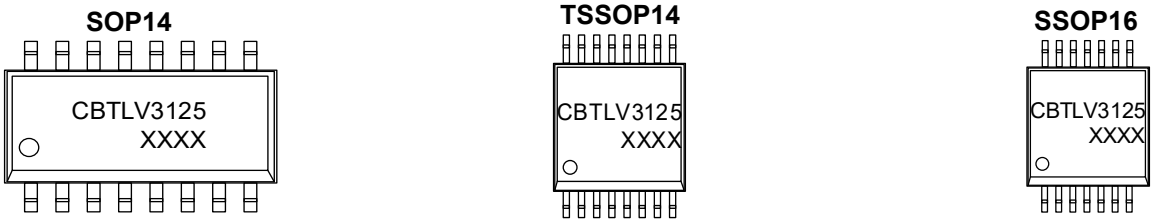

**Figure 5-1 Pin configuration**

## 5.2 Pin Function

| PIN | | | I/O(1) | DESCRIPTION |
|---|---|---|---|---|
| No. | | NAME | | |
| SOP14/TSSOP14 | SSOP16 | | | |
| - | 1 | N.C. | - | Not connected |
| 1 | 2 | $\overline{1OE}$ | I | Output enable input |
| 2 | 3 | 1A | I/O | A input/output |
| 3 | 4 | 1B | I/O | B output/input |
| 4 | 5 | $\overline{2OE}$ | I | Output enable input |
| 5 | 6 | 2A | I/O | A input/output |
| 6 | 7 | 2B | I/O | B output/input |
| 7 | 8 | GND | G | Ground (0V) |
| - | 9 | N.C. | - | Not connected |
| 8 | 10 | 3B | I/O | B output/input |
| 9 | 11 | 3A | I/O | A input/output |
| 10 | 12 | $\overline{3OE}$ | I | Output enable input |
| 11 | 13 | 4B | I/O | B output/input |
| 12 | 14 | 4A | I/O | A input/output |
| 13 | 15 | $\overline{4OE}$ | I | Output enable input |
| 14 | 16 | VCC | P | Power supply voltage |

(1) I-Input, O-Output, P-Power, G-Ground

## 5.3 Marking Information




XXXX: Code, indicates weekly record information.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | - | -0.5 | +4.6 | V |
| $V_I$ | Input voltage | Control input | -0.5 | +4.6 | V |
| $V_{SW}$ | Switch voltage | Enable and disable mode | -0.5 | $V_{CC}$+0.5 | V |
| $I_{IK}$ | Input clamping current | $V_I$<-0.5V | -50 | - | mA |
| $I_{SK}$ | Switch clamping current | $V_I$<-0.5V | -50 | - | mA |
| $I_{SW}$ | Switch current | $V_{SW}$=0 to $V_{CC}$ | - | ±128 | mA |
| $I_{CC}$ | Supply current | - | - | ±100 | mA |
| $I_{GND}$ | Ground current | - | -100 | - | mA |
| $T_{stg}$ | Storage temperature | - | -65 | 150 | °C |
| $T_L$ | Soldering temperature | 10s | - | 260 | °C |

**Note:** Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

## 6.2 Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | - | 2.3 | - | 3.6 | V |
| $V_I$ | Input voltage | - | 0 | - | 3.6 | V |
| $V_{SW}$ | Switch voltage | Enable and disable mode | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | Ambient temperature | - | -40 | - | +125 | °C |

## 6.3 Electrical Characteristics

### 6.3.1 DC Characteristics 1

$T_{amb}$=-40°C to +85°C, GND=0V, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$=2.3V to 2.7V | | 1.7 | - | - | V |
| | | $V_{CC}$=3.0V to 6V | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$=2.3V to 2.7V | | - | - | 0.7 | V |
| | | $V_{CC}$=3.0V to 6V | | - | - | 0.9 | V |
| $I_I$ | Input leakage current | Pin $\overline{nOE}$ ; $V_I$=GND to $V_{CC}$; $V_{CC}$=3.6V | | - | - | ±1 | uA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$=3.6V | | - | - | ±1 | uA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$=3.6V | | - | - | ±1 | uA |
| $I_{OFF}$ | Power-off leakage current | $V_I$ or $V_O$=0 V to 3.6 V; $V_{CC}$=0V | | - | - | ±10 | uA |
| $I_{CC}$ | Supply current | $V_I$=GND or $V_{CC}$; $I_O$=0 A; $V_{SW}$=GND or $V_{CC}$; $V_{CC}$=3.6V | | - | - | 10 | uA |
| $\Delta I_{CC}$ | Additional supply current | Pin $\overline{nOE}$ ; $V_I$=$V_{CC}$ - 0.6V; $V_{SW}$=GND or $V_{CC}$; $V_{CC}$=3.6V | | - | - | 300 | uA |
| $R_{ON}$ | ON resistance | $V_{CC}$=2.3V to 2.7V; See Figure 7-2 to 7-4 | $I_{SW}$=64mA; $V_I$=0V | - | 3.3 | 8 | Ω |
| | | | $I_{SW}$=24mA; $V_I$=0V | - | 3.2 | 8 | Ω |
| | | | $I_{SW}$=15mA; $V_I$=1.7V | - | 10.8 | 40 | Ω |
| | | $V_{CC}$=3.0V to 3.6V; See Figure 7-5 to 7-7 | $I_{SW}$=64mA; $V_I$=0V | - | 2.8 | 7 | Ω |
| | | | $I_{SW}$=24mA; $V_I$=0V | - | 2.8 | 7 | Ω |
| | | | $I_{SW}$=15mA; $V_I$=2.4V | - | 7.1 | 15 | Ω |

**Note:** All typical values are measured at $V_{CC}$=2.5V, 3.3V (unless otherwise specified) and $T_{amb}$=25°C.

### 6.3.2 DC Characteristics 2

$T_{amb}$=-40°C to +125°C, GND=0V, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$=2.3V to 2.7V | | 1.7 | - | - | V |
| | | $V_{CC}$=3.0V to 6V | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$=2.3V to 2.7V | | - | - | 0.7 | V |
| | | $V_{CC}$=3.0V to 6V | | - | - | 0.9 | V |
| $I_I$ | Input leakage current | Pin $\overline{nOE}$ ;$V_I$=GND to $V_{CC}$; $V_{CC}$=3.6V | | - | - | ±20 | uA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$=3.6V | | - | - | ±20 | uA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$=3.6V | | - | - | ±20 | uA |
| $I_{OFF}$ | Power-off leakage current | $V_I$ or $V_O$=0 V to 3.6 V; $V_{CC}$=0V | | - | - | ±50 | uA |
| $I_{CC}$ | Supply current | $V_I$=GND or $V_{CC}$; $I_O$=0 A; $V_{SW}$=GND or $V_{CC}$; $V_{CC}$=3.6V | | - | - | 50 | uA |
| $\Delta I_{CC}$ | Additional supply current | Pin $\overline{nOE}$ ; $V_I$=$V_{CC}$ - 0.6V; $V_{SW}$=GND or $V_{CC}$; $V_{CC}$=3.6V | | - | - | 2000 | uA |
| $R_{ON}$ | ON resistance | $V_{CC}$=2.3V to 2.7V; See Figure 7-2 to 7-4 | $I_{SW}$=64mA; $V_I$=0V | - | - | 15 | Ω |
| | | | $I_{SW}$=24mA; $V_I$=0V | - | - | 15 | Ω |
| | | | $I_{SW}$=15mA; $V_I$=1.7V | - | - | 60 | Ω |
| | | $V_{CC}$=3.0V to 3.6V; See Figure 7-5 to 7-7 | $I_{SW}$=64mA; $V_I$=0V | - | - | 11 | Ω |
| | | | $I_{SW}$=24mA; $V_I$=0V | - | - | 11 | Ω |
| | | | $I_{SW}$=15mA; $V_I$=2.4V | - | - | 25.5 | Ω |

### 6.3.3 AC Characteristics 1

$T_{amb}$=-40°C to +85°C, GND=0V, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | nA to nB<br>nB to nA<br>See Figure 7-9 | $V_{CC}$=2.3V to 2.7V | - | - | 0.13 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 0.20 | ns |
| $t_{PZH}$, $t_{PZL}$ | Enable time | $\overline{nOE}$ to nA/nB<br>See Figure 7-10 | $V_{CC}$=2.3V to 2.7V | - | 2.7 | 4.6 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | 2.4 | 4.4 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Disable time | $\overline{nOE}$ to nA/nB<br>See Figure 7-10 | $V_{CC}$=2.3V to 2.7V | - | 2.2 | 3.9 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | 2.9 | 4.2 | ns |

**Note:** All typical values are measured at $V_{CC}$=2.5V/3.3V (unless otherwise specified), and $T_{amb}$=25°C.

### 6.3.4 AC Characteristics 2

$T_{amb}$=-40°C to +125°C, GND=0V, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | nA to nB<br>nB to nA<br>See Figure 7-9 | $V_{CC}$=2.3V to 2.7V | - | - | 0.20 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 0.31 | ns |
| $t_{PZH}$, $t_{PZL}$ | Enable time | $\overline{nOE}$ to nA/nB<br>See Figure 7-10 | $V_{CC}$=2.3V to 2.7V | - | - | 6.0 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 6.0 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Disable time | $\overline{nOE}$ to nA/nB<br>See Figure 7-10 | $V_{CC}$=2.3V to 2.7V | - | - | 5.5 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 5.5 | ns |

# 7 Detailed Description

## 7.1 Overview

CJ74CBTLV3125 is a 4-bit bus single-channel analog switch circuit. Each bit is controlled by the separate enable port (/1OE to /4OE) and enable ports are all Schmitt designed. To ensure the high-impedance OFF-state during power-up or power-down, it is recommended that /nOE connect an external pull-up resistor to $V_{CC}$. When the circuit is in power down state ($V_{CC}$=0V), the control port and the switch port are in high resistance state, which can effectively prevent backflow and circuit damage.

## 7.2 Functional Block Diagram

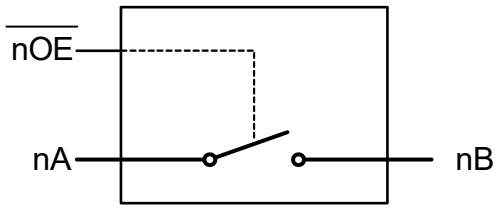



**Figure 7-1 Block diagram**

## 7.3 Function Table(1)

| OUTPUT ENABLE INPUT $\overline{nOE}$ | FUNCTION SWITCH |
|---|---|
| L | ON-state |
| H | OFF-state |

(1) H=HIGH voltage level; L=LOW voltage level.

## 7.4 Testing Circuit

### 7.4.1 ON Resistance Testing Waveform

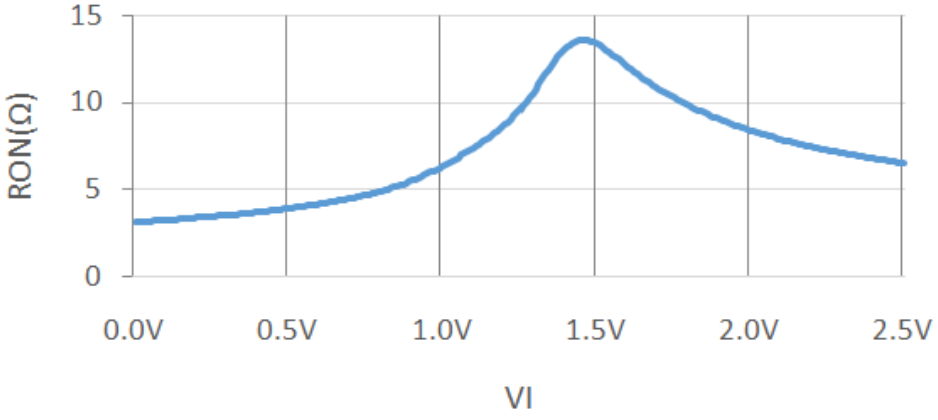



**Figure 7-2 The relation between on resistance and input voltage ($V_{CC}$=2.5V, $I_{SW}$=15mA, $T_{amb}$=25°C)**

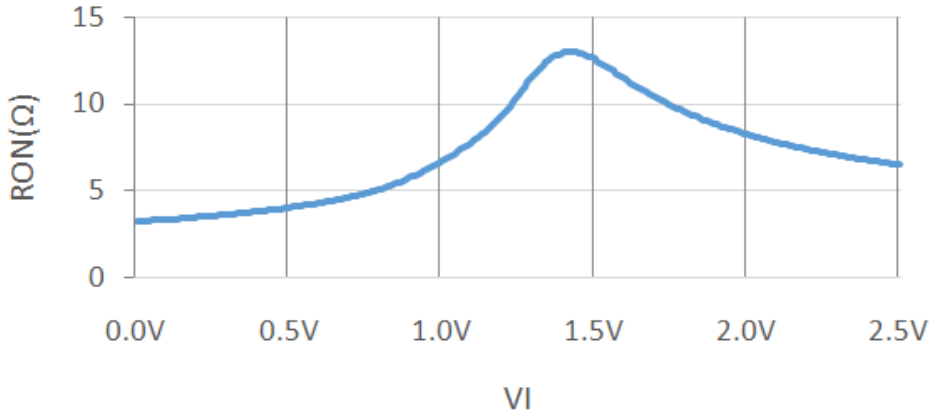



**Figure 7-3 The relation between on resistance and input voltage ($V_{CC}$=2.5V, $I_{SW}$=24mA, $T_{amb}$=25°C)**

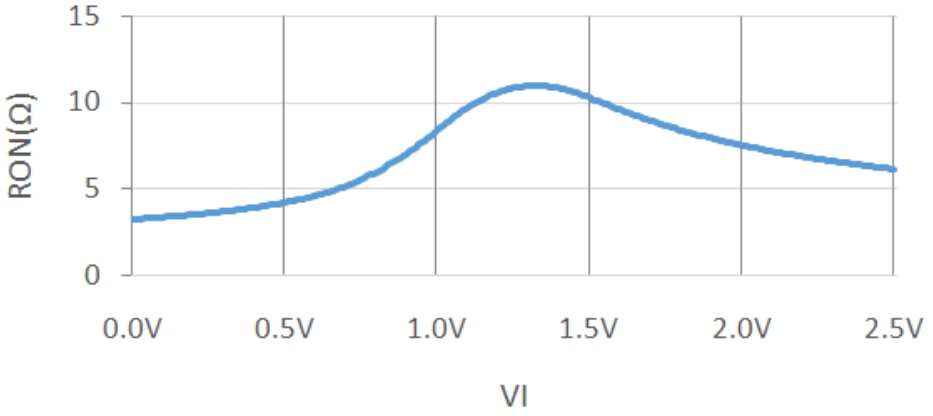



**Figure 7-4 The relation between on resistance and input voltage ($V_{CC}$=2.5V, $I_{SW}$=64mA, $T_{amb}$=25°C)**

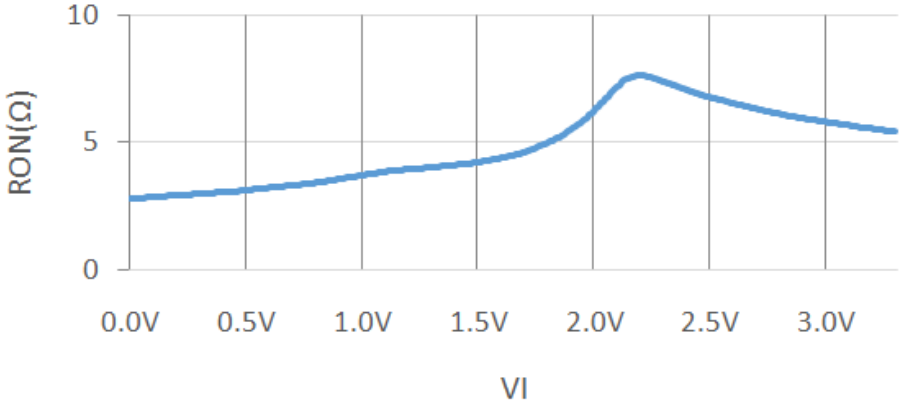



**Figure 7-5 The relation between on resistance and input voltage ($V_{CC}$=3.3V, $I_{SW}$=15mA, $T_{amb}$=25°C)**

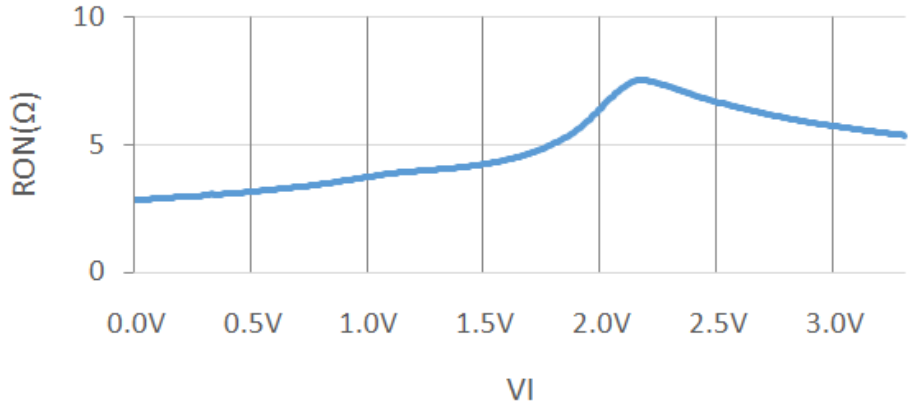



**Figure 7-6 The relation between on resistance and input voltage ($V_{CC}$=3.3V, $I_{SW}$=24mA, $T_{amb}$=25°C)**

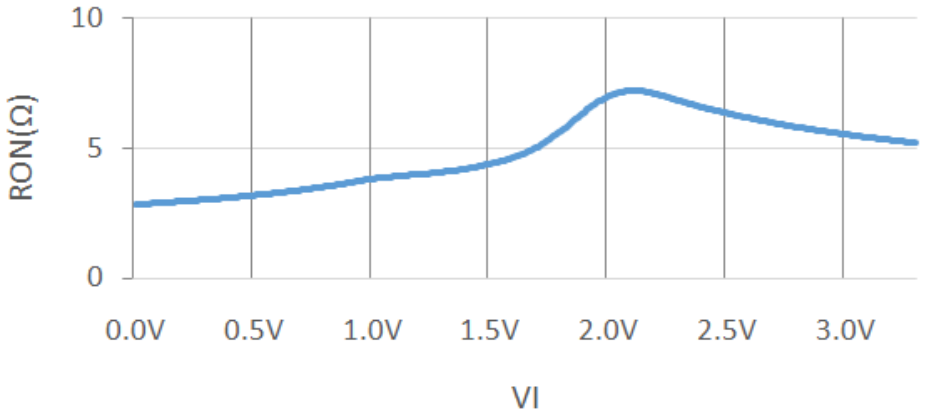



**Figure 7-7 The relation between on resistance and input voltage ($V_{CC}$=3.3V, $I_{SW}$=64mA, $T_{amb}$=25°C)**

### 7.4.2 AC Testing Circuit

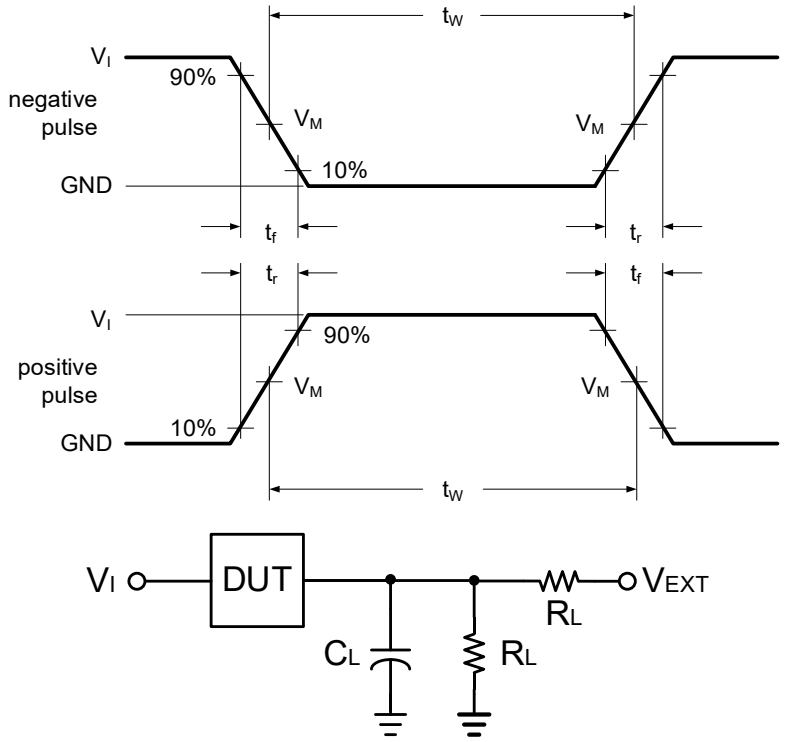



**Figure 7-8 Test circuit for measuring switching times**

Definitions for test circuit:

$R_L$=Load Resistance

$C_L$=Load Capacitance, including capacitors on the probe and clip.

### 7.4.3 AC Testing Waveforms

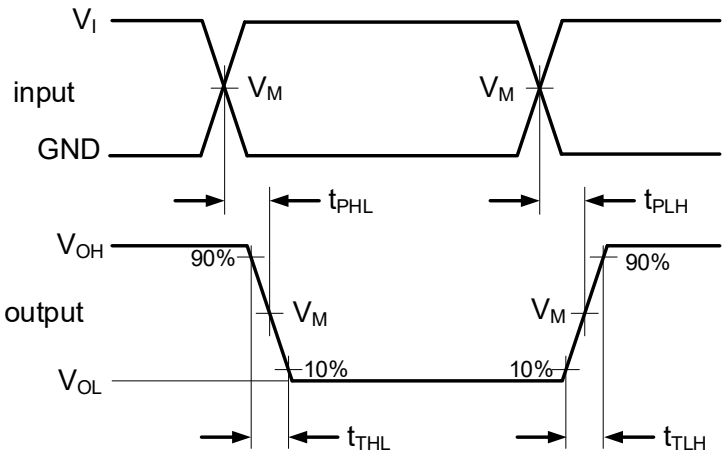



**Figure 7-9 The data input (nA/nB) to output (nB/nA) propagation delays**

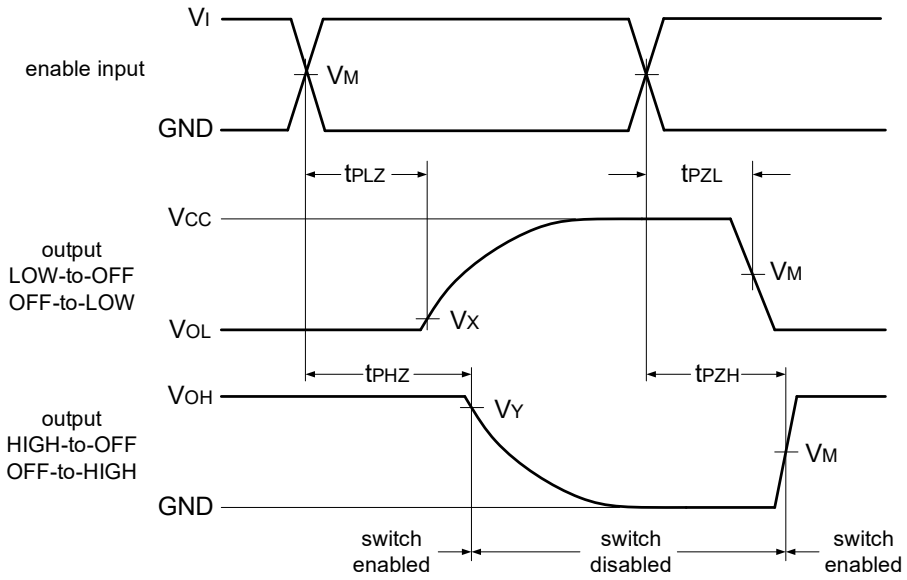



**Figure 7-10 Enable and disable times**

### 7.4.4 Measurement Points

| SUPPLY VOLTAGE | INPUT | | OUTPUT | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 2.3V to 2.7V | $V_{CC}$ | 0.5x$V_{CC}$ | 0.5x$V_{CC}$ | $V_{OL}$+0.15V | $V_{OH}$-0.15V |
| 3.0V to 3.6V | $V_{CC}$ | 0.5x$V_{CC}$ | 0.5x$V_{CC}$ | $V_{OL}$+0.3V | $V_{OH}$-0.3V |

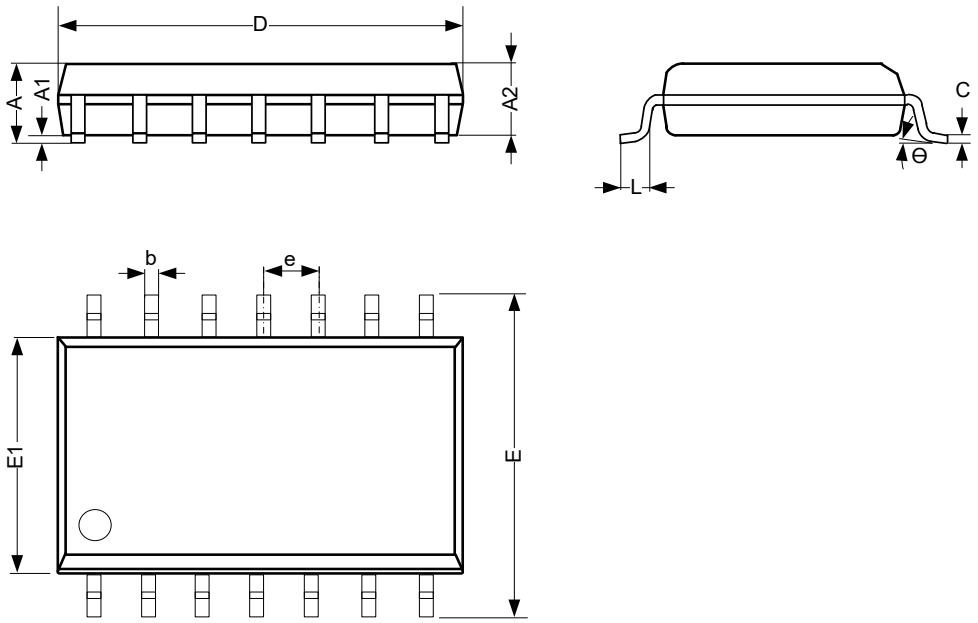
### 7.4.5 Test Data

| SUPPLY VOLTAGE | INPUT | | LOAD | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$ , $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$,$t_{PHL}$ | $t_{PHZ}$,$t_{PZH}$ | $t_{PLZ}$ ,$t_{PZL}$ |
| 2.3V to 2.7V | $V_{CC}$ | ≤ 3.0ns | 30pF | 500Ω | Open | GND | 2x$V_{CC}$ |
| 3.0V to 3.6V | $V_{CC}$ | ≤ 3.0ns | 50pF | 500Ω | Open | GND | 2x$V_{CC}$ |

# 8 Mechanical Information

## 8.1 SOP14 Mechanical Information

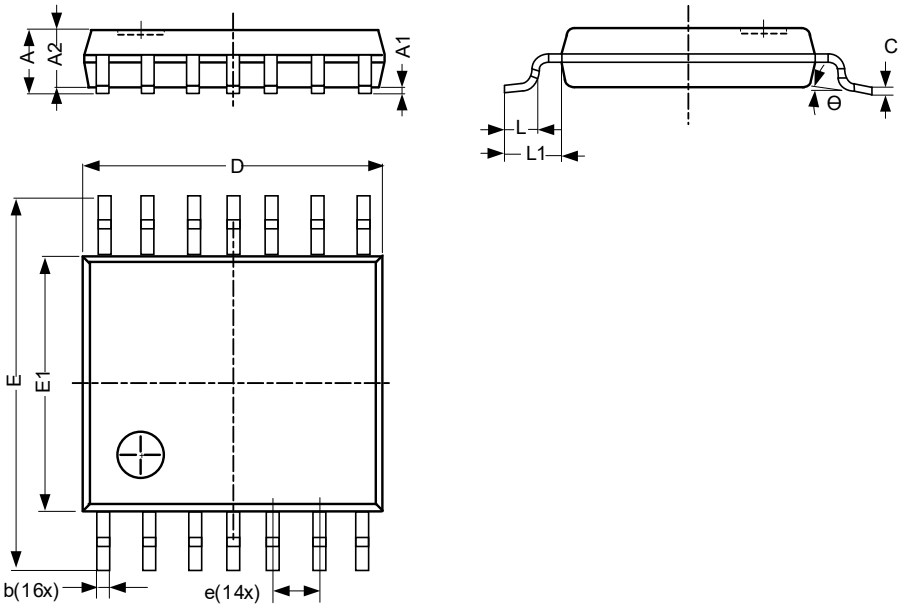
### 8.1.1 SOP14 Outline Dimensions




| SYMBOL | Dimensions In Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 1.50 | - | 1.75 |
| A1 | 0.05 | - | 0.25 |
| A2 | 1.30 | - | - |
| b | 0.33 | - | 0.50 |
| c | 0.19 | - | 0.25 |
| D | 8.43 | - | 8.76 |
| E | 5.80 | - | 6.25 |
| E1 | 3.75 | - | 4.00 |
| e | 1.27 BSC | | |
| L | 0.40 | - | 0.89 |
| Θ | 0° | - | 8° |
| Unit: mm | | | |

## 8.2 TSSOP14 Mechanical Information

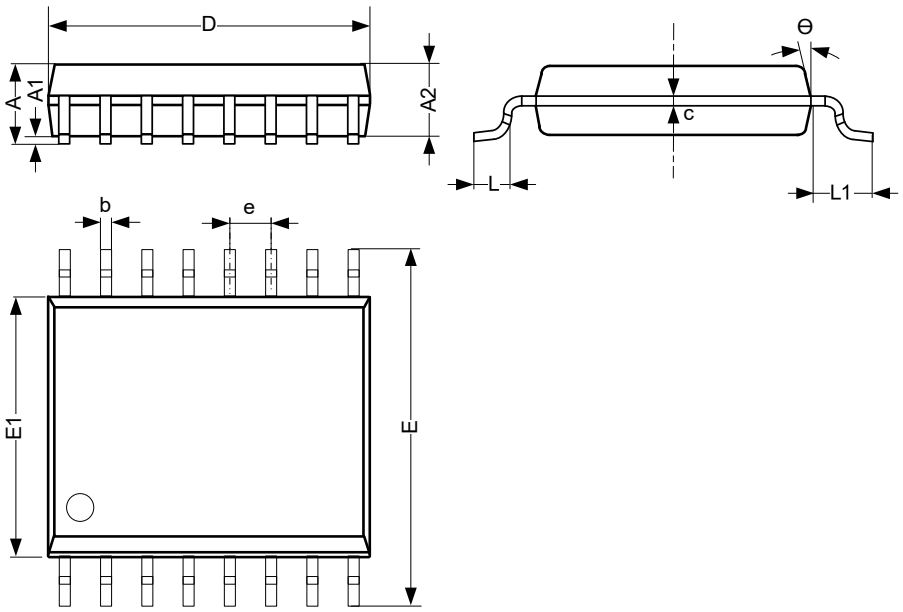
### 8.2.1 TSSOP14 Outline Dimensions




| SYMBOL | Dimensions In Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.80 | - | 1.05 |
| b | 0.19 | - | 0.30 |
| c | 0.09 | - | 0.20 |
| D | 4.90 | - | 5.10 |
| E | 6.20 | - | 6.60 |
| E1 | 4.30 | - | 4.50 |
| e | 0.65 BSC | | |
| L | 0.45 | - | 0.75 |
| L1 | - | 1.00 | - |
| Θ | 0° | - | 8° |
| Unit: mm | | | |

## 8.3 SSOP16 Mechanical Information

### 8.3.1 SSOP16 Outline Dimensions




| SYMBOL | Dimensions In Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | - | 1.75 |
| A1 | 0.02 | - | 0.23 |
| A2 | 1.30 | - | 1.50 |
| b | 0.23 | - | 0.31 |
| c | 0.20 | - | 0.24 |
| D | 4.70 | - | 5.10 |
| E | 5.80 | - | 6.25 |
| E1 | 3.80 | - | 4.02 |
| e | 0.635 BSC | | |
| L | 0.45 | - | 0.80 |
| L1 | 1.05 BSC | | |
| Θ | 0° | - | 8° |
| Unit: mm | | | |

# 9 Notes and Revision History

## 9.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

## 9.2 Notes

**Electrostatic Discharge Caution**

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

# DISCLAIMER

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