Dual Retriggerable Monostable Multivibrator with Reset

CJ74HC/HCT123 Logic

1 Introduction

The CJ74HC/HCT123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL).

The CJ74HC/HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).

2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input (/nA) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ=HIGH, /nQ=LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input /nRD, which also inhibits the triggering.

3. An internal connection from /nRD to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input /nRD.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC123	SOP16
	TSSOP16
CJ74HCT123	SOP16
	TSSOP16

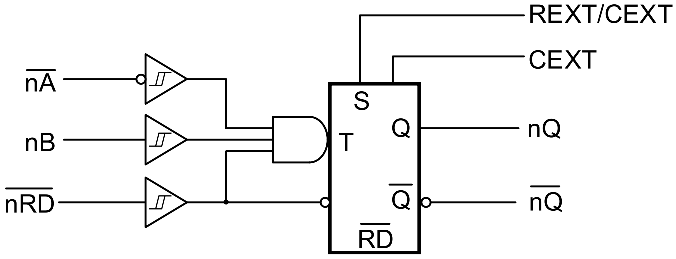
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Specified from -40°C to +125°C

4 Applications

- Blu-ray Players and Home Theaters
- Digital Video Cameras (DVC)
- GPS: Personal Navigation Devices
- Wireless Headsets, Keyboard, and Mice



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC123AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT123AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC123BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74HCT123BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

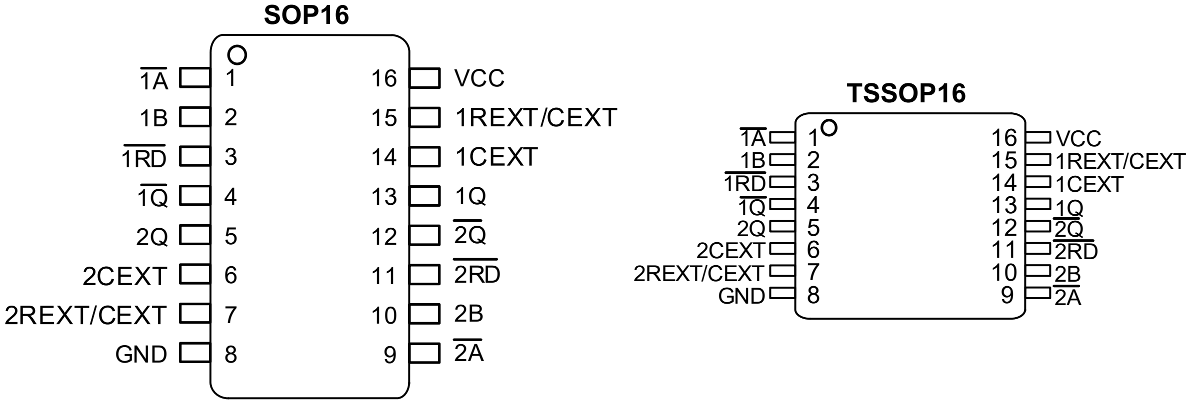


Figure 6-1 Pin configuration

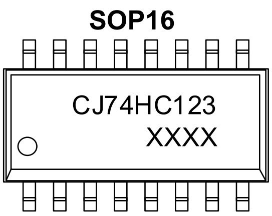
6.2 Pin Function

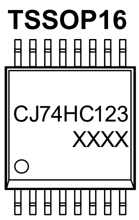
PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	$\overline{1A}$	I	Negative-edge triggered input 1
2	1B	I	Positive-edge triggered input 1
3	$\overline{1RD}$	I	Direct reset LOW and positive-edge triggered input 1
4	$\overline{1Q}$	O	Active LOW output 1
5	2Q	O	Active HIGH output 2
6	2CEXT	-	External capacitor connection 2
7	2REXT/CEXT	-	External resistor and capacitor connection 2
8	GND	G	Ground (0V)
9	$\overline{2A}$	I	Negative-edge triggered input 2
10	2B	I	Positive-edge triggered input 2
11	$\overline{2RD}$	I	Direct reset LOW and positive-edge triggered input 2
12	$\overline{2Q}$	O	Active LOW output 2
13	1Q	O	Active HIGH output 1
14	1CEXT	-	External capacitor connection 1
15	1REXT/CEXT	-	External resistor and capacitor connection 1
16	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground.

6.3 Marking Information

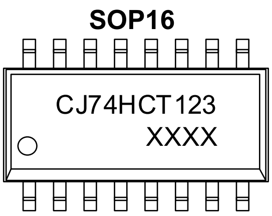
6.3.1 CJ74HC123

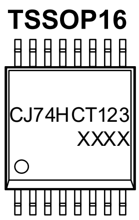




XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT123





XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-	-0.5	+7.0	V
I_{IK}	Input clamping current	V_I < -0.5V or V_I > V_{CC}+0.5V	-	±20	mA
I_{OK}	Output clamping current	V_O < -0.5V or V_O > V_{CC}+0.5V	-	±20	mA
I_O	Output current	Except for pins nREXT/CEXT; V_O= -0.5V to (V_{CC}+0.5V)	-	±25	mA
I_{CC}	Supply current	-	-	50	mA
I_{GND}	Ground current	-	-	-50	mA
T_{stg}	Storage temperature	-	-65	+150	°C
P_{tot}	Total power dissipation	-	-	500	mW
T_L	Soldering temperature	10s SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC123						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	$\overline{nRD}$ input, V_{CC}=2.0V	-	-	625	ns/V
		$\overline{nRD}$ input, V_{CC}=4.5V	-	1.67	139	ns/V
		$\overline{nRD}$ input, V_{CC}=6.0V	-	-	83	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT123						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	$\overline{nRD}$ input, V_{CC}=2.0V	-	-	-	ns/V
		$\overline{nRD}$ input, V_{CC}=4.5V	-	1.67	139	ns/V
		$\overline{nRD}$ input, V_{CC}=6.0V	-	-	-	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±4000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC123							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
C_I	Input capacitance	-		-	3.5	-	pF
CJ74HCT123							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	0	0.1	V
			I_O=4mA	-	0.15	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	8.0	uA

ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	pins $\overline{nA}$, nB	-	35	125	uA
			pin $\overline{nRD}$	-	50	180	uA
C_I	Input capacitance	-		-	3.5	-	pF

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC123							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
CJ74HCT123							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=4mA	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at V_{CC} or	pins $\overline{nA}$, nB	-	-	160	uA
			pin $\overline{nRD}$	-	-	225	uA

		GND; V_{CC}=4.5V to 5.5V; I_O=0A					

7.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC123							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
CJ74HCT123							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=4mA	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	pins $\overline{nA}$, nB	-	-	170	uA
			pin $\overline{nRD}$	-	-	245	uA

7.4.4 AC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V); C_L=50pF, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC123							
t_{pd}	Propagation delay	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6 (1)	V_{CC}=2.0V	-	83	255	ns
			V_{CC}=4.5V	-	30	51	ns
			V_{CC}=5.0V; C_L=15pF	-	26	-	ns
			V_{CC}=6.0V	-	24	43	ns
		$\overline{nRD}$ (reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=2.0V	-	66	215	ns
			V_{CC}=4.5V	-	25	43	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
			V_{CC}=6.0V	-	19	37	ns
t_t	Transition time	See Figure 8-6 (1)	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
t_W	Pulse width	$\overline{nA}$ LOW; See Figure 8-7	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		nB HIGH; See Figure 8-7	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		$\overline{nRD}$ LOW; See Figure 8-8	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		nQ HIGH and $\overline{nQ}$ LOW; V_{CC}=5.0V; See Figure 8-7 and Figure 8-8 (2)	C_{EXT}=100nF; R_{EXT}=10kΩ	-	450	-	us
			C_{EXT}=0pF; R_{EXT}=5kΩ	-	75	-	ns
t_{rtrig}	Retrigger time	$\overline{nA}$, nB; C_{EXT}=0pF; R_{EXT}=5kΩ; V_{CC}=5.0V; See Figure 8-7 (3) (4)		-	110	-	ns
R_{EXT}	External timing resistor	See Figure 8-7	V_{CC}=2.0V	10	-	1000	kΩ
			V_{CC}=5.0V	2	-	1000	kΩ
C_{EXT}	External timing capacitor	V_{CC}=5.0V; See Figure 8-9 (4)		-	-	-	pF
C_{PD}	Power dissipation capacitance	Per monostable; V_I=GND to V_{CC} (5)		-	54	-	pF
CJ74HCT123							
t_{PHL}	HIGH to LOW propagation delay	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	30	51	ns
			V_{CC}=5V; C_L=15pF	-	26	-	ns
		$\overline{nRD}$ (reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	27	46	ns
			V_{CC}=5V; C_L=15pF	-	23	-	ns
t_{PLH}	LOW to HIGH	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$;	V_{CC}=4.5V	-	28	51	ns

	propagation delay	C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=5V; C_L=15pF	-	26	-	ns
		$\overline{nRD}$ (reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	23	46	ns
			V_{CC}=5V; C_L=15pF	-	23	-	ns
t_t	Transition time	V_{CC}=4.5V; See Figure 8-6(1)		-	7	15	ns
t_W	Pulse width	V_{CC}=4.5V	$\overline{nA}$ LOW; See Figure 8-7	20	-	-	ns
			nB HIGH; See Figure 8-7	20	-	-	ns
			$\overline{nRD}$ LOW; See Figure 8-8	20	-	-	ns
		nQ HIGH and $\overline{nQ}$ LOW; V_{CC}=5.0V; See Figure 8-7 and Figure 8-8 (2)	C_{EXT}=100nF; R_{EXT}=10kΩ	-	450	-	us
			C_{EXT}=0pF; R_{EXT}=5kΩ	-	75	-	ns
t_{rtrig}	Retrigger time	$\overline{nA}$, nB; C_{EXT}=0pF; R_{EXT}=5kΩ; V_{CC}=5.0V; See Figure 8-7 (3) (4)		-	110	-	ns
R_{EXT}	External timing resistor	V_{CC}=5.0V; See Figure 8-9		2	-	1000	kΩ
C_{EXT}	External timing capacitor	V_{CC}=5.0V; See Figure 8-9(4)		-	-	-	pF
C_{PD}	Power dissipation capacitance	Per monostable; V_I=GND to V_{CC}–1.5V (5)		-	56	-	pF

(1) t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.

(2) For other R_{EXT} and C_{EXT} combinations see Figure 9. If C_{EXT}>10nF, the next formula is valid.
$t_W = K \times R_{EXT} \times C_{EXT}$, where:
t_W=typical output pulse width in ns;
R_{EXT}=external resistor in kΩ; C_{EXT}=external capacitor in pF;
K=constant = 0.45 for V_{CC}=5.0V and 0.55 for V_{CC}=2.0V.
The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7pF.

(3) The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If C_{EXT}>10pF,
the next formula (at V_{CC}=5.0V) for the setup time of a retrigger pulse is valid:
$t_{rtrig} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where:
t_{rtrig}=retrigger time in ns;
C_{EXT}=external capacitor in pF; R_{EXT}=external resistor in kΩ.
The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7pF.

(4) When the device is powered-up, initiate the device via a reset pulse, when C_{EXT}<50pF.

(5) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:
f_i=input frequency in MHz; f_o=output frequency in MHz;
D=duty factor in %; C_L=output load capacitance in pF;
V_{CC}=supply voltage in V;
C_{EXT}=timing capacitance in pF;
$\sum(C_L \times V_{CC}^2 \times f_o)$=sum of outputs.

7.4.5 AC Characteristics 2

T_{amb}=-40°C to +85°C, GND=0V, C_L=50pF, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC123							
t_{pd}	Propagation delay	$\overline{nRD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6(1)	V_{CC}=2.0V	-	-	320	ns
t_{pd}	Propagation delay	$\overline{nRD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6(1)	V_{CC}=4.5V	-	-	64	ns
t_{pd}	Propagation delay	$\overline{nRD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6(1)	V_{CC}=6.0V	-	-	54	ns
t_{pd}	Propagation delay	$\overline{nRD}$ (reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=2.0V	-	-	270	ns
t_{pd}	Propagation delay	$\overline{nRD}$ (reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	-	54	ns
t_{pd}	Propagation delay	$\overline{nRD}$ (reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=6.0V	-	-	46	ns
t_t	Transition time	See Figure 8-6(1)	V_{CC}=2.0V	-	-	95	ns
t_t	Transition time	See Figure 8-6(1)	V_{CC}=4.5V	-	-	19	ns
t_t	Transition time	See Figure 8-6(1)	V_{CC}=6.0V	-	-	16	ns
t_W	Pulse width	$n\overline{A}$ LOW; See Figure 8-7	V_{CC}=2.0V	125	-	-	ns
t_W	Pulse width	$n\overline{A}$ LOW; See Figure 8-7	V_{CC}=4.5V	25	-	-	ns
t_W	Pulse width	$n\overline{A}$ LOW; See Figure 8-7	V_{CC}=6.0V	21	-	-	ns
t_W	Pulse width	nB HIGH; See Figure 8-7	V_{CC}=2.0V	125	-	-	ns
t_W	Pulse width	nB HIGH; See Figure 8-7	V_{CC}=4.5V	25	-	-	ns
t_W	Pulse width	nB HIGH; See Figure 8-7	V_{CC}=6.0V	21	-	-	ns
t_W	Pulse width	$\overline{nRD}$ LOW; See Figure 8-8	V_{CC}=2.0V	125	-	-	ns
t_W	Pulse width	$\overline{nRD}$ LOW; See Figure 8-8	V_{CC}=4.5V	25	-	-	ns
t_W	Pulse width	$\overline{nRD}$ LOW; See Figure 8-8	V_{CC}=6.0V	21	-	-	ns
CJ74HCT123							
t_{PHL}	HIGH to LOW propagation delay	$\overline{nRD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	-	64	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{nRD}$ (reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	-	58	ns
t_{PLH}	LOW to HIGH propagation delay	$\overline{nRD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	-	64	ns
t_{PLH}	LOW to HIGH propagation delay	$\overline{nRD}$ (reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	-	58	ns
t_t	Transition time	V_{CC}=4.5V; See Figure 8-6(1)		-	-	19	ns
t_W	Pulse width	V_{CC}=4.5V	$n\overline{A}$ LOW; See Figure 8-7	25	-	-	ns
t_W	Pulse width	V_{CC}=4.5V	nB HIGH; See Figure 8-7	25	-	-	ns
t_W	Pulse width	V_{CC}=4.5V	$\overline{nRD}$ LOW; See Figure 8-8	25	-	-	ns

(1) t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.

7.4.6 AC Characteristics 3

T_{amb}=-40°C to +125°C, GND=0V, C_L=50pF, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC123							
t_{pd}	Propagation delay	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6(1)	V_{CC}=2.0V	-	-	385	ns
			V_{CC}=4.5V	-	-	77	ns
			V_{CC}=6.0V	-	-	65	ns
		$\overline{nRD}$ (reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=2.0V	-	-	325	ns
			V_{CC}=4.5V	-	-	65	ns
			V_{CC}=6.0V	-	-	55	ns
t_t	Transition time	See Figure 8-6(1)	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
t_W	Pulse width	$\overline{nA}$ LOW; See Figure 8-7	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		nB HIGH; See Figure 8-7	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		$\overline{nRD}$ LOW; See Figure 8-8	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
CJ74HCT123							
t_{PHL}	HIGH to LOW propagation delay	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	-	77	ns
		$\overline{nRD}$ (reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	-	69	ns
t_{PLH}	LOW to HIGH propagation delay	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	-	77	ns
		$\overline{nRD}$ (reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; See Figure 8-6	V_{CC}=4.5V	-	-	69	ns
t_t	Transition time	V_{CC}=4.5V; See Figure 8-6(1)		-	-	22	ns
t_W	Pulse width	V_{CC}=4.5V	$\overline{nA}$ LOW; See Figure 8-7	30	-	-	ns
			nB HIGH; See Figure 8-7	30	-	-	ns
			$\overline{nRD}$ LOW; See Figure 8-8	30	-	-	ns

(1) t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.

8 Detailed Description

8.1 Overview

The CJ74HC/HCT123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL).

The CJ74HC/HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse is programmed by selection of an external resistor (REXT) and capacitor (CEXT).

2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input (/nA) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ=HIGH, /nQ=LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input /nRD, which also inhibits the triggering.

3. An internal connection from /nRD to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input /nRD.

8.2 Functional Block Diagram

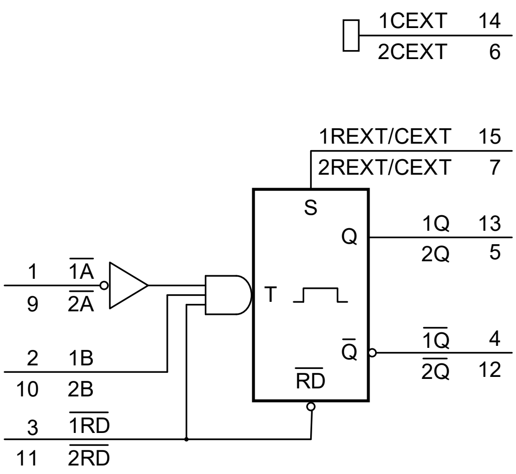


Figure 8-1 Logic symbol

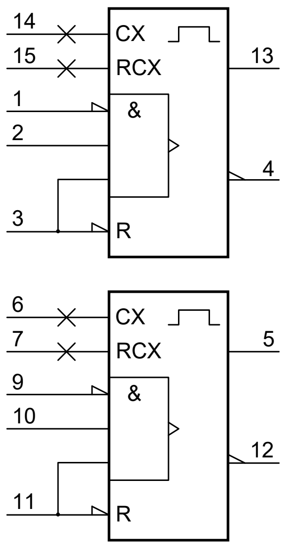


Figure 8-2 IEC logic symbol

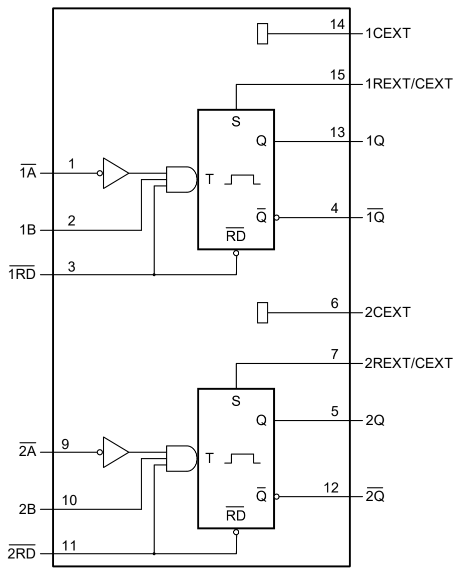


Figure 8-3 Functional diagram

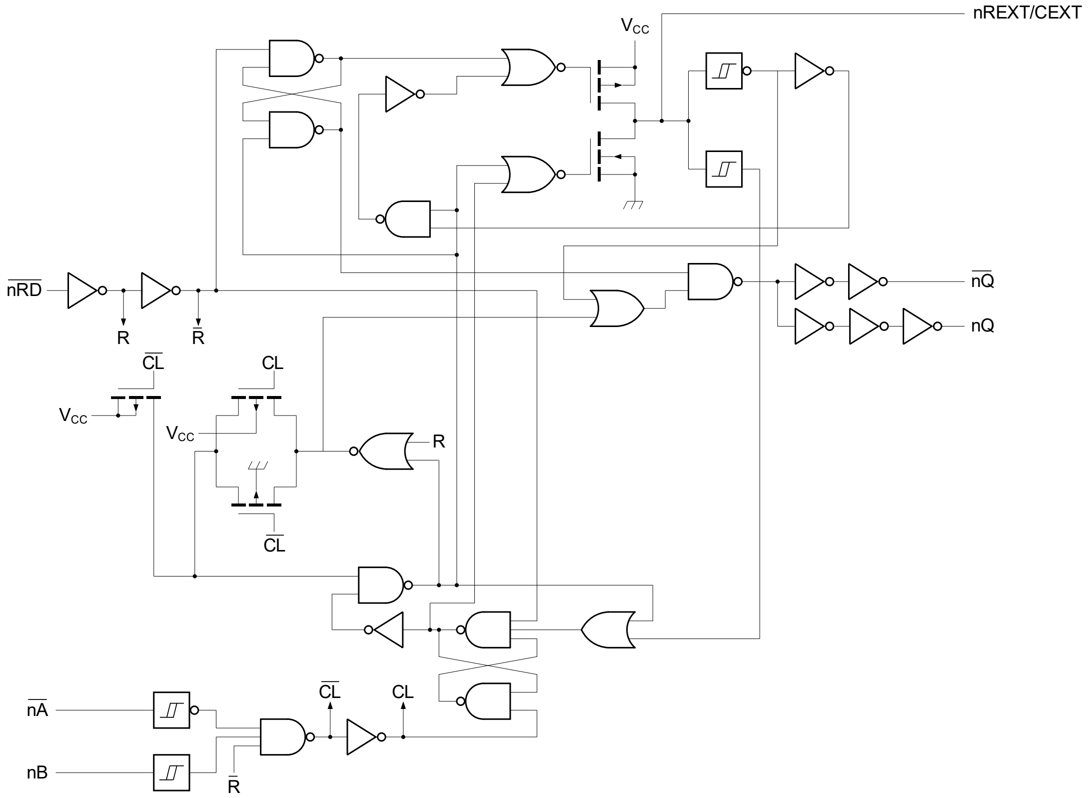
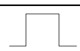
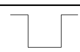
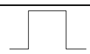
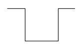
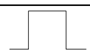
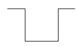


Figure 8-4 Logic diagram

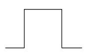
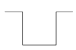
8.3 Function Table

INPUT			OUTPUT	
$\overline{nRD}$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

Note:

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care.

(2) ↑ =LOW-to-HIGH transition; ↓ =HIGH-to-LOW transition.

(3)  =one HIGH level output pulse;  =one LOW level output pulse.

(4) If the monostable was triggered before this condition was established, the pulse will continue as programmed.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

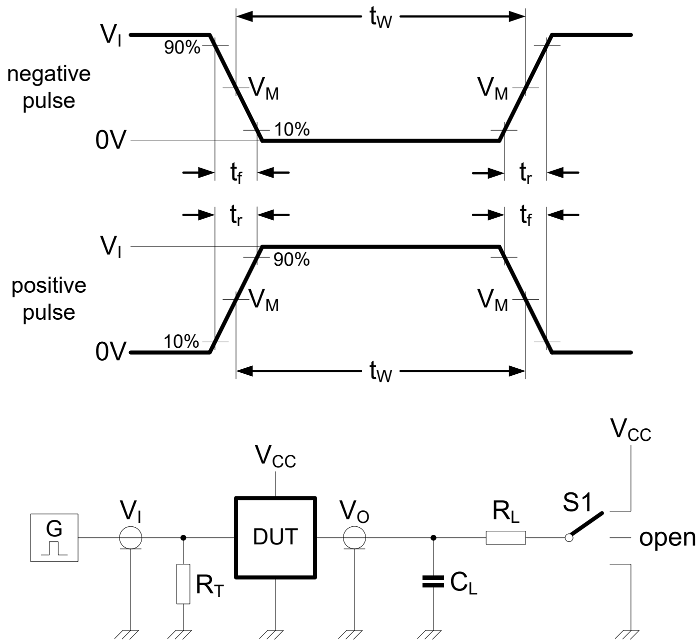


Figure 8-5 Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

8.4.2 AC Testing Waveforms

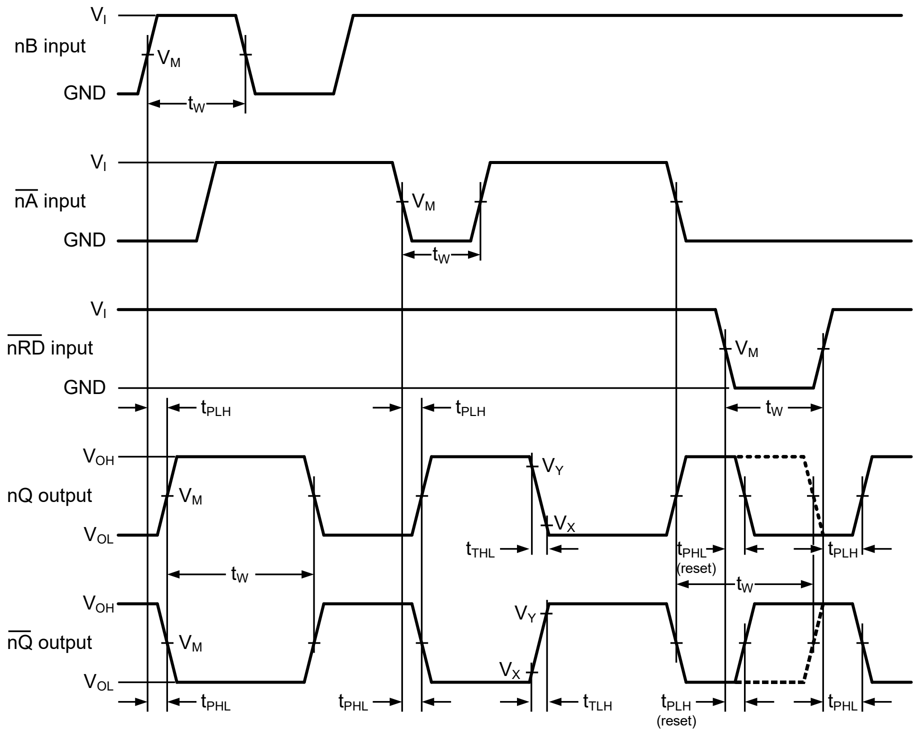


Figure 8-6 Propagation delays from inputs ($\overline{nA}$, nB, $\overline{nRD}$) to outputs (nQ, $\overline{nQ}$) and output transition times

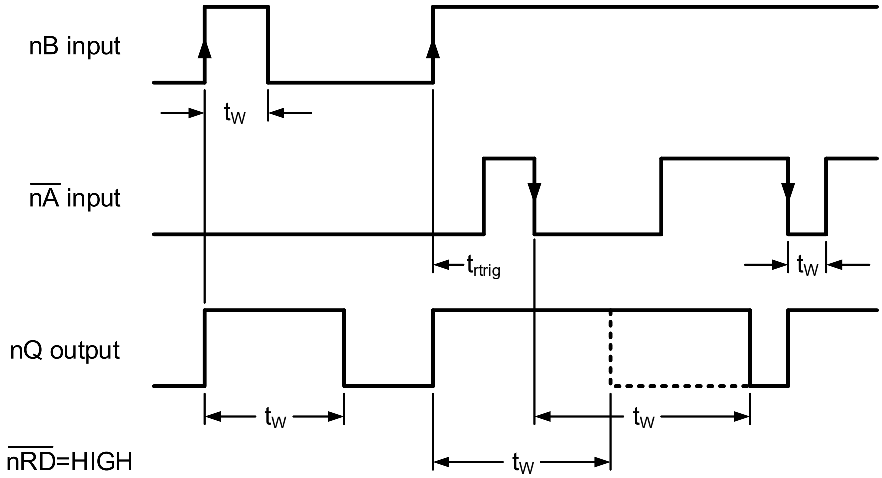


Figure 8-7 Output pulse control using retrigger pulse

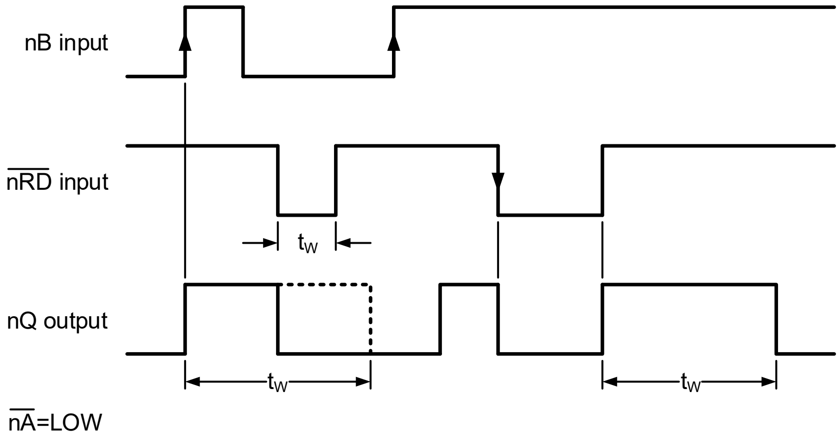


Figure 8-8 Output pulse control using reset input $\overline{nRD}$

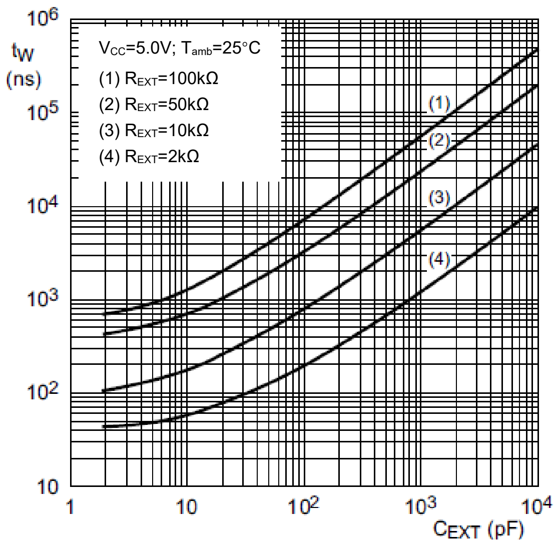
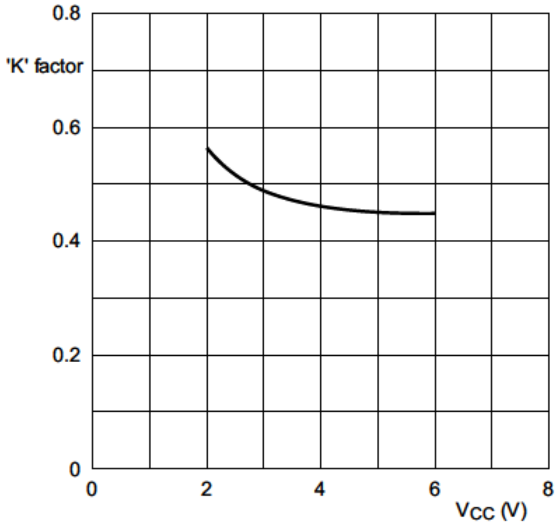


Figure 8-9 Typical output pulse width as a function of the external capacitor value



C_{EXT}=10nF; R_{EXT}=10kΩ to 100kΩ.T_{amb}=25°C

Figure 8-10 CJ74HC123 typical 'K' factor as function of V_{CC}

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT
	V_M	V_M
CJ74HC123	0.5xV_{CC}	0.5xV_{CC}
CJ74HCT123	1.3V	1.3V

8.4.4 Test Data

TYPE	INPUT		LOAD		S1 POSITION
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}
CJ74HC123	V_{CC}	6ns	15pF, 50pF	1kΩ	Open
CJ74HCT123	3V	6ns	15pF, 50pF	1kΩ	Open

9 Typical Application Circuit and Application Note

9.1 Timing Component Connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.

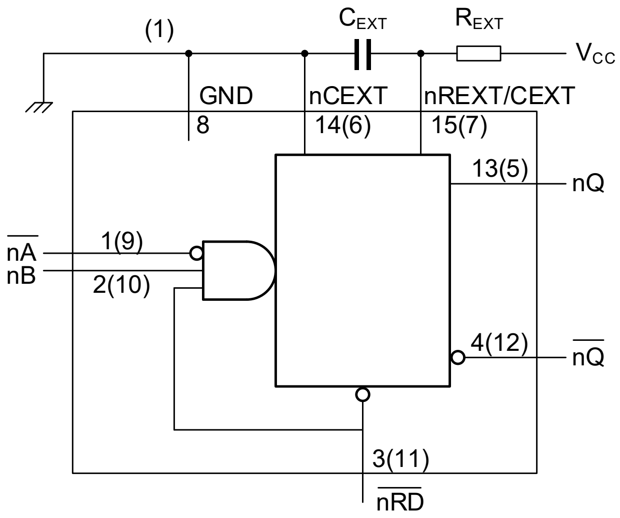


Figure 9-1 Timing component connections

(1) For minimum noise generation it is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

9.2 Power-up Considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT}. This output pulse can be eliminated using the circuit shown in Figure 9-2.

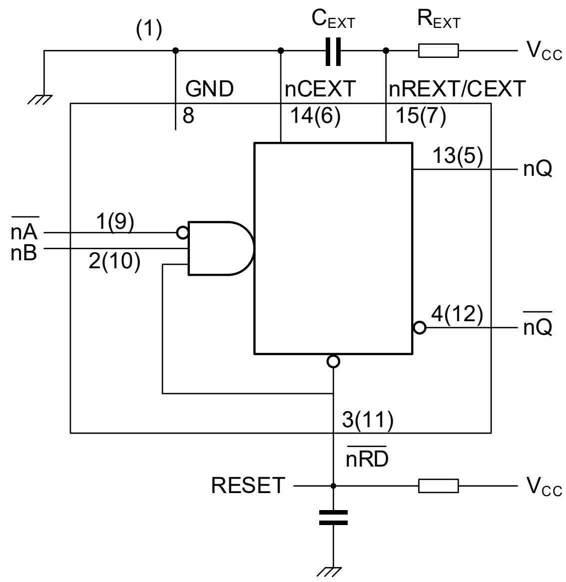


Figure 9-2 Power-up output pulse elimination circuit

9.3 Power-down Considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 9-3.

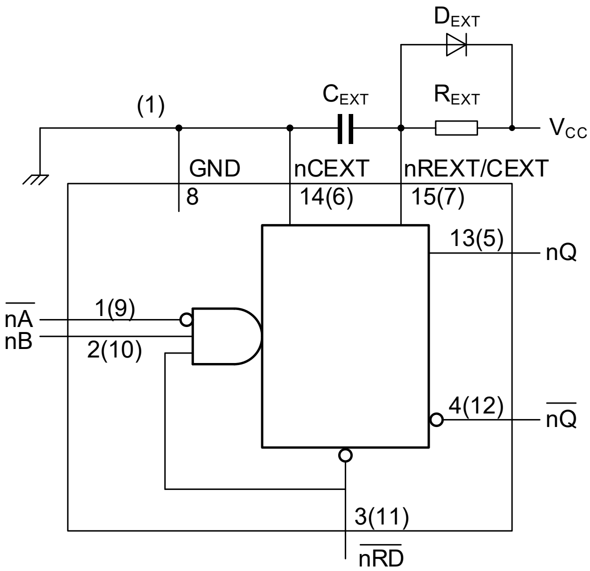
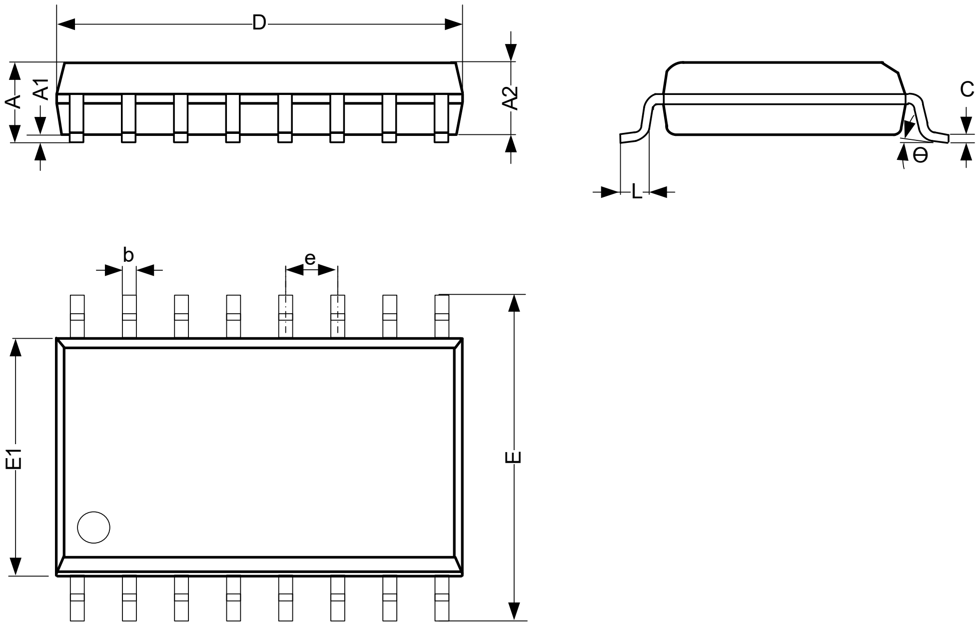


Figure 9-3 Power-down protection circuit

10 Mechanical Information

10.1 SOP16 Mechanical Information

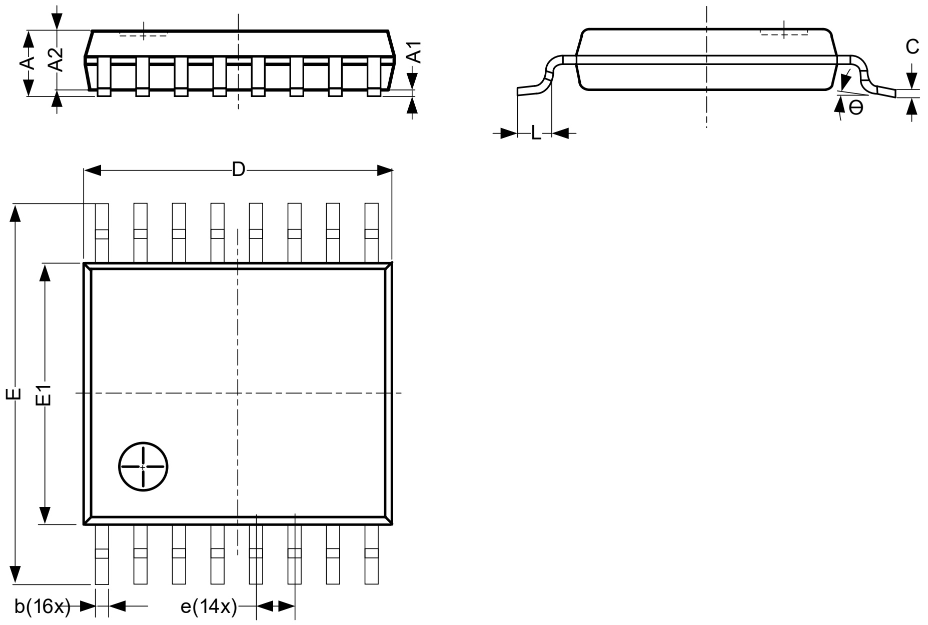
10.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	**Typ.**	**Max.**
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
Θ	0°	-	8°
Unit: mm			

10.2 TSSOP16 Mechanical Information

10.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

11 Notes and Revision History

11.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

11.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

Official Website: www.jscj-elec.com

Copyright © JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD