8-bit Parallel-in/Serial-out Shift Register

CJ74HC/HCT166 Logic

1 Introduction

The CJ74HC/HCT166 is an 8-bit serial or parallel-in/serial-out shift register.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC166	SOP16
	TSSOP16
CJ74HCT166	SOP16
	TSSOP16

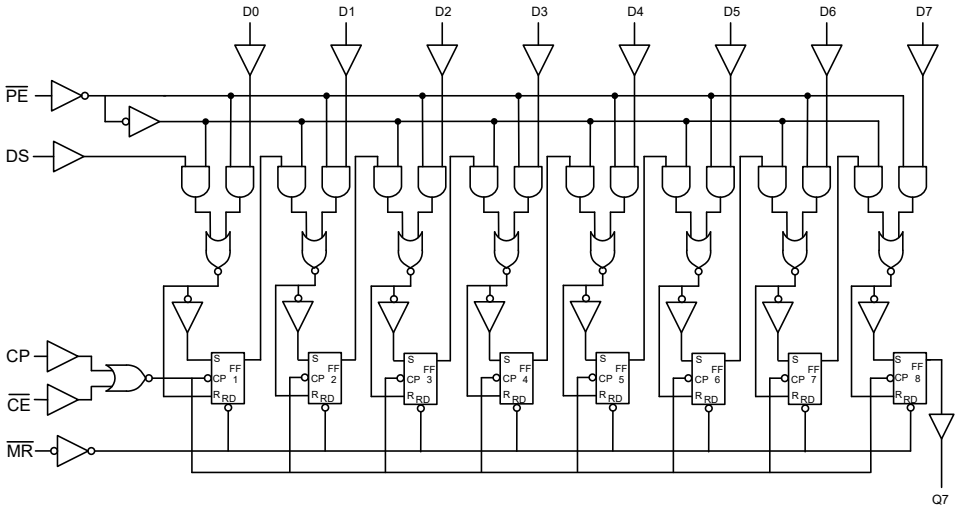
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Supply voltage range:
  - CJ74HC166: 2~6V
  - CJ74HCT166: 4.5~5.5V
- Input levels:
  - CJ74HC166: CMOS level
  - CJ74HCT166: TTL level
- Temperature range: -40°C to +125°C

4 Applications

- Increase number of inputs/outputs to a microcontroller



Logic symbol

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC166AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT166AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC166BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74HCT166BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

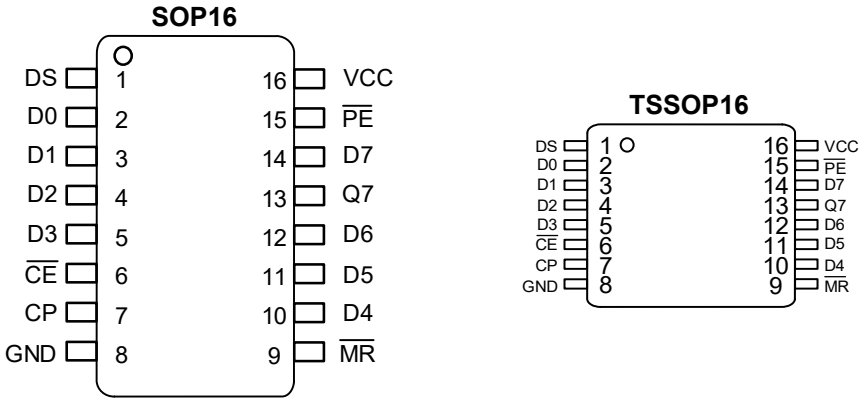


Figure 6-1 Pin configuration

6.2 Pin Function

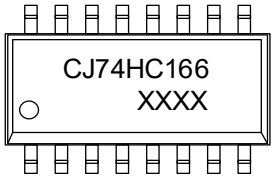
PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	DS	I	Serial data input
2	D0	I	Parallel data input
3	D1	I	Parallel data input
4	D2	I	Parallel data input
5	D3	I	Parallel data input
6	$\overline{CE}$	I	Clock enable input (active LOW)
7	CP	I	Clock input (LOW-to-HIGH edge-triggered)
8	GND	G	Ground (0V)
9	$\overline{MR}$	I	Asynchronous master reset (active LOW)
10	D4	I	Parallel data input
11	D5	I	Parallel data input
12	D6	I	Parallel data input
13	Q7	O	Serial output from the last stage
14	D7	I	Parallel data input
15	$\overline{PE}$	I	Parallel enable input (active LOW)
16	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

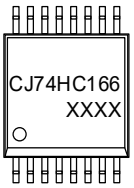
6.3 Marking Information

6.3.1 CJ74HC166

SOP16



TSSOP16



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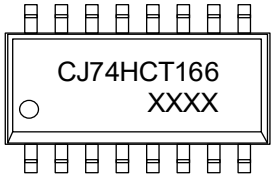
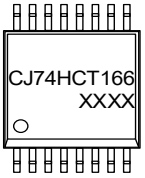
6.3.2 CJ74HCT166

SOP16



TSSOP16



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7	V
I_{CC}	Supply current	-		-	50	mA
I_{GND}	Ground current	-		-50	-	mA
I_{IK}	Input clamping current	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
I_{OK}	Output clamping current	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
I_O	Output current	-0.5V < V_O < V_{CC}+0.5V		-	±25	mA
T_{stg}	Storage temperature	-		-65	+150	°C
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC166						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT166						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC166						
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V	1.5	-	-	V
		V_{CC}=4.5V	3.15	-	-	V
		V_{CC}=6.0V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_{CC}=2.0V; I_O=-20uA	1.9	2.0	-	V
		V_{CC}=4.5V; I_O=-20uA	4.4	4.5	-	V
		V_{CC}=6.0V; I_O=-20uA	5.9	6.0	-	V
		V_{CC}=4.5V; I_O=-4.0mA	3.84	4.32	-	V
		V_{CC}=6.0V; I_O=-5.2mA	5.34	5.81	-	V
V_{OL}	LOW-level output voltage	V_{CC}=2.0V; I_O=20uA	-	0	0.1	V
		V_{CC}=4.5V; I_O=20uA	-	0	0.1	V
		V_{CC}=6.0V; I_O=20uA	-	0	0.1	V
		V_{CC}=4.5V; I_O=4.0mA	-	0.15	0.33	V
		V_{CC}=6.0V; I_O=5.2mA	-	0.16	0.33	V
I_I	Input leakage current	V_{CC}=6.0V; V_I=V_{CC} or GND	-	-	±1	uA
I_{CC}	Supply current	V_{CC}=6.0V; V_I=V_{CC} or GND;I_O=0A	-	-	80	uA
CJ74HCT166						
V_{IH}	HIGH-level input voltage	V_{CC}=4.5 to 5.5V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5 to 5.5V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC}=4.5V; I_O=-20uA	4.4	4.5	-	V
		V_{CC}=4.5V; I_O=-4.0mA	3.84	4.32	-	V
V_{OL}	LOW-level output voltage	V_{CC}=4.5V; I_O=20uA	-	0	0.1	V
		V_{CC}=4.5V; I_O=5.2mA	-	0.16	0.33	V
I_I	Input leakage current	V_{CC}=5.5V; V_I=V_{CC} or GND	-	-	±1	uA
I_{CC}	Supply current	V_{CC}=4.5V; V_I=V_{CC} or GND; I_O=0A	-	-	80	uA
ΔI_{CC}	Additional supply current	V_{CC}=4.5 to 5.5V; One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A	-	-	135	uA

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC166						
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V	1.5	-	-	V
		V_{CC}=4.5V	3.15	-	-	V
		V_{CC}=6.0V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_{CC}=2.0V; I_O=-20uA	1.9	-	-	V
		V_{CC}=4.5V; I_O=-20uA	4.4	-	-	V
		V_{CC}=6.0V; I_O=-20uA	5.9	-	-	V
		V_{CC}=4.5V; I_O=-4.0mA	3.7	-	-	V
		V_{CC}=6.0V; I_O=-5.2mA	5.2	-	-	V
V_{OL}	LOW-level output voltage	V_{CC}=2.0V; I_O=20uA	-	-	0.1	V
		V_{CC}=4.5V; I_O=20uA	-	-	0.1	V
		V_{CC}=6.0V; I_O=20uA	-	-	0.1	V
		V_{CC}=4.5V; I_O=4.0mA	-	-	0.4	V
		V_{CC}=6.0V; I_O=5.2mA	-	-	0.4	V
I_I	Input leakage current	V_{CC}=6.0V; V_I=V_{CC} or GND	-	-	±1	uA
I_{CC}	Supply current	V_{CC}=6.0V; V_I=V_{CC} or GND; I_O=0A	-	-	160	uA
CJ74HCT166						
V_{IH}	HIGH-level input voltage	V_{CC}=4.5 to 5.5V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5 to 5.5V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC}=4.5V; I_O=-20uA	4.4	-	-	V
		V_{CC}=4.5V; I_O=-4.0mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_{CC}=4.5V; I_O=20uA	-	-	0.1	V
		V_{CC}=4.5V; I_O=5.2mA	-	-	0.4	V
I_I	Input leakage current	V_{CC}=5.5V; V_I=V_{CC} or GND	-	-	±1	uA
I_{CC}	Supply current	V_{CC}=4.5V;V_I=V_{CC} or GND; I_O=0A	-	-	160	uA
ΔI_{CC}	Additional supply current	V_{CC}=4.5 to 5.5V; One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A	-	-	147	uA

7.4.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC166							
t_{PLH}, t_{PHL}	CP to Q7 propagation delay	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	50	190	ns
			V_{CC}=4.5V; C_L=50pF	-	18	38	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V; C_L=50pF	-	14	33	ns
	$\overline{MR}$ to Q7 propagation delay	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	-	47	200	ns
			V_{CC}=4.5V; C_L=50pF	-	17	40	ns
			V_{CC}=5.0V; C_L=15pF	-	14	-	ns
			V_{CC}=6.0V; C_L=50pF	-	14	34	ns
t_{THL}, t_{TLH}	Transition time	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	19	95	ns
			V_{CC}=4.5V; C_L=50pF	-	7	19	ns
			V_{CC}=6.0V; C_L=50pF	-	6	16	ns
t_w	CP input HIGH or LOW pulse width	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	100	-	-	ns
			V_{CC}=4.5V; C_L=50pF	20	-	-	ns
			V_{CC}=6.0V; C_L=50pF	17	-	-	ns
	$\overline{MR}$ input LOW pulse width	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	125	-	-	ns
			V_{CC}=4.5V; C_L=50pF	25	-	-	ns
			V_{CC}=6.0V; C_L=50pF	21	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	0	-	-	ns
			V_{CC}=4.5V; C_L=50pF	0	-	-	ns
			V_{CC}=6.0V; C_L=50pF	0	-	-	ns
t_{su}	Dn、$\overline{CE}$ to CP set_up time	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	100	-	-	ns
			V_{CC}=4.5V; C_L=50pF	20	-	-	ns
			V_{CC}=6.0V; C_L=50pF	17	-	-	ns
	$\overline{PE}$ to CP set_up time		V_{CC}=2.0V; C_L=50pF	125	-	-	ns
			V_{CC}=4.5V; C_L=50pF	25	-	-	ns
			V_{CC}=6.0V; C_L=50pF	21	-	-	ns
t_h	Dn、$\overline{CE}$ to CP hold time	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	2	-	-	ns
			V_{CC}=4.5V; C_L=50pF	2	-	-	ns
			V_{CC}=6.0V; C_L=50pF	2	-	-	ns
	$\overline{PE}$ to CP hold time		V_{CC}=2.0V; C_L=50pF	0	-	-	ns
			V_{CC}=4.5V; C_L=50pF	0	-	-	ns
			V_{CC}=6.0V; C_L=50pF	0	-	-	ns
f_{max}	Maximum frequency	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	4.8	19	-	MHz
			V_{CC}=4.5V; C_L=50pF	24	57	-	MHz

			V_{CC}=5.0V; C_L=15pF	-	63	-	MHz
			V_{CC}=6.0V; C_L=50pF	28	68	-	MHz
CJ74HCT166							
t_{PLH}, t_{PHL}	CP to Q7 propagation delay	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	23	50	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
	$\overline{MR}$ to Q7 propagation delay	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	-	22	50	ns
			V_{CC}=5.0V; C_L=15pF	-	19	-	ns
t_{THL}, t_{TLH}	Transition time	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	7	19	ns
t_w	CP input HIGH or LOW pulse width	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	25	-	-	ns
	$\overline{MR}$ input LOW pulse width	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	31	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	0	-	-	ns
t_{su}	Dn、$\overline{CE}$ to CP set_up time	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	20	-	-	ns
	$\overline{PE}$ to CP set_up time		V_{CC}=4.5V; C_L=50pF	38	-	-	ns
t_h	Dn、$\overline{CE}$ to CP hold time	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	0	-	-	ns
	$\overline{PE}$ to CP hold time		V_{CC}=4.5V; C_L=50pF	0	-	-	ns
f_{max}	Maximum frequency	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	20	45	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	50	-	MHz

7.4.4 AC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC166							
t_{PLH}, t_{PHL}	CP to Q7 propagation delay	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	-	225	ns
			V_{CC}=4.5V; C_L=50pF	-	-	45	ns
			V_{CC}=6.0V; C_L=50pF	-	-	38	ns
	$\overline{MR}$ to Q7 propagation delay	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	-	-	240	ns
			V_{CC}=4.5V; C_L=50pF	-	-	48	ns
			V_{CC}=6.0V; C_L=50pF	-	-	41	ns
t_{THL}, t_{TLH}	Transition time	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	-	110	ns
			V_{CC}=4.5V; C_L=50pF	-	-	22	ns
			V_{CC}=6.0V; C_L=50pF	-	-	19	ns
t_w	CP input HIGH or LOW pulse width	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	120	-	-	ns
			V_{CC}=4.5V; C_L=50pF	24	-	-	ns
			V_{CC}=6.0V; C_L=50pF	20	-	-	ns
	$\overline{MR}$ input LOW pulse width	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	150	-	-	ns
			V_{CC}=4.5V; C_L=50pF	30	-	-	ns
			V_{CC}=6.0V; C_L=50pF	26	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	0	-	-	ns

			V_{CC}=4.5V; C_L=50pF	0	-	-	ns
			V_{CC}=6.0V; C_L=50pF	0	-	-	ns
t_{su}	Dn、$\overline{CE}$ to CP set_up time	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	120	-	-	ns
			V_{CC}=4.5V; C_L=50pF	24	-	-	ns
			V_{CC}=6.0V; C_L=50pF	20	-	-	ns
	$\overline{PE}$ to CP set_up time		V_{CC}=2.0V; C_L=50pF	150	-	-	ns
			V_{CC}=4.5V; C_L=50pF	30	-	-	ns
			V_{CC}=6.0V; C_L=50pF	26	-	-	ns
t_h	Dn、$\overline{CE}$ to CP hold time	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	2	-	-	ns
			V_{CC}=4.5V; C_L=50pF	2	-	-	ns
			V_{CC}=6.0V; C_L=50pF	2	-	-	ns
	$\overline{PE}$ to CP hold time		V_{CC}=2.0V; C_L=50pF	0	-	-	ns
			V_{CC}=4.5V; C_L=50pF	0	-	-	ns
			V_{CC}=6.0V; C_L=50pF	0	-	-	ns
f_{max}	Maximum frequency	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	4	-	-	MHz
			V_{CC}=4.5V; C_L=15pF	20	-	-	MHz
			V_{CC}=6.0V; C_L=50pF	24	-	-	MHz
CJ74HCT166							
t_{PLH}, t_{PHL}	CP to Q7 propagation delay	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	-	60	ns
	$\overline{MR}$ to Q7 propagation delay	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	-	-	60	ns
t_{THL}, t_{TLH}	Transition time	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	-	22	ns
t_w	CP input HIGH or LOW pulse width	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	30	-	-	ns
	$\overline{MR}$ input LOW pulse width	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	38	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	0	-	-	ns
t_{su}	Dn、$\overline{CE}$ to CP set_up time	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	24	-	-	ns
	$\overline{PE}$ to CP set_up time		V_{CC}=4.5V; C_L=50pF	45	-	-	ns
t_h	Dn、$\overline{CE}$ to CP hold time	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	0	-	-	ns
	$\overline{PE}$ to CP hold time		V_{CC}=4.5V; C_L=50pF	0	-	-	ns
f_{max}	Maximum frequency	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	17	-	-	MHz

8 Detailed Description

8.1 Overview

The CJ74HC/HCT166 is an 8-bit serial or parallel-in/serial-out shift register.

8.2 Functional Block Diagram

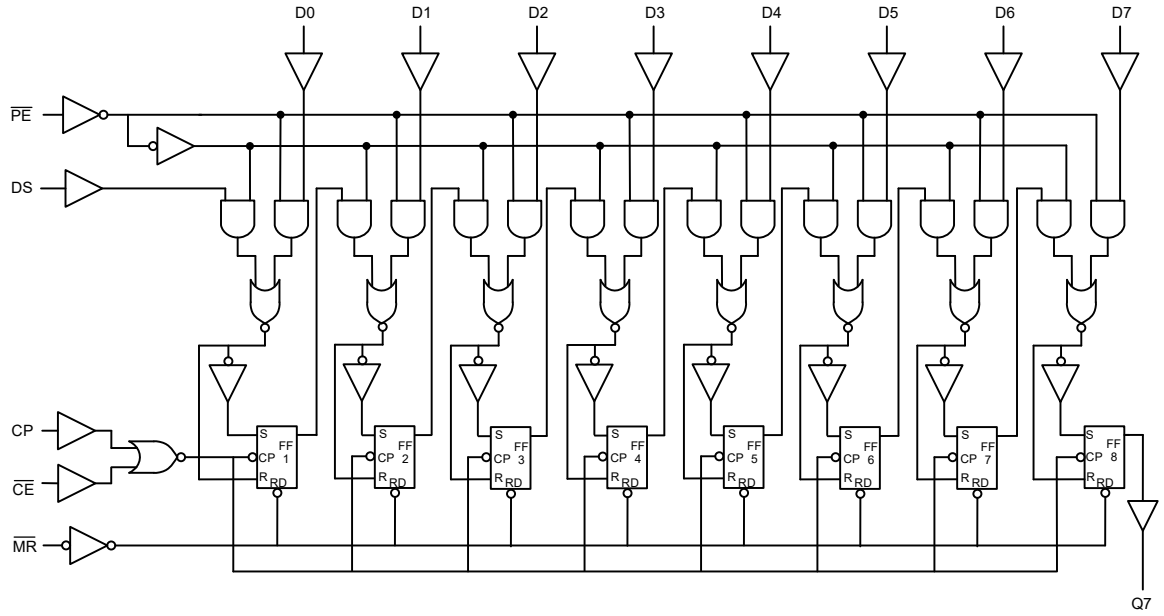


Figure 8-1 Logic symbol

8.3 Function Table

OPERATING MODES	INPUTS					Qn REGISTERS		OUTPUT
	$\overline{PE}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7
Parallel load	l	l	↑	X	l	L	L to L	L
	l	l	↑	X	h	H	H to H	H
Serial shift	h	l	↑	l	X	L	q0 to q5	q6
	h	l	↑	h	X	H	q0 to q5	q6
Hold “do nothing”	X	H	X	X	X	q0	q1 to q6	q7

Note:

(1) H = HIGH voltage level;

(2) h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

(3) L = LOW voltage level;

(4) l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

(5) q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;

(6) X = don’t care;

(7) ↑ = LOW-to-HIGH clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

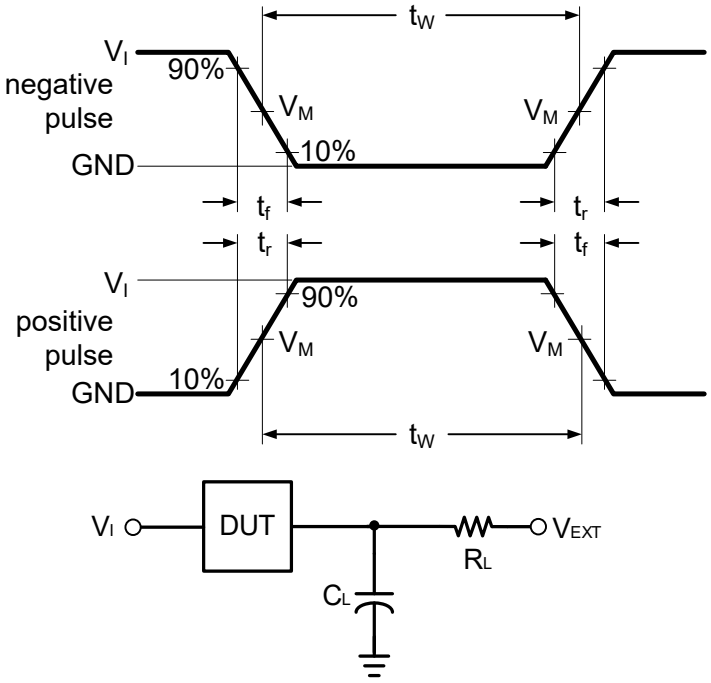


Figure 8-2 Test circuit for measuring switching times

Definitions for test circuit:

C_L includes probe and jig capacitance.

8.4.2 AC Testing Waveforms

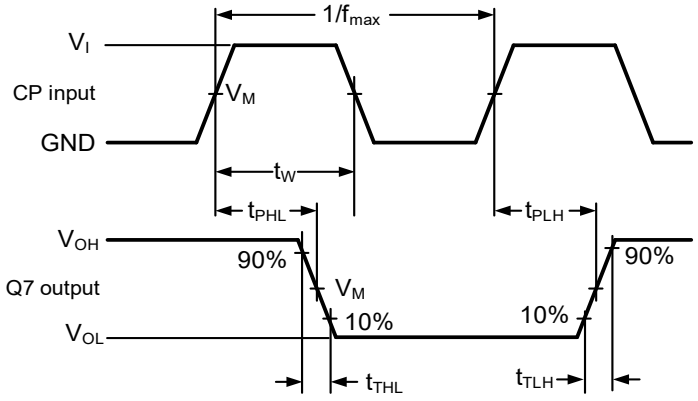


Figure 8-3 Clock (CP) to output (Q7) propagation delays, pulse width, output transition times and maximum frequency

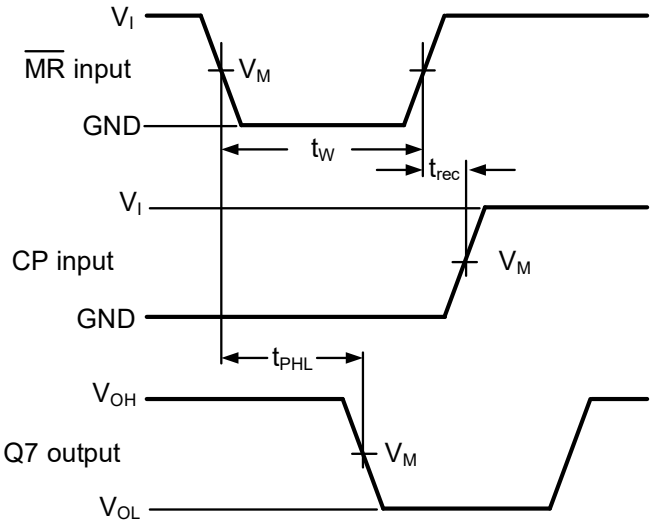


Figure 8-4 Master reset ($\overline{MR}$) pulse width, $\overline{MR}$ to output (Q7) propagation delay and $\overline{MR}$ to clock (CP) recovery time

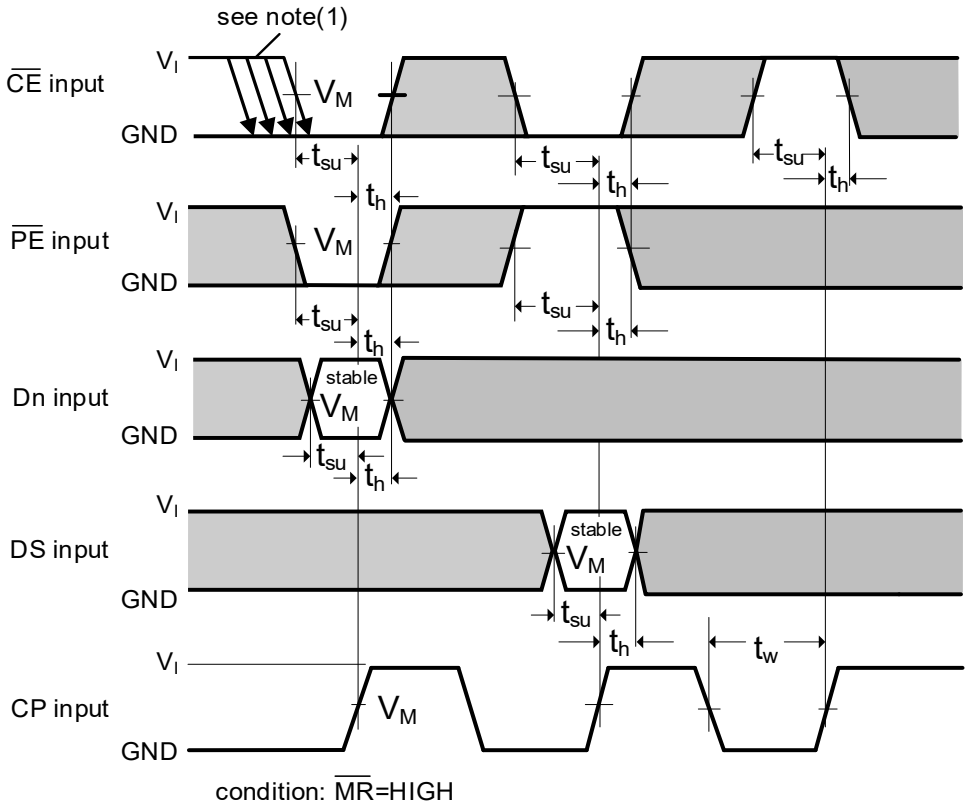


Figure 8-5 Set-up and hold times

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT
	V_M	V_M
CJ74HC166	0.5xV_{CC}	0.5xV_{CC}
CJ74HCT166	1.3V	1.3V

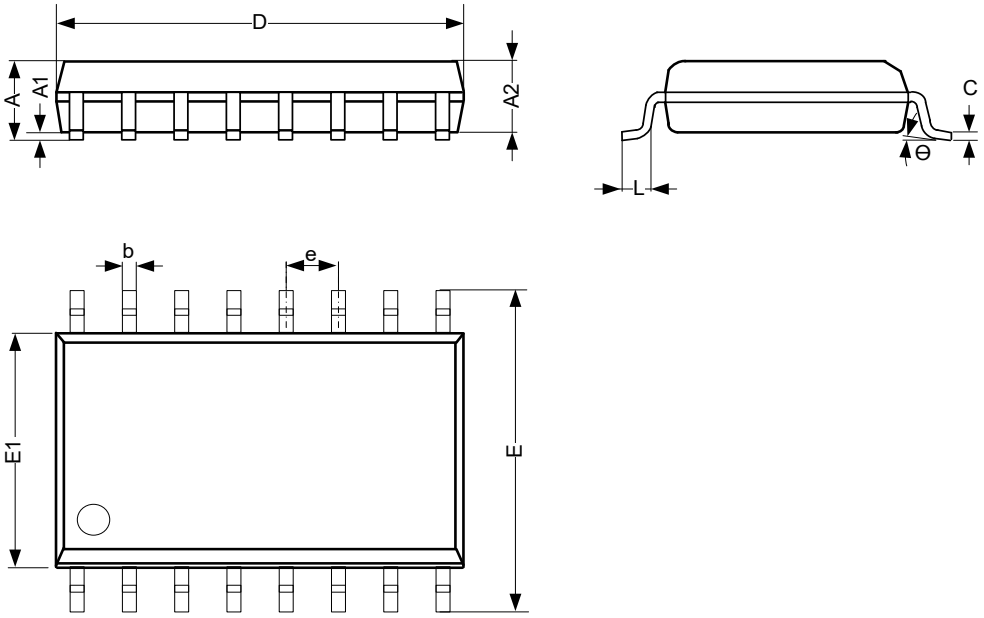
8.4.4 Test Data

TYPE	INPUT		LOAD		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
CJ74HC166	V_{CC}	3.0ns	15pF, 50pF	1kΩ	Open	V_{CC}	GND
CJ74HCT166	3.0V	3.0ns	15pF, 50pF	1kΩ	Open	V_{CC}	GND

9 Mechanical Information

9.1 SOP16 Mechanical Information

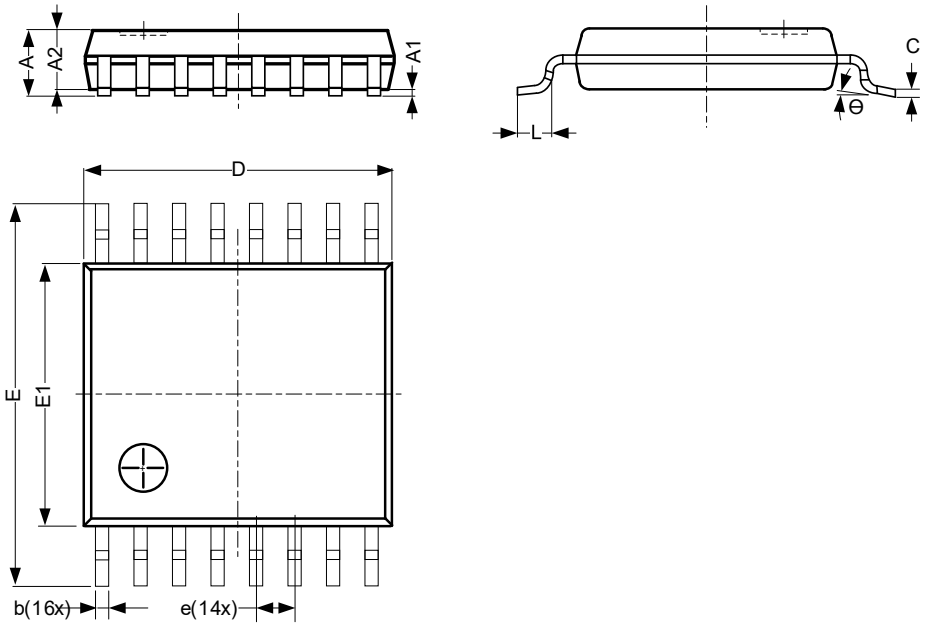
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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