8-bit Addressable Latch

CJ74HC/HCT259 Logic

1 Introduction

The CJ74HC/HCT259 is an 8-bit addressable latch. The device features four modes of operation. In the addressable latch mode, data on the D input is written into the latch addressed by the inputs A0 to A3. The addressed latch will follow the data input, non-addressed latches will retain their previous states. In memory mode, all latches retain their previous states and are unaffected by the data or address inputs. In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the D input and all other outputs are LOW. In the reset mode, all outputs are forced LOW and unaffected by the data or address inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

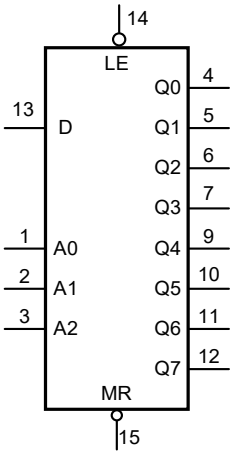
2 Available Packages

PART NUMBER	PACKAGE
CJ74HC259	SOP16
	TSSOP16
CJ74HCT259	SOP16
	TSSOP16

Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
  - For CJ74HC259: CMOS level
  - For CJ74HCT259: TTL level
- Combined demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Specified from -40°C to +125°C



Logic symbol

4 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC259AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT259AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC259BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74HCT259BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

5 Pin Configuration and Marking Information

5.1 Pin Configuration

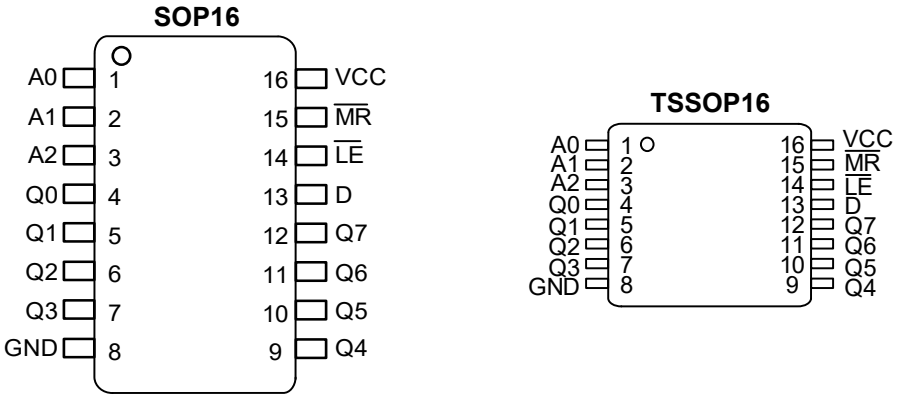


Figure 5-1 Pin configuration

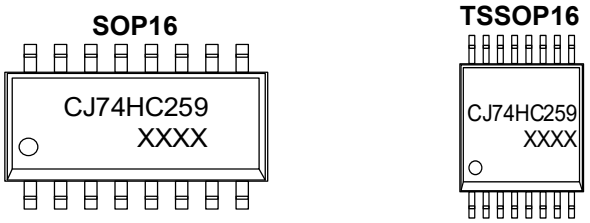
5.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	A0	I	Address input
2	A1	I	Address input
3	A2	I	Address input
4	Q0	O	Latch output
5	Q1	O	Latch output
6	Q2	O	Latch output
7	Q3	O	Latch output
8	GND	G	Ground (0V)
9	Q4	O	Latch output
10	Q5	O	Latch output
11	Q6	O	Latch output
12	Q7	O	Latch output
13	D	I	Data input
14	$\overline{LE}$	I	Latch enable input (active LOW)
15	$\overline{MR}$	I	Conditional reset input (active LOW)
16	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

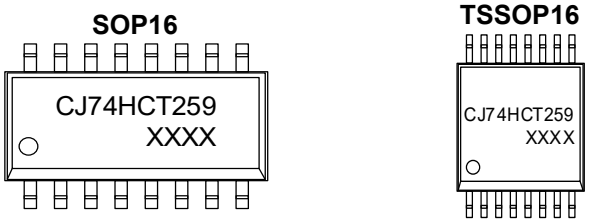
5.3 Marking Information

5.3.1 CJ74HC259



XXXX: Code, indicates weekly record information.

5.3.2 CJ74HCT259



XXXX: Code, indicates weekly record information.

6 Specifications

6.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7.0	V
I_{IK}	Input clamping current	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
I_{OK}	Output clamping current	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
I_O	Output current	V_O= -0.5V to (V_{CC}+0.5V)		-	±25	mA
I_{CC}	Supply current	-		-	+70	mA
I_{GND}	Ground current	-		-70	-	mA
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

6.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC259						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT259						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

6.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Electrical Characteristics

6.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC259							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
C_I	Input capacitance	-		-	3.5	-	pF
CJ74HCT259							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL};	I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.15	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	8.0	uA
ΔI_{CC}	Additional supply current	V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	Pin An, $\overline{LE}$	-	150	540	uA
			Pin D	-	120	432	uA
			Pin $\overline{MR}$	-	75	270	uA
C_I	Input capacitance	-		-	3.5	-	pF

6.4.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC259							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
C_I	Input capacitance	-		-	-	-	pF
CJ74HCT259							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL};	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL};	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
ΔI_{CC}	Additional supply current	V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	Pin An, $\overline{LE}$	-	-	675	uA
			Pin D	-	-	540	uA
			Pin $\overline{MR}$	-	-	338	uA
C_I	Input capacitance	-		-	-	-	pF

6.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC259							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
C_I	Input capacitance	-		-	-	-	pF
CJ74HCT259							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL};	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL};	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
ΔI_{CC}	Additional supply current	V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	Pin An, $\overline{LE}$	-	-	735	uA
			Pin D	-	-	588	uA
			Pin $\overline{MR}$	-	-	368	uA
C_I	Input capacitance	-		-	-	-	pF

6.4.4 AC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC259							
t_{pd}	Propagation delay	D to Qn; See Figure 7-5	V_{CC}=2.0V	-	58	185	ns
			V_{CC}=4.5V	-	21	37	ns
			V_{CC}=5.0V; C_L=15pF	-	18	-	ns
			V_{CC}=6.0V	-	17	31	ns
		An to Qn; See Figure 7-6	V_{CC}=2.0V	-	58	185	ns
			V_{CC}=4.5V	-	21	37	ns
			V_{CC}=5.0V; C_L=15pF	-	17	-	ns
			V_{CC}=6.0V	-	17	31	ns
		$\overline{LE}$ to Qn; See Figure 7-7	V_{CC}=2.0V	-	55	170	ns
			V_{CC}=4.5V	-	20	34	ns
			V_{CC}=5.0V; C_L=15pF	-	17	-	ns
			V_{CC}=6.0V	-	16	29	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; See Figure 7-8	V_{CC}=2.0V	-	50	155	ns
			V_{CC}=4.5V	-	18	31	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	26	ns
t_t	Transition time	See Figure 7-7	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
t_W	Pulse width	$\overline{LE}$ HIGH or LOW; See Figure 7-7	V_{CC}=2.0V	70	-	-	ns
			V_{CC}=4.5V	14	-	-	ns
			V_{CC}=6.0V	12	-	-	ns
		$\overline{MR}$ LOW; See Figure 7-8	V_{CC}=2.0V	70	-	-	ns
			V_{CC}=4.5V	14	-	-	ns
			V_{CC}=6.0V	12	-	-	ns
t_{su}	Set-up time	D, An to $\overline{LE}$; See Figure 7-9 and Figure 7-10	V_{CC}=2.0V	80	-	-	ns
			V_{CC}=4.5V	16	-	-	ns
			V_{CC}=6.0V	14	-	-	ns
t_h	Hold time	D to $\overline{LE}$; See Figure 7-9 and Figure 7-10	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		An to $\overline{LE}$; See Figure 7-9 and Figure 7-10	V_{CC}=2.0V	2	-	-	ns
			V_{CC}=4.5V	2	-	-	ns
			V_{CC}=6.0V	2	-	-	ns

C_{PD}	Power dissipation capacitance	f_i=1MHz; V_I=GND to V_{CC}		-	19	-	pF
CJ74HCT259							
t_{pd}	Propagation delay	D to Qn; See Figure 7-5	V_{CC}=4.5V	-	23	39	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
		An to Qn; See Figure 7-6	V_{CC}=4.5V	-	25	41	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
		$\overline{LE}$ to Qn; See Figure 7-7	V_{CC}=4.5V	-	22	38	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; See Figure 7-8	V_{CC}=4.5V	-	23	39	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
t_t	Transition time	V_{CC}=4.5V; See Figure 7-7		-	7	15	ns
t_W	Pulse width	$\overline{LE}$ HIGH or LOW; V_{CC}=4.5V; See Figure 7-7		19	-	-	ns
		$\overline{MR}$ LOW; V_{CC}=4.5V; See Figure 7-8		18	-	-	ns
t_{su}	Set-up time	D, An to $\overline{LE}$; V_{CC}=4.5V; See Figure 7-9 and Figure 7-10		17	-	-	ns
t_h	Hold time	D to $\overline{LE}$; V_{CC}=4.5V; See Figure 7-9 and Figure 7-10		0	-	-	ns
		An to $\overline{LE}$; V_{CC}=4.5V; See Figure 7-9 and Figure 7-10		0	-	-	ns
C_{PD}	Power dissipation capacitance	f_i=1MHz; V_I=GND to V_{CC}-1.5V		-	19	-	pF

Note:

(1) Typical values are measured at nominal supply voltage (V_{CC}=3.3V and V_{CC}=5.0V).

(2) t_{pd} is the same as t_{PLH} and t_{PHL}.

(3) t_t is the same as t_{THL} and t_{TLH}.

(4) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}xV_{CC}^2xf_ixN+\sum(C_LxV_{CC}^2xf_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_LxV_{CC}^2xf_o)$=sum of outputs.

6.4.5 AC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC259							
t_{pd}	Propagation delay	D to Qn; See Figure 7-5	V_{CC}=2.0V	-	-	230	ns
			V_{CC}=4.5V	-	-	46	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	39	ns
		An to Qn; See Figure 7-6	V_{CC}=2.0V	-	-	230	ns
			V_{CC}=4.5V	-	-	46	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	39	ns
		$\overline{LE}$ to Qn; See Figure 7-7	V_{CC}=2.0V	-	-	215	ns
			V_{CC}=4.5V	-	-	43	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	37	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; See Figure 7-8	V_{CC}=2.0V	-	-	195	ns
			V_{CC}=4.5V	-	-	39	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	33	ns
t_t	Transition time	See Figure 7-7	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
t_W	Pulse width	$\overline{LE}$ HIGH or LOW; See Figure 7-7	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
		$\overline{MR}$ LOW; See Figure 7-8	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
t_{su}	Set-up time	D, An to $\overline{LE}$; See Figure 7-9 and Figure 7-10	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
t_h	Hold time	D to $\overline{LE}$; See Figure 7-9 and Figure 7-10	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		An to $\overline{LE}$; See Figure 7-9 and Figure 7-10	V_{CC}=2.0V	2	-	-	ns
			V_{CC}=4.5V	2	-	-	ns
			V_{CC}=6.0V	2	-	-	ns

C_{PD}	Power dissipation capacitance	fi=1MHz; V_I=GND to V_{CC}		-	-	-	pF
CJ74HCT259							
t_{pd}	Propagation delay	D to Qn; See Figure 7-5	V_{CC}=4.5V	-	-	49	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
		An to Qn; See Figure 7-6	V_{CC}=4.5V	-	-	51	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
		$\overline{LE}$ to Qn; See Figure 7-7	V_{CC}=4.5V	-	-	48	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; See Figure 7-8	V_{CC}=4.5V	-	-	49	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
t_t	Transition time	V_{CC}=4.5V; See Figure 7-7		-	-	19	ns
t_W	Pulse width	$\overline{LE}$ HIGH or LOW; V_{CC}=4.5V; See Figure 7-7		24	-	-	ns
		$\overline{MR}$ LOW; V_{CC}=4.5V; See Figure 7-8		23	-	-	ns
t_{su}	Set-up time	D, An to $\overline{LE}$; V_{CC}=4.5V; See Figure 7-9 and Figure 7-10		21	-	-	ns
t_h	Hold time	D to $\overline{LE}$; V_{CC}=4.5V; See Figure 7-9 and Figure 7-10		0	-	-	ns
		An to $\overline{LE}$; V_{CC}=4.5V; See Figure 7-9 and Figure 7-10		0	-	-	ns
C_{PD}	Power dissipation capacitance	f_i=1MHz; V_I=GND to V_{CC}-1.5V		-	-	-	pF

Note:

(1) Typical values are measured at nominal supply voltage (V_{CC}=3.3V and V_{CC}=5.0V).

(2) t_{pd} is the same as t_{PLH} and t_{PHL}.

(3) t_t is the same as t_{THL} and t_{TLH}.

(4) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}xV_{CC}^2xf_ixN+\sum(C_LxV_{CC}^2xf_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_LxV_{CC}^2xf_o)$=sum of outputs.

6.4.6 AC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC259							
t_{pd}	Propagation delay	D to Qn; See Figure 7-5	V_{CC}=2.0V	-	-	280	ns
			V_{CC}=4.5V	-	-	56	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	48	ns
		An to Qn; See Figure 7-6	V_{CC}=2.0V	-	-	280	ns
			V_{CC}=4.5V	-	-	56	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	48	ns
		$\overline{LE}$ to Qn; See Figure 7-7	V_{CC}=2.0V	-	-	255	ns
			V_{CC}=4.5V	-	-	51	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	43	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; See Figure 7-8	V_{CC}=2.0V	-	-	235	ns
			V_{CC}=4.5V	-	-	47	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	40	ns
t_t	Transition time	See Figure 7-7	V_{CC}=2.0V	-	-	119	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
t_W	Pulse width	$\overline{LE}$ HIGH or LOW; See Figure 7-7	V_{CC}=2.0V	105	-	-	ns
			V_{CC}=4.5V	21	-	-	ns
			V_{CC}=6.0V	18	-	-	ns
		$\overline{MR}$ LOW; See Figure 7-8	V_{CC}=2.0V	105	-	-	ns
			V_{CC}=4.5V	21	-	-	ns
			V_{CC}=6.0V	18	-	-	ns
t_{su}	Set-up time	D, An to $\overline{LE}$; See Figure 7-9 and Figure 7-10	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
t_h	Hold time	D to $\overline{LE}$; See Figure 7-9 and Figure 7-10	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		An to $\overline{LE}$; See Figure 7-9 and Figure 7-10	V_{CC}=2.0V	2	-	-	ns
			V_{CC}=4.5V	2	-	-	ns
			V_{CC}=6.0V	2	-	-	ns

C_{PD}	Power dissipation capacitance	f_i=1MHz; V_I=GND to V_{CC}		-	-	-	pF
CJ74HCT259							
t_{pd}	Propagation delay	D to Qn; See Figure 7-5	V_{CC}=4.5V	-	-	59	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
		An to Qn; See Figure 7-6	V_{CC}=4.5V	-	-	62	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
		$\overline{LE}$ to Qn; See Figure 7-7	V_{CC}=4.5V	-	-	57	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; See Figure 7-8	V_{CC}=4.5V	-	-	59	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
t_t	Transition time	V_{CC}=4.5V; See Figure 7-7		-	-	22	ns
t_W	Pulse width	$\overline{LE}$ HIGH or LOW; V_{CC}=4.5V; See Figure 7-7		29	-	-	ns
		$\overline{MR}$ LOW; V_{CC}=4.5V; See Figure 7-8		27	-	-	ns
t_{su}	Set-up time	D, An to $\overline{LE}$; V_{CC}=4.5V; See Figure 7-9 and Figure 7-10		26	-	-	ns
t_h	Hold time	D to $\overline{LE}$; V_{CC}=4.5V; See Figure 7-9 and Figure 7-10		0	-	-	ns
		An to $\overline{LE}$; V_{CC}=4.5V; See Figure 7-9 and Figure 7-10		0	-	-	ns
C_{PD}	Power dissipation capacitance	f_i=1MHz; V_I=GND to V_{CC}-1.5V		-	-	-	pF

Note:

(1) Typical values are measured at nominal supply voltage (V_{CC}=3.3V and V_{CC}=5.0V).

(2) t_{pd} is the same as t_{PLH} and t_{PHL}.

(3) t_t is the same as t_{THL} and t_{TLH}.

(4) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}xV_{CC}^2xf_ixN+\sum(C_LxV_{CC}^2xf_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_LxV_{CC}^2xf_o)$=sum of outputs.

7 Detailed Description

7.1 Overview

The CJ74HC/HCT259 is an 8-bit addressable latch. The device features four modes of operation. In the addressable latch mode, data on the D input is written into the latch addressed by the inputs A0 to A3. The addressed latch will follow the data input, non-addressed latches will retain their previous states. In memory mode, all latches retain their previous states and are unaffected by the data or address inputs. In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the D input and all other outputs are LOW. In the reset mode, all outputs are forced LOW and unaffected by the data or address inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

7.2 Functional Block Diagram

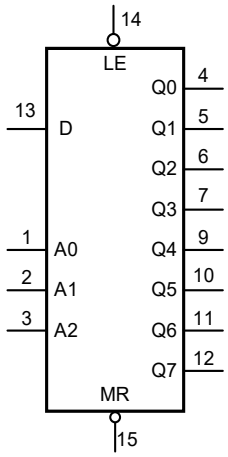


Figure 7-1 Logic symbol

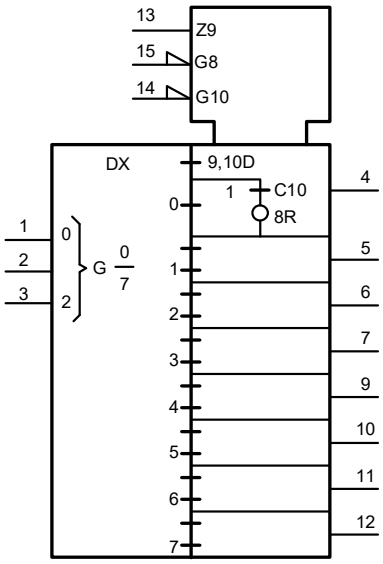


Figure 7-2 IEC logic symbol

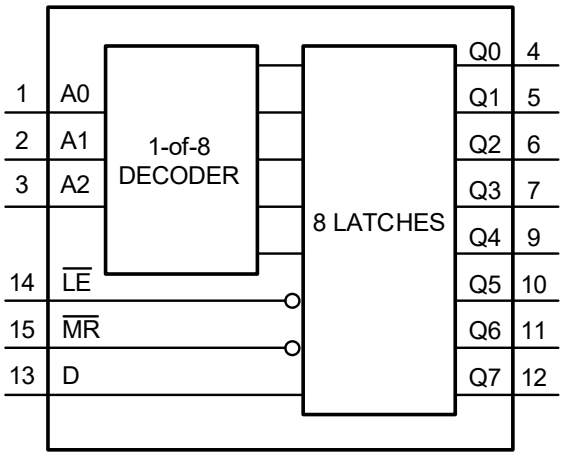


Figure 7-3 Functional diagram

7.3 Function Table

OPERATING MODE	INPUT						OUTPUT							
	$\overline{MR}$	$\overline{LE}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Reset (clear)	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active HIGH 8-channel) decoder (when D=H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Memory (no action)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	H	L	q_0	q_1	q_2	Q=d	q_4	q_5	q_6	q_7
	H	L	d	L	L	H	q_0	q_1	q_2	q_3	Q=d	q_5	q_6	q_7
	H	L	d	H	L	H	q_0	q_1	q_2	q_3	q_4	Q=d	q_6	q_7
	H	L	d	L	H	H	q_0	q_1	q_2	q_3	q_4	q_5	Q=d	q_7
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d

Note:

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care.

(2) d=HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{LE}$ transition.

(3) q=lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

7.4 Operating Mode Select Table

$\overline{LE}$	$\overline{MR}$	MODE
L	H	Addressable latch mode
H	H	Memory mode
L	L	Demultiplexer mode
H	L	Reset mode

Note: H=HIGH voltage level; L=LOW voltage level

7.5 Testing Circuit

7.5.1 AC Testing Circuit

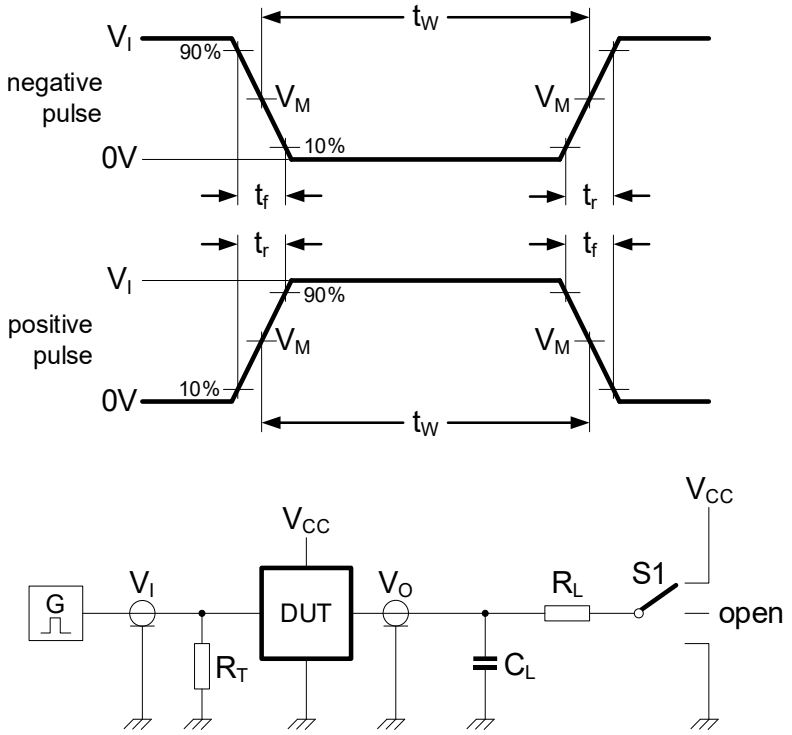


Figure 7-4 Test circuit for measuring switching times

Definitions for test circuit:

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

S1=Test selection switch.

7.5.2 AC Testing Waveforms

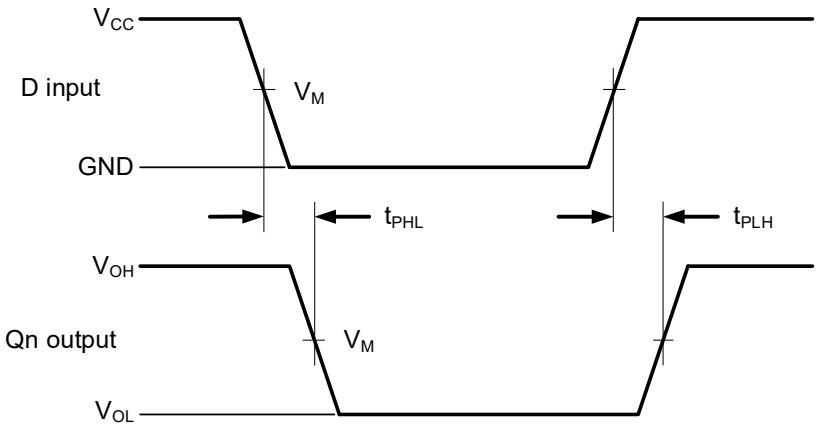


Figure 7-5 Data input to output propagation delays

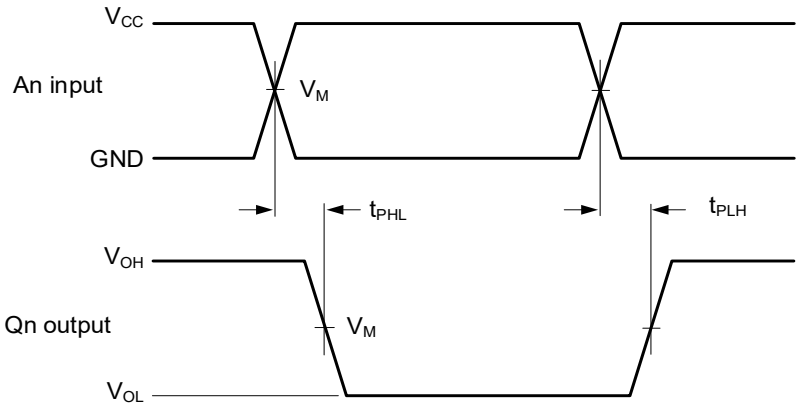


Figure 7-6 Address input to output propagation delays

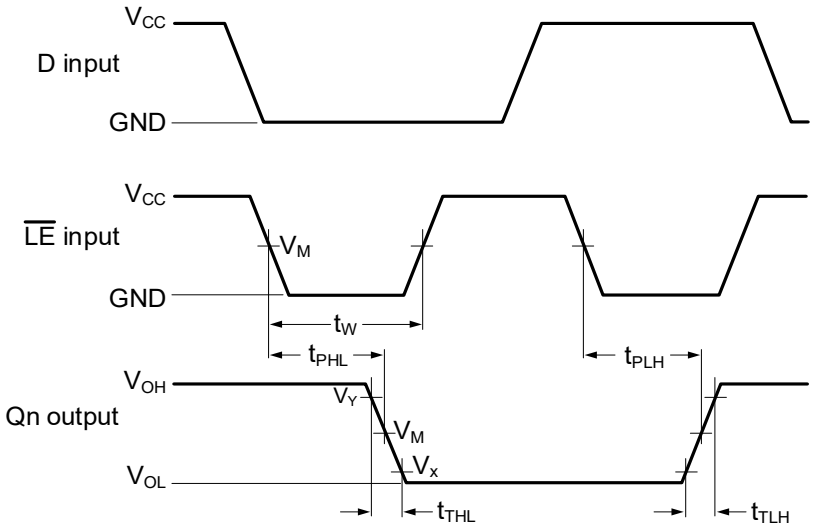


Figure 7-7 Enable input to output propagation delays and pulse width

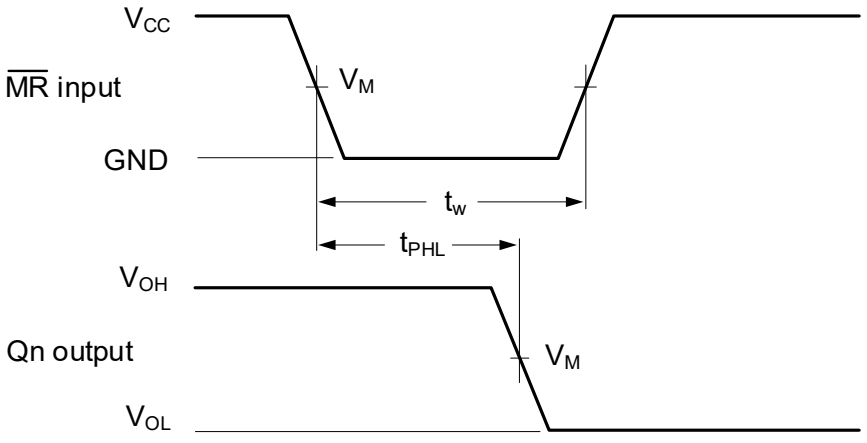


Figure 7-8 Master reset input to output propagation delay

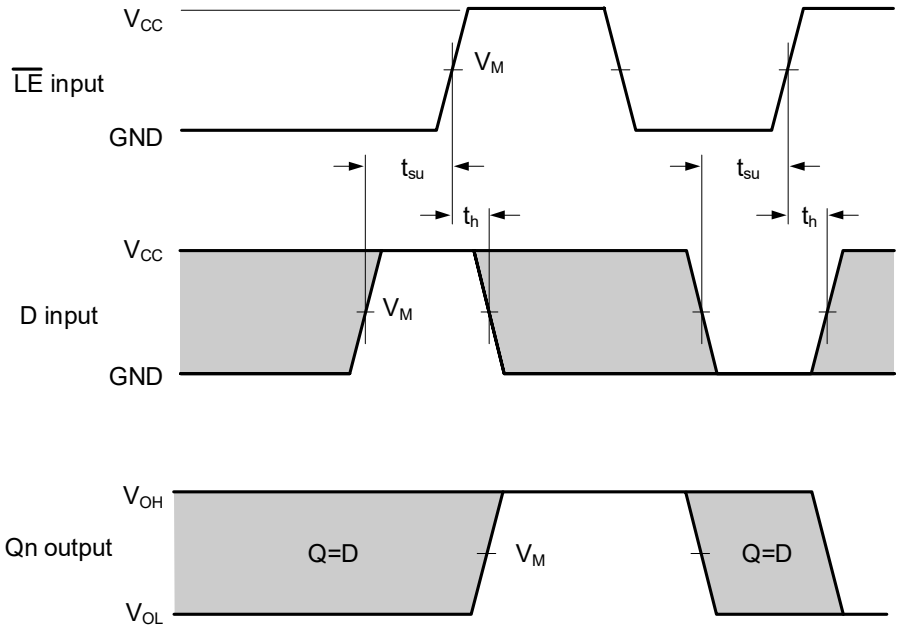


Figure 7-9 Data input to latch enable input set-up and hold times

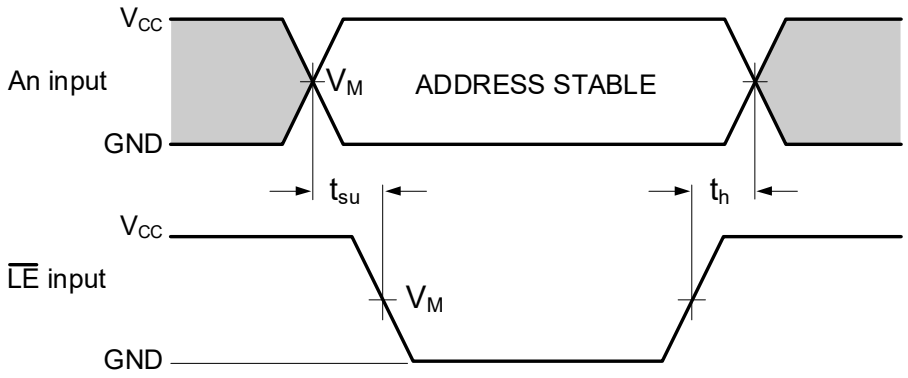


Figure 7-10 Address input to latch enable input set-up and hold times

7.5.3 Measurement Points

TYPE	INPUT	OUTPUT		
	V_M	V_M	V_X	V_Y
CJ74HC259	0.5xV_{CC}	0.5xV_{CC}	0.1xV_{CC}	0.9xV_{CC}
CJ74HCT259	1.3V	1.3V	0.1xV_{CC}	0.9xV_{CC}

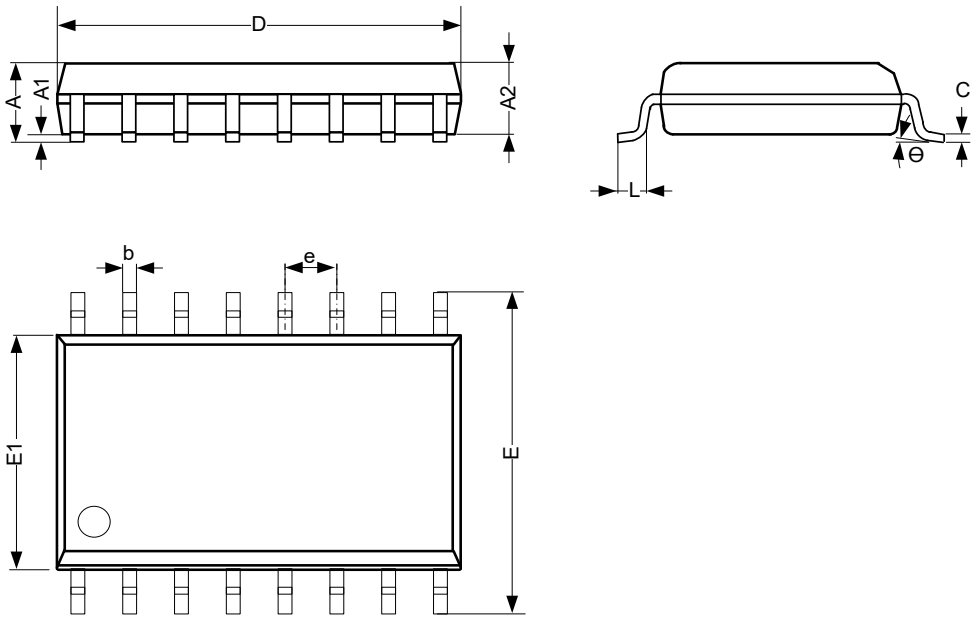
7.5.4 Test Data

TYPE	INPUT		LOAD		S1 POSITION
	V_I	t_r , t_f	C_L	R_L	t_{PHL},t_{PLH}
CJ74HC259	V_{CC}	6ns	15pF, 50pF	1kΩ	Open
CJ74HCT259	3V	6ns	15pF, 50pF	1kΩ	Open

8 Mechanical Information

8.1 SOP16 Mechanical Information

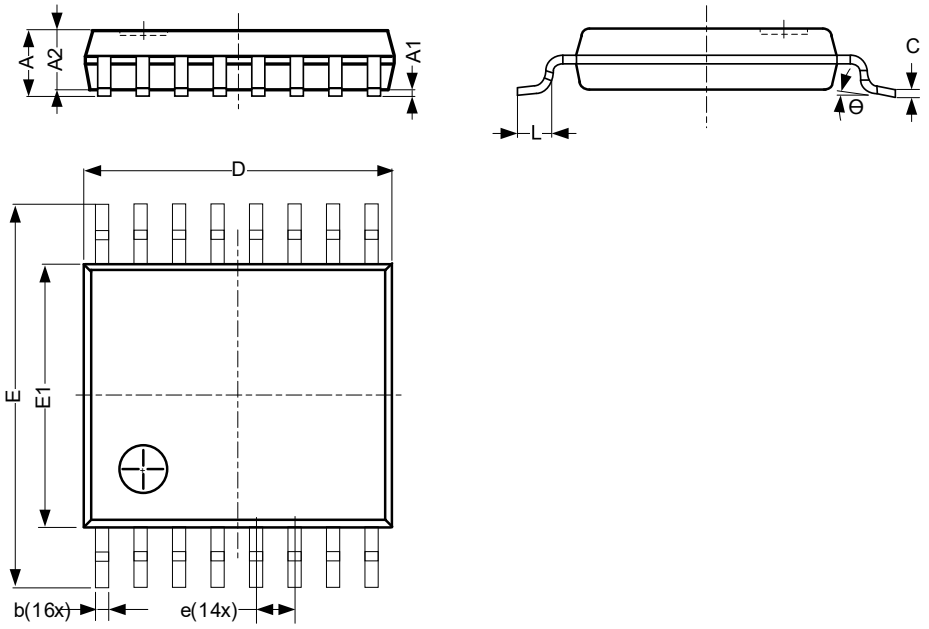
8.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
Θ	0°	-	8°
Unit: mm			

8.2 TSSOP16 Mechanical Information

8.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

9 Notes and Revision History

9.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

9.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

Official Website: www.jscj-elec.com