

**Octal D-type Flip-flop with Reset: Positive Edge-trigger****CJ74HC/HCT273 Logic****1 Introduction**

The CJ74HC/HCT273 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and master reset (/MR) inputs. The outputs Q_n will assume the state of their corresponding D_n inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A LOW on /MR forces the outputs LOW independently of clock and data inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC273	SOP20
	TSSOP20
CJ74HCT273	SOP20
	TSSOP20

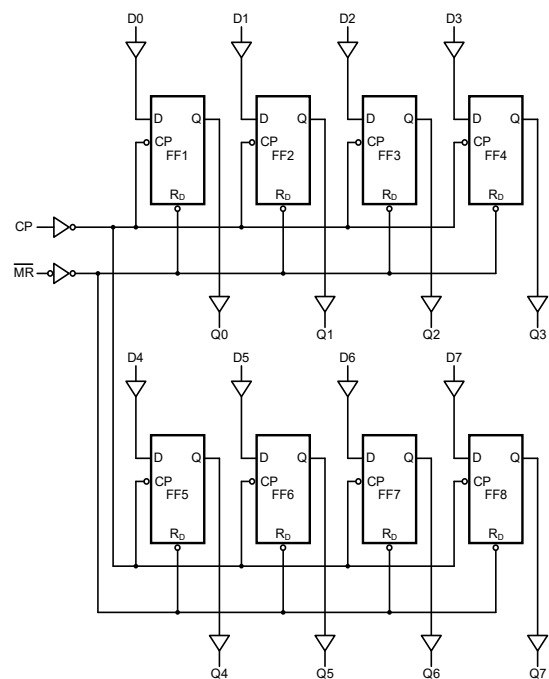
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
 - For CJ74HC273: CMOS level
 - For CJ74HCT273: TTL level
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Specified from -40°C to +125°C

4 Applications

- Buffer or store registers
- Shift registers
- Pattern generators



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC273AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units / Reel	Active
CJ74HCT273AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units / Reel	Active
CJ74HC273BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT273BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

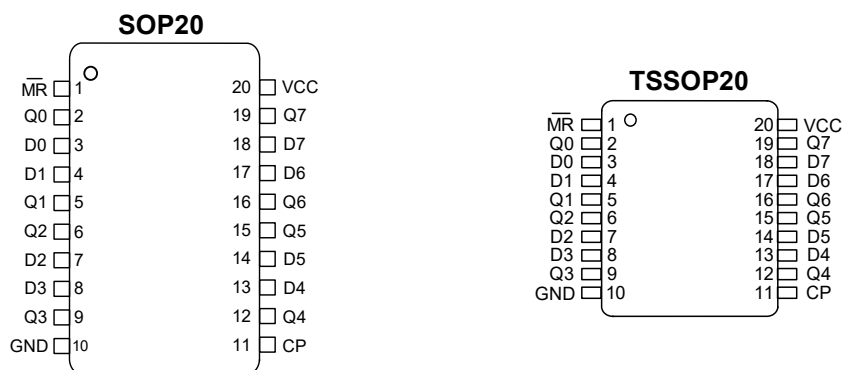


Figure 6-1 Pin configuration

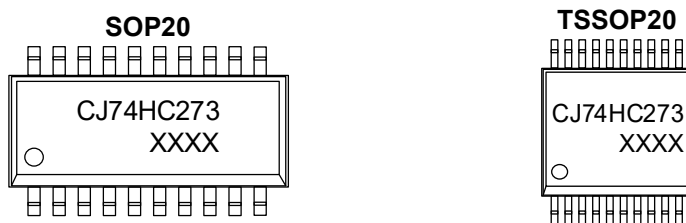
6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	MR	I	Master reset input (active LOW)
2	Q0	O	Flip-flop output
3	D0	I	Data input
4	D1	I	Data input
5	Q1	O	Flip-flop output
6	Q2	O	Flip-flop output
7	D2	I	Data input
8	D3	I	Data input
9	Q3	O	Flip-flop output
10	GND	G	Ground (0V)
11	CP	I	Clock input (LOW-to-HIGH, edge-triggered)
12	Q4	O	Flip-flop output
13	D4	I	Data input
14	D5	I	Data input
15	Q5	O	Flip-flop output
16	Q6	O	Flip-flop output
17	D6	I	Data input
18	D7	I	Data input
19	Q7	O	Flip-flop output
20	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

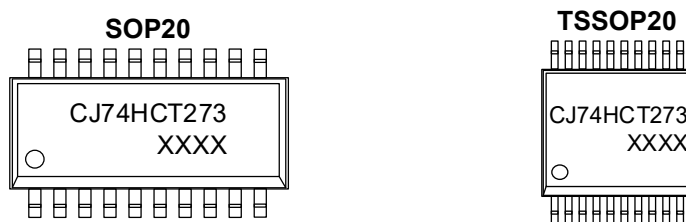
6.3 Marking Information

6.3.1 CJ74HC273



XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT273



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7.0	V
I_{IK}	Input clamping current	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	± 20	mA
I_{OK}	Output clamping current	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	± 20	mA
I_O	Output current	$-0.5V < V_O < V_{CC}+0.5V$		-	± 25	mA
I_{CC}	Supply current	-		-	50	mA
I_{GND}	Ground current	-		-50	-	mA
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC273						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
$\Delta t/\Delta V$	Input transition rise and fall rate	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
T_{amb}	Ambient temperature	-	-40	-	+85	°C
CJ74HCT273						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
$\Delta t/\Delta V$	Input transition rise and fall rate	$V_{CC}=2.0V$	-	-	-	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	-	ns/V
T_{amb}	Ambient temperature	-	-40	-	+85	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	± 4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

$T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC273							
V _{IH}	HIGH-level input voltage	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I =V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	2.0	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	4.5	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	6.0	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.98	4.32	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.48	5.81	-	V
V _{OL}	LOW-level output voltage	V _I =V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	0	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	0	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	0	0.1	V
			I _O =4.0mA; V _{CC} =4.5V	-	0.15	0.26	V
			I _O =5.2mA; V _{CC} =6.0V	-	0.16	0.26	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	8.0	uA
C _I	Input capacitance	-		-	3.5	-	pF
CJ74HCT273							
V _{IH}	HIGH-level input voltage	V _{CC} =4.5V to 5.5V		2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =4.5V to 5.5V		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I =V _{IH} or V _{IL} ;	I _O =-20uA; V _{CC} =4.5V	4.4	4.5	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.98	4.32	-	V
V _{OL}	LOW-level output voltage	V _I =V _{IH} or V _{IL}	I _O =20uA; V _{CC} =4.5V	-	0	0.1	V
			I _O =5.2mA; V _{CC} =5.5V	-	0.15	0.26	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =5.5V		-	-	±1.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =5.5V		-	-	8.0	uA
ΔI _{CC}	Additional supply current	Per input pin; V _I =V _{CC} -2.1V; Other inputs at V _{CC} or GND; V _{CC} =4.5V to 5.5V	MR input	-	-	360	uA
			CP input	-	-	630	uA
			Dn input	-	-	54	uA

C_i	Input capacitance	-	-	3.5	-	pF
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7.4.2 DC Characteristics 2

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC273							
V _{IH}	HIGH-level input voltage	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I =V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	-	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	-	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.84	-	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.34	-	-	V
V _{OL}	LOW-level output voltage	V _I =V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	-	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	-	0.1	V
			I _O =4.0mA; V _{CC} =4.5V	-	-	0.33	V
			I _O =5.2mA; V _{CC} =6.0V	-	-	0.33	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	80	uA
CJ74HCT273							
V _{IH}	HIGH-level input voltage	V _{CC} =4.5V to 5.5V		2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =4.5V to 5.5V		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I =V _{IH} or V _{IL} ;	I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.84	-	-	V
V _{OL}	LOW-level output voltage	V _I =V _{IH} or V _{IL} ;	I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =5.2mA; V _{CC} =5.5V	-	-	0.33	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =5.5V		-	-	±1.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =5.5V		-	-	80	uA
ΔI _{CC}	Additional supply current	Per input pin; V _I =V _{CC} -2.1V; Other inputs at V _{CC} or GND; V _{CC} =4.5V to 5.5V	MR input	-	-	450	uA
			CP input	-	-	787.5	uA
			Dn input	-	-	67.5	uA

7.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC273							
V _{IH}	HIGH-level input voltage	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I =V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	-	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	-	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.7	-	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I =V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	-	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	-	0.1	V
			I _O =4.0mA; V _{CC} =4.5V	-	-	0.4	V
			I _O =5.2mA; V _{CC} =6.0V	-	-	0.4	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	160	uA
CJ74HCT273							
V _{IH}	HIGH-level input voltage	V _{CC} =4.5V to 5.5V		2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =4.5V to 5.5V		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I =V _{IH} or V _{IL} ;	I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-4.0mA; V _{CC} =4.5V	3.7	-	-	V
V _{OL}	LOW-level output voltage	V _I =V _{IH} or V _{IL} ;	I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =5.2mA; V _{CC} =5.5V	-	-	0.4	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =5.5V		-	-	±1.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =5.5V		-	-	160	uA
ΔI _{CC}	Additional supply current	Per input pin; V _I =V _{CC} -2.1V; Other inputs at V _{CC} or GND; V _{CC} =4.5V to 5.5V:	MR input	-	-	490	uA
			CP input	-	-	857.5	uA
			Dn input	-	-	73.5	uA

7.4.4 AC Characteristics 1

T_{amb}=25°C, GND=0V, C_L=50pF, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC273							
t _{pd}	CP to Qn propagation delay	See Figure 8-6	V _{CC} =2.0V	-	41	150	ns
			V _{CC} =4.5V	-	15	30	ns
			V _{CC} =5.0V; C _L =15pF	-	15	-	ns
			V _{CC} =6.0V	-	13	26	ns
t _{PHL}	MR to Qn HIGH to LOW propagation delay	See Figure 8-7	V _{CC} =2.0V	-	44	150	ns
			V _{CC} =4.5V	-	16	30	ns
			V _{CC} =5.0V; C _L =15pF	-	15	-	ns
			V _{CC} =6.0V	-	14	26	ns
t _t	Transition time	Qn output; See Figure 8-6	V _{CC} =2.0V	-	19	75	ns
			V _{CC} =4.5V	-	7	15	ns
			V _{CC} =6.0V	-	6	13	ns
t _w	Pulse width	CP input HIGH or LOW; See Figure 8-6	V _{CC} =2.0V	80	-	-	ns
			V _{CC} =4.5V	16	-	-	ns
			V _{CC} =6.0V	14	-	-	ns
		MR input LOW; See Figure 8-7	V _{CC} =2.0V	60	-	-	ns
			V _{CC} =4.5V	12	-	-	ns
			V _{CC} =6.0V	10	-	-	ns
t _{rec}	Recovery time	MR to CP; See Figure 8-7	V _{CC} =2.0V	50	-	-	ns
			V _{CC} =4.5V	10	-	-	ns
			V _{CC} =6.0V	9	-	-	ns
t _{su}	Set-up time	Dn to CP; See Figure 8-8	V _{CC} =2.0V	60	-	-	ns
			V _{CC} =4.5V	12	-	-	ns
			V _{CC} =6.0V	10	-	-	ns
t _h	Hold time	Dn to CP; See Figure 8-8	V _{CC} =2.0V	3	-	-	ns
			V _{CC} =4.5V	3	-	-	ns
			V _{CC} =6.0V	3	-	-	ns
f _{max}	Maximum frequency	CP input; See Figure 8-6	V _{CC} =2.0V	6	20.6	-	MHz
			V _{CC} =4.5V	30	103	-	MHz
			V _{CC} =5.0V; C _L =15pF	-	66	-	MHz
			V _{CC} =6.0V	35	122	-	MHz
C _{PD}	Power dissipation capacitance	Per package; V _I =GND to V _{CC}		-	20	-	pF
CJ74HCT273							
t _{pd}	CP to Qn propagation delay	See Figure 8-6	V _{CC} =4.5V	-	16	30	ns
			V _{CC} =5.0V; C _L =15pF	-	15	-	ns

t_{PHL}	MR to Qn HIGH to LOW propagation delay	See Figure 8-7	$V_{CC}=4.5V$	-	23	34	ns
			$V_{CC}=5.0V; C_L=15pF$	-	20	-	ns
t_t	Transition time	See Figure 8-6	$V_{CC}=4.5V$	-	7	15	ns
t_w	Pulse width	CP input ; See Figure 8-6	$V_{CC}=4.5V$	16	-	-	ns
		MR input LOW ; See Figure 8-7	$V_{CC}=4.5V$	16	-	-	ns
t_{rec}	Recovery time	MR to CP; See Figure 8-7	$V_{CC}=4.5V$	10	-	-	ns
t_{su}	Set-up time	Dn to CP; See Figure 8-8	$V_{CC}=4.5V$	12	-	-	ns
t_h	Hold time	Dn to CP; See Figure 8-8	$V_{CC}=4.5V$	3	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	$V_{CC}=4.5V$	30	56	-	MHz
			$V_{CC}=5.0V; C_L=15pF$	-	36	-	MHz
C_{PD}	Power dissipation capacitance	Per package; $V_I=GND$ to $V_{CC}-1.5V$		-	23	-	pF

Note:

- (1) t_{pd} is the same as t_{PLH} and t_{PHL} .
(2) t_t is the same as t_{THL} and t_{TLH} .
(3) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =output load capacitance in pF;

V_{CC} =supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

7.4.5 AC Characteristics 2

$T_{amb} = -40^\circ C$ to $+85^\circ C$, $GND=0V$, $C_L=50pF$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC273						
t_{pd}	CP to Qn propagation delay	See Figure 8-6	$V_{CC}=2.0V$	-	-	185 ns
			$V_{CC}=4.5V$	-	-	37 ns
			$V_{CC}=6.0V$	-	-	31 ns
t_{PHL}	MR to Qn HIGH to LOW propagation delay	See Figure 8-7	$V_{CC}=2.0V$	-	-	185 ns
			$V_{CC}=4.5V$	-	-	37 ns
			$V_{CC}=6.0V$	-	-	31 ns
t_t	Transition time	Qn output; See Figure 8-6	$V_{CC}=2.0V$	-	-	95 ns
			$V_{CC}=4.5V$	-	-	19 ns
			$V_{CC}=6.0V$	-	-	15 ns
t_w	Pulse width	CP input HIGH or LOW; See Figure 8-6	$V_{CC}=2.0V$	100	-	- ns
			$V_{CC}=4.5V$	20	-	- ns
			$V_{CC}=6.0V$	17	-	- ns
		MR input LOW;	$V_{CC}=2.0V$	75	-	- ns

		See Figure 8-7	V _{CC} =4.5V	15	-	-	ns
			V _{CC} =6.0V	13	-	-	ns
t _{rec}	Recovery time	MR to CP; See Figure 8-7	V _{CC} =2.0V	65	-	-	ns
			V _{CC} =4.5V	13	-	-	ns
			V _{CC} =6.0V	11	-	-	ns
t _{su}	Set-up time	Dn to CP; See Figure 8-8	V _{CC} =2.0V	75	-	-	ns
			V _{CC} =4.5V	15	-	-	ns
			V _{CC} =6.0V	73	-	-	ns
t _h	Hold time	Dn to CP; See Figure 8-8	V _{CC} =2.0V	3	-	-	ns
			V _{CC} =4.5V	3	-	-	ns
			V _{CC} =6.0V	3	-	-	ns
f _{max}	Maximum frequency	CP input; See Figure 8-6	V _{CC} =2.0V	4.8	-	-	MHz
			V _{CC} =4.5V	24	-	-	MHz
			V _{CC} =6.0V	28	-	-	MHz

CJ74HCT273

t _{pd}	CP to Qn propagation delay	See Figure 8-6	V _{CC} =4.5V	-	-	38	ns
t _{PHL}	MR to Qn HIGH to LOW propagation delay	See Figure 8-7	V _{CC} =4.5V	-	-	43	ns
t _t	Transition time	See Figure 8-6	V _{CC} =4.5V	-	-	19	ns
t _w	Pulse width	CP input ; See Figure 8-6	V _{CC} =4.5V	20	-	-	ns
		MR input LOW ; See Figure 8-7	V _{CC} =4.5V	20	-	-	ns
t _{rec}	Recovery time	MR to CP; See Figure 8-7	V _{CC} =4.5V	13	-	-	ns
t _{su}	Set-up time	Dn to CP; See Figure 8-8	V _{CC} =4.5V	15	-	-	ns
t _h	Hold time	Dn to CP; See Figure 8-8	V _{CC} =4.5V	3	-	-	ns
f _{max}	Maximum frequency	CP input; See Figure 8-6	V _{CC} =4.5V	24	-	-	MHz

Note:

- (1) t_{pd} is the same as t_{PLH} and t_{PHL}.
(2) t_t is the same as t_{THL} and t_{TLH}.

7.4.6 AC Characteristics 3

T_{amb}=−40°C to +125°C, GND=0V, C_L=50pF, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC273							
t _{pd}	CP to Qn propagation delay	See Figure 8-6	V _{CC} =2.0V	-	-	225	ns
			V _{CC} =4.5V	-	-	45	ns
			V _{CC} =6.0V	-	-	38	ns
t _{PHL}	MR to Qn HIGH to LOW propagation delay	See Figure 8-7	V _{CC} =2.0V	-	-	225	ns
			V _{CC} =4.5V	-	-	45	ns
			V _{CC} =6.0V	-	-	38	ns
t _t	Transition time	Qn output; See Figure 8-6	V _{CC} =2.0V	-	-	110	ns
			V _{CC} =4.5V	-	-	22	ns
			V _{CC} =6.0V	-	-	19	ns
t _w	Pulse width	CP input HIGH or LOW; See Figure 8-6	V _{CC} =2.0V	120	-	-	ns
			V _{CC} =4.5V	24	-	-	ns
			V _{CC} =6.0V	20	-	-	ns
		MR input LOW; See Figure 8-7	V _{CC} =2.0V	90	-	-	ns
			V _{CC} =4.5V	18	-	-	ns
			V _{CC} =6.0V	15	-	-	ns
t _{rec}	Recovery time	MR to CP; See Figure 8-7	V _{CC} =2.0V	75	-	-	ns
			V _{CC} =4.5V	15	-	-	ns
			V _{CC} =6.0V	13	-	-	ns
t _{su}	Set-up time	Dn to CP; See Figure 8-8	V _{CC} =2.0V	90	-	-	ns
			V _{CC} =4.5V	18	-	-	ns
			V _{CC} =6.0V	15	-	-	ns
t _h	Hold time	Dn to CP; See Figure 8-8	V _{CC} =2.0V	3	-	-	ns
			V _{CC} =4.5V	3	-	-	ns
			V _{CC} =6.0V	3	-	-	ns
f _{max}	Maximum frequency	CP input; See Figure 8-6	V _{CC} =2.0V	4	-	-	MHz
			V _{CC} =4.5V	20	-	-	MHz
			V _{CC} =6.0V	24	-	-	MHz
CJ74HCT273							
t _{pd}	CP to Qn propagation delay	See Figure 8-6	V _{CC} =4.5V	-	-	45	ns
t _{PHL}	MR to Qn HIGH to LOW propagation delay	See Figure 8-7	V _{CC} =4.5V	-	-	51	ns
t _t	Transition time	See Figure 8-6	V _{CC} =4.5V	-	-	22	ns
t _w	Pulse width	CP input ; See Figure 8-6	V _{CC} =4.5V	24	-	-	ns
		MR input LOW ;	V _{CC} =4.5V	24	-	-	ns

		See Figure 8-7					
t_{rec}	Recovery time	MR to CP; See Figure 8-7	$V_{CC}=4.5V$	15	-	-	ns
t_{su}	Set-up time	Dn to CP; See Figure 8-8	$V_{CC}=4.5V$	18	-	-	ns
t_h	Hold time	Dn to CP; See Figure 8-8	$V_{CC}=4.5V$	3	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	$V_{CC}=4.5V$	20	-	-	MHz

Note:

(1) t_{pd} is the same as t_{PLH} and t_{PHL} .

(2) t_t is the same as t_{THL} and t_{TLH} .

8 Detailed Description

8.1 Overview

The CJ74HC/HCT273 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and master reset (/MR) inputs. The outputs Q_n will assume the state of their corresponding D_n inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A LOW on /MR forces the outputs LOW independently of clock and data inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

8.2 Functional Block Diagram

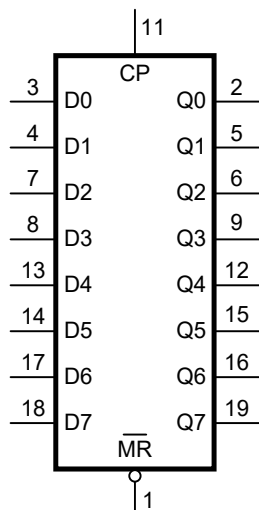


Figure 8-1 Logic symbol

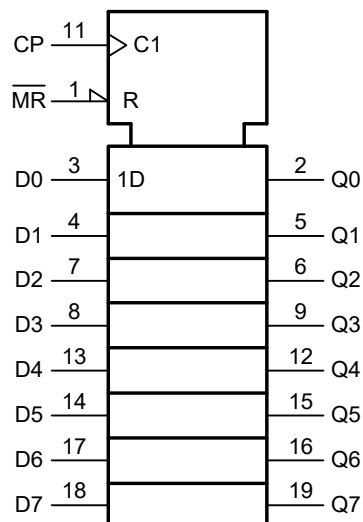


Figure 8-2 IEC logic symbol

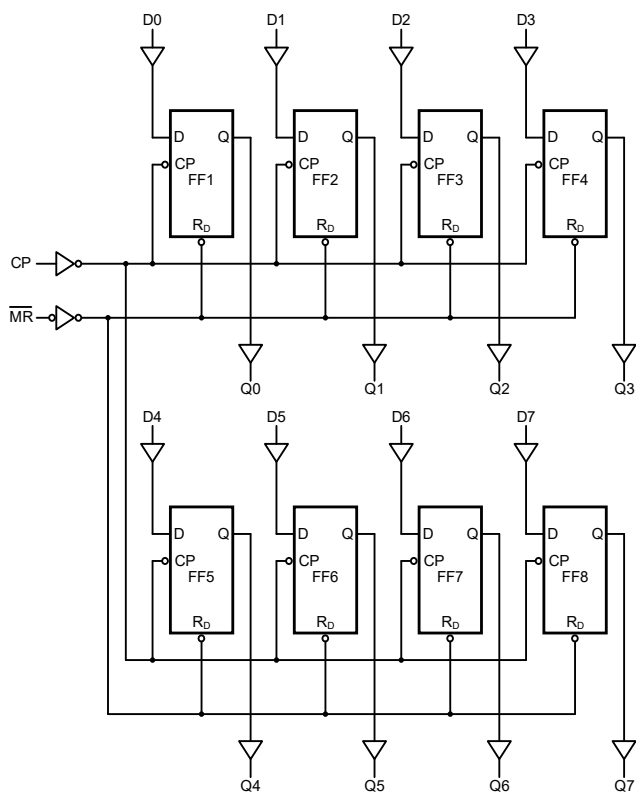


Figure 8-3 Logic diagram

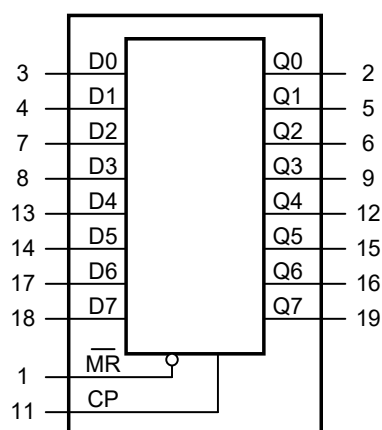


Figure 8-4 Functional diagram

8.3 Function Table

OPERATING MODES	INPUT			OUTPUT
	$\overline{\text{MR}}$	CP	Dn	Qn
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

Note:

- (1) H=HIGH voltage level; L=LOW voltage level; X=don't care;
- (2) h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
- (3) l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
- (4) ↑=LOW-to-HIGH clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

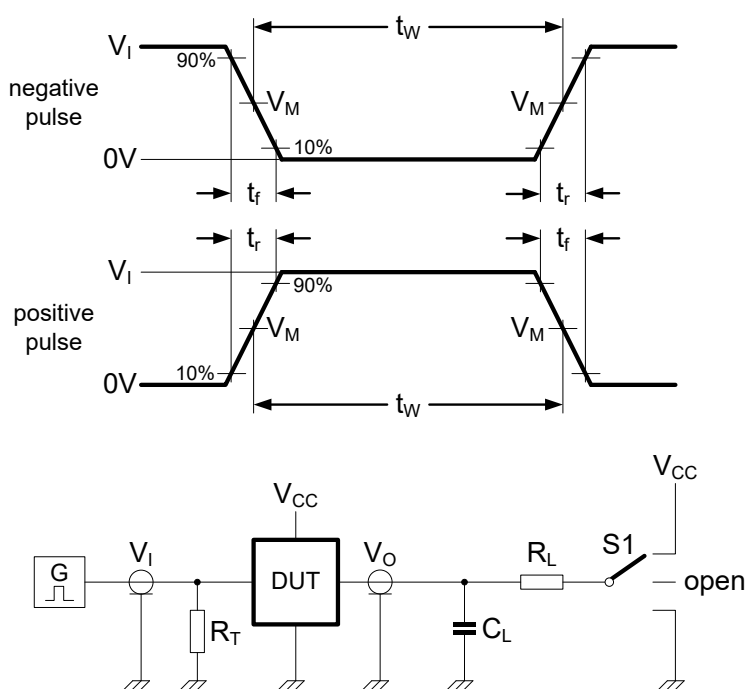


Figure 8-5 Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

8.4.2 AC Testing Waveforms

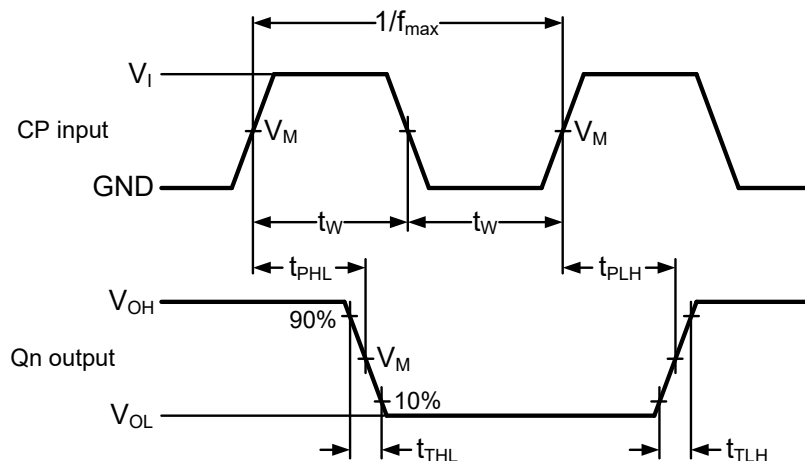


Figure 8-6 Propagation delay clock input (CP) to output (Qn), clock (CP) pulse width, output transition time and the maximum clock pulse frequency

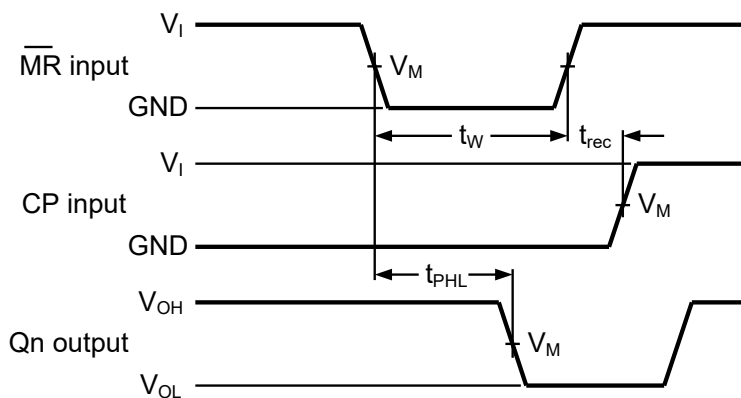


Figure 8-7 Propagation delay master reset ($\overline{MR}$) to output (Qn), pulse width master reset ($\overline{MR}$) and recovery time master reset ($\overline{MR}$) to clock (CP)

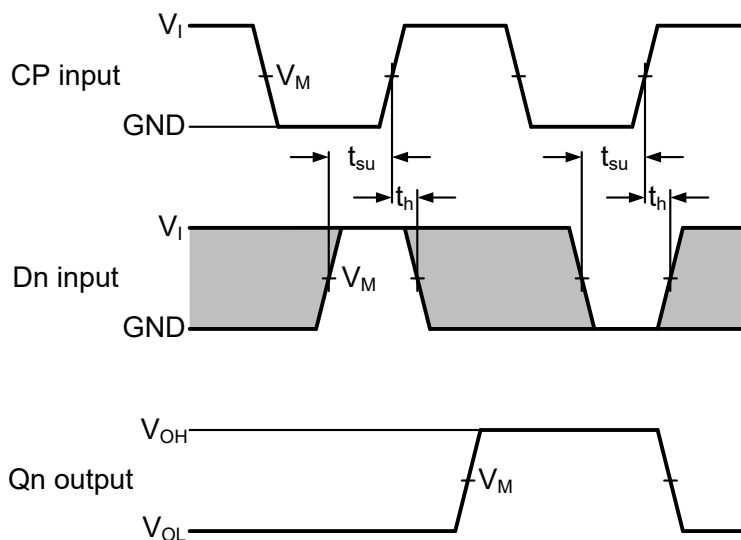


Figure 8-8 Data set-up and hold times data input (Dn)

8.4.3 Measurement Points

TYPE	INPUT		OUTPUT
	V_I	V_M	V_M
CJ74HC273	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
CJ74HCT273	3V	1.3V	1.3V

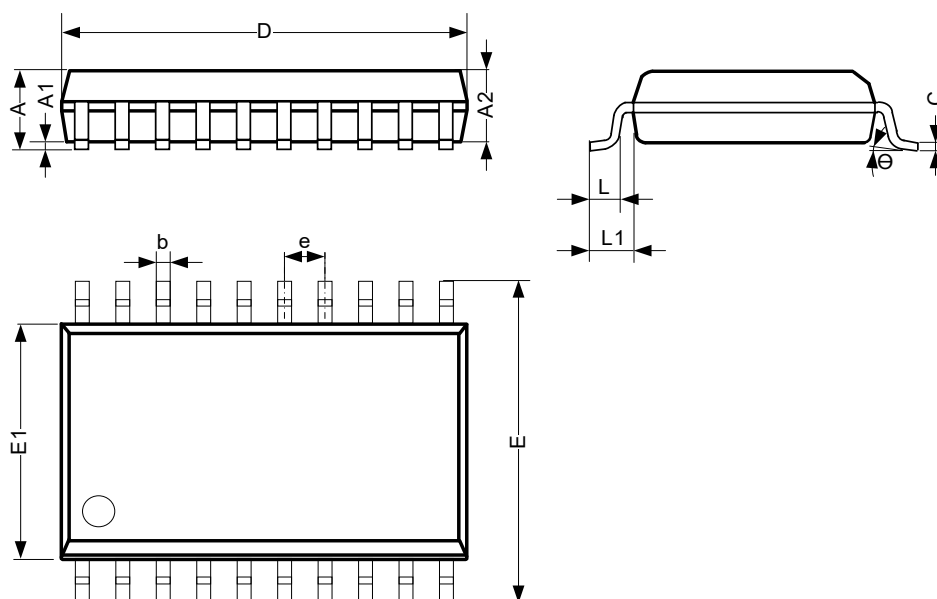
8.4.4 Test Data

TYPE	INPUT		LOAD		S1 POSITION
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
CJ74HC273	V_{CC}	6ns	15pF, 50pF	1k Ω	Open
CJ74HCT273	3V	6ns	15pF, 50pF	1k Ω	Open

9 Mechanical Information

9.1 SOP20 Mechanical Information

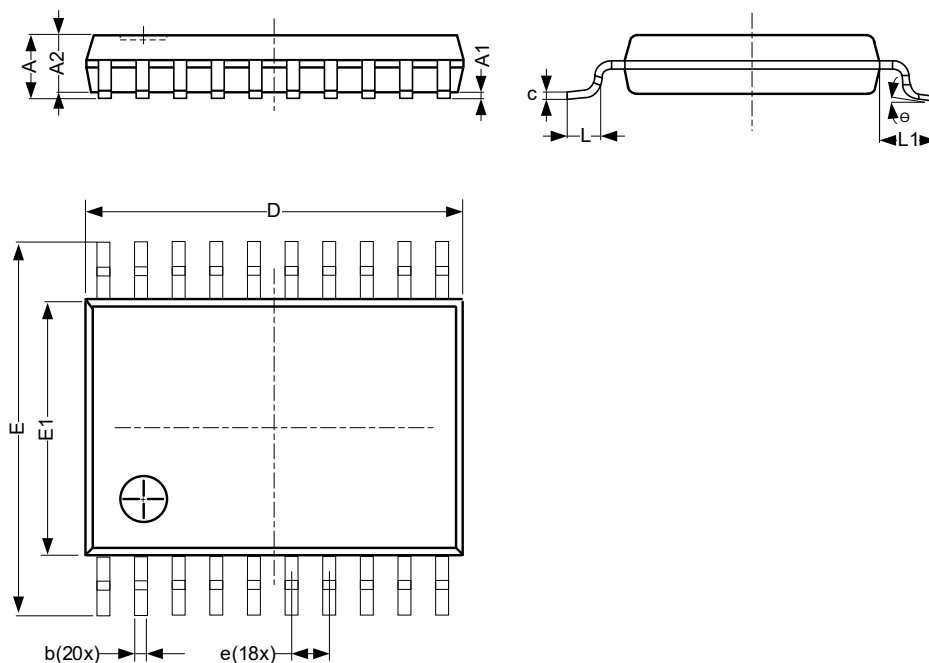
9.1.1 SOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	2.47	-	2.65
A1	0.05	-	0.30
A2	2.20	-	2.44
b	0.35	-	0.50
c	0.15	-	0.30
D	12.54	-	12.94
E	10.00	-	10.60
E1	7.30	-	7.70
e	1.27 BSC		
L	0.40	-	1.05
L1	1.30	-	1.50
θ	0°	-	8°
Unit: mm			

9.2 TSSOP20 Mechanical Information

9.2.1 TSSOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	-	6.60
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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