Octal D-type Transparent Latch; 3-state

CJ74HC/HCT573 Logic

1 Introduction

The CJ74HC/HCT573 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable (/OE) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on /OE causes the outputs to assume a high-impedance OFF-state. Operation of the /OE input does not affect the state of the latches. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC573	SOP20
	TSSOP20
CJ74HCT573	SOP20
	TSSOP20

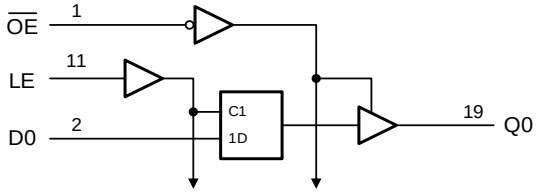
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
  For CJ74HC573: CMOS level
  For CJ74HCT573: TTL level
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Specified from -40°C to +125°C

4 Applications

- Buffer Registers
- Bidirectional Bus Drivers
- Working Registers



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC573AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units / Reel	Active
CJ74HCT573AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units / Reel	Active
CJ74HC573BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT573BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

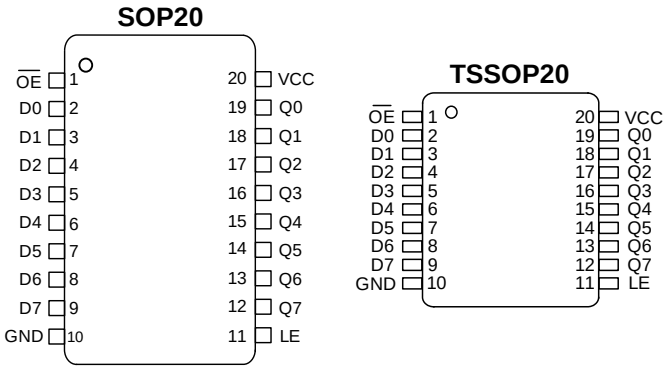


Figure 6-1 Pin configuration

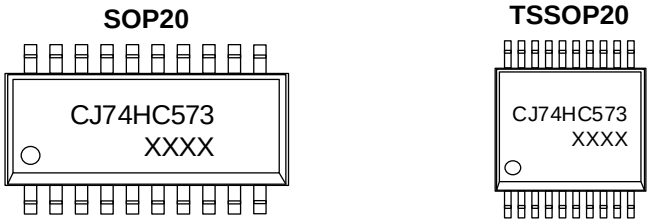
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	$\overline{OE}$	I	3-state output enable input (active LOW)
2	D0	I	Data input
3	D1	I	Data input
4	D2	I	Data input
5	D3	I	Data input
6	D4	I	Data input
7	D5	I	Data input
8	D6	I	Data input
9	D7	I	Data input
10	GND	G	Ground (0V)
11	LE	I	Latch enable input (active HIGH)
12	Q7	O	3-state latch output
13	Q6	O	3-state latch output
14	Q5	O	3-state latch output
15	Q4	O	3-state latch output
16	Q3	O	3-state latch output
17	Q2	O	3-state latch output
18	Q1	O	3-state latch output
19	Q0	O	3-state latch output
20	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

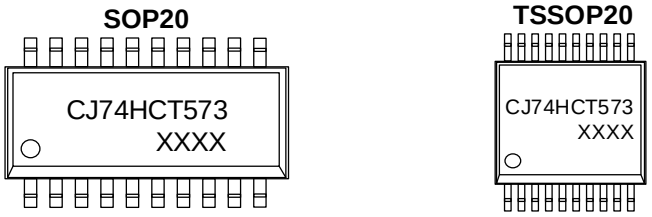
6.3 Marking Information

6.3.1 CJ74HC573



XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT573



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7.0	V
I_{IK}	Input clamping current	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
I_{OK}	Output clamping current	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
I_O	Output current	V_O= -0.5V to (V_{CC}+0.5V)		-	±35	mA
I_{CC}	Supply current	-		-	+70	mA
I_{GND}	Ground current	-		-70	-	mA
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC573						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT573						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=4.5V	-	1.67	139	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb} =25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC573							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=7.8mA; V_{CC}=6.0V	-	0.16	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND;V_{CC}=6.0V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
C_I	Input capacitance	-		-	3.5	-	pF
CJ74HCT573							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-6.0mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	0	0.1	V
			I_O=6.0mA	-	0.16	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND;V_{CC}=5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	8.0	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs	Per input pin; Dn inputs	-	35	126	uA
			Per input pin; LE input	-	65	234	uA

		at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	Per input pin; $\overline{OE}$ input	-	125	450	uA
C_I	Input capacitance	-		-	3.5	-	pF

7.4.2 DC Characteristics 2

T_{amb} =-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC573							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=7.8mA; V_{CC}=6.0V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±5.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
CJ74HCT573							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-6.0mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=6.0mA	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±5.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA

ΔI_{CC}	Additional supply current	Per input pin; $V_I=V_{CC}$-2.1V; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	Per input pin; Dn inputs	-	-	158	uA
			Per input pin; LE input	-	-	293	uA
			Per input pin; $\overline{OE}$ input	-	-	563	uA

7.4.3 DC Characteristics 3

T_{amb} =-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC573							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I=V_{IH}$ or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I=V_{IH}$ or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=7.8mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	$V_I=V_{CC}$ or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	$V_I=V_{IH}$ or V_{IL}; V_{CC}=6.0V; $V_O=V_{CC}$ or GND		-	-	±10	uA
I_{CC}	Supply current	$V_I=V_{CC}$ or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
CJ74HCT573							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I=V_{IH}$ or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-6.0mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_I=V_{IH}$ or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=6.0mA	-	-	0.4	V
I_I	Input leakage current	$V_I=V_{CC}$ or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	$V_I=V_{IH}$ or V_{IL}; V_{CC}=5.5V; $V_O=V_{CC}$ or GND		-	-	±10	uA
I_{CC}	Supply current	$V_I=V_{CC}$ or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA

ΔI_{CC}	Additional supply current	Per input pin; $V_I=V_{CC}$-2.1V; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	Per input pin; Dn inputs	-	-	172	uA
			Per input pin; LE input	-	-	319	uA
			Per input pin; $\overline{OE}$ input	-	-	613	uA

7.4.4 AC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC573							
t_{pd}	Propagation delay	Dn to Qn; See Figure 8-6	V_{CC}=2.0V	-	47	150	ns
			V_{CC}=4.5V	-	17	30	ns
			V_{CC}=5.0V; C_L=15pF	-	14	-	ns
			V_{CC}=6.0V	-	14	26	ns
		LE to Qn; See Figure 8-7	V_{CC}=2.0V	-	50	150	ns
			V_{CC}=4.5V	-	18	30	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	26	ns
t_{en}	$\overline{OE}$ to Qn enable time	See Figure 8-8	V_{CC}=2.0V	-	44	140	ns
			V_{CC}=4.5V	-	16	28	ns
			V_{CC}=6.0V	-	13	24	ns
t_{dis}	$\overline{OE}$ to Qn disable time	See Figure 8-8	V_{CC}=2.0V	-	55	150	ns
			V_{CC}=4.5V	-	20	30	ns
			V_{CC}=6.0V	-	16	26	ns
t_t	Transition time	Qn; See Figure 8-6	V_{CC}=2.0V	-	14	60	ns
			V_{CC}=4.5V	-	5	12	ns
			V_{CC}=6.0V	-	4	10	ns
t_W	Pulse width	LE HIGH; See Figure 8-7	V_{CC}=2.0V	80	-	-	ns
			V_{CC}=4.5V	16	-	-	ns
			V_{CC}=6.0V	14	-	-	ns
t_{su}	Set-up time	Dn to LE; See Figure 8-9	V_{CC}=2.0V	50	-	-	ns
			V_{CC}=4.5V	10	-	-	ns
			V_{CC}=6.0V	9	-	-	ns
t_h	Hold time	Dn to LE; See Figure 8-9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
C_{PD}	Power dissipation capacitance	C_L=50pF, f=1MHz; V_I=GND to V_{CC}		-	26	-	pF
CJ74HCT573							
t_{pd}	Propagation delay	Dn to Qn;	V_{CC}=4.5V	-	20	35	ns

		See Figure 8-6	V_{CC}=5.0V; C_L=15pF	-	17	-	ns
		LE to Qn; See Figure 8-7	V_{CC}=4.5V	-	18	35	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
t_{en}	$\overline{OE}$ to Qn enable time	V_{CC}=4.5V; See Figure 8-8		-	17	30	ns
t_{dis}	$\overline{OE}$ to Qn disable time	V_{CC}=4.5V; See Figure 8-8		-	18	30	ns
t_t	Transition time	Qn; V_{CC}=4.5V; See Figure 8-6		-	5	12	ns
t_W	Pulse width	LE HIGH; V_{CC}=4.5V; See Figure 8-7		16	-	-	ns
t_{su}	Dn to LE set-up time	V_{CC}=4.5V; See Figure 8-9		13	-	-	ns
t_h	Dn to LE hold time	V_{CC}=4.5V; See Figure 8-9		9	-	-	ns
C_{PD}	Power dissipation capacitance	C_L=50pF, f=1MHz; V_I=GND to V_{CC}-1.5V		-	26	-	pF

Note:

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_{en} is the same as t_{PZL} and t_{PZH}.

(3) t_{dis} is the same as t_{PLZ} and t_{PHZ}.

(4) t_t is the same as t_{THL} and t_{TLH}.

(5) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}xV_{CC}^2xf_ixN+\sum(C_LxV_{CC}^2xf_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_LxV_{CC}^2xf_o)$=sum of outputs.

7.4.5 AC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC573							
t_{pd}	Propagation delay	Dn to Qn; See Figure 8-6	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
		LE to Qn; See Figure 8-7	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
t_{en}	$\overline{OE}$ to Qn enable time	See Figure 8-8	V_{CC}=2.0V	-	-	175	ns
			V_{CC}=4.5V	-	-	35	ns
			V_{CC}=6.0V	-	-	30	ns
t_{dis}	$\overline{OE}$ to Qn disable time	See Figure 8-8	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns

t_t	Transition time	Qn; See Figure 8-6	V_{CC}=2.0V	-	-	75	ns
			V_{CC}=4.5V	-	-	15	ns
			V_{CC}=6.0V	-	-	13	ns
t_W	Pulse width	LE HIGH; See Figure 8-7	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
t_{su}	Set-up time	Dn to LE; See Figure 8-9	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
t_h	Hold time	Dn to LE; See Figure 8-9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
CJ74HCT573							
t_{pd}	Propagation delay	Dn to Qn; See Figure 8-6	V_{CC}=4.5V	-	-	44	ns
		LE to Qn; See Figure 8-7	V_{CC}=4.5V	-	-	44	ns
t_{en}	$\overline{OE}$ to Qn enable time	V_{CC}=4.5V; See Figure 8-8		-	-	38	ns
t_{dis}	$\overline{OE}$ to Qn disable time	V_{CC}=4.5V; See Figure 8-8		-	-	38	ns
t_t	Transition time	Qn; V_{CC}=4.5V; See Figure 8-6		-	-	15	ns
t_W	Pulse width	LE HIGH; V_{CC}=4.5V; See Figure 8-7		20	-	-	ns
t_{su}	Dn to LE set-up time	V_{CC}=4.5V; See Figure 8-9		16	-	-	ns
t_h	Dn to LE hold time	V_{CC}=4.5V; See Figure 8-9		11	-	-	ns

Note:

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_{en} is the same as t_{PZL} and t_{PZH}.

(3) t_{dis} is the same as t_{PLZ} and t_{PHZ}.

(4) t_t is the same as t_{THL} and t_{TLH}.

7.4.6 AC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC573							
t_{pd}	Propagation delay	Dn to Qn; See Figure 8-6	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
		LE to Qn; See Figure 8-7	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
t_{en}	$\overline{OE}$ to Qn enable	See Figure 8-8	V_{CC}=2.0V	-	-	210	ns

	time		V_{CC}=4.5V	-	-	42	ns
			V_{CC}=6.0V	-	-	36	ns
t_{dis}	$\overline{OE}$ to Qn disable time	See Figure 8-8	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
t_t	Transition time	Qn; See Figure 8-6	V_{CC}=2.0V	-	-	90	ns
			V_{CC}=4.5V	-	-	18	ns
			V_{CC}=6.0V	-	-	15	ns
t_W	Pulse width	LE HIGH; See Figure 8-7	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
t_{su}	Set-up time	Dn to LE; See Figure 8-9	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
t_h	Hold time	Dn to LE; See Figure 8-9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
CJ74HCT573							
t_{pd}	Propagation delay	Dn to Qn; See Figure 8-6	V_{CC}=4.5V	-	-	53	ns
		LE to Qn; See Figure 8-7	V_{CC}=4.5V	-	-	53	ns
t_{en}	$\overline{OE}$ to Qn enable time	V_{CC}=4.5V; See Figure 8-8		-	-	45	ns
t_{dis}	$\overline{OE}$ to Qn disable time	V_{CC}=4.5V; See Figure 8-8		-	-	45	ns
t_t	Transition time	Qn; V_{CC}=4.5V; See Figure 8-6		-	-	18	ns
t_W	Pulse width	LE HIGH; V_{CC}=4.5V; See Figure 8-7		24	-	-	ns
t_{su}	Dn to LE set-up time	V_{CC}=4.5V; See Figure 8-9		20	-	-	ns
t_h	Dn to LE hold time	V_{CC}=4.5V; See Figure 8-9		15	-	-	ns

Note:

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_{en} is the same as t_{PZL} and t_{PZH}.

(3) t_{dis} is the same as t_{PLZ} and t_{PHZ}.

(4) t_t is the same as t_{THL} and t_{TLH}.

8 Detailed Description

8.1 Overview

The CJ74HC/HCT573 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable (/OE) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on /OE causes the outputs to assume a high-impedance OFF-state. Operation of the /OE input does not affect the state of the latches. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

8.2 Functional Block Diagram

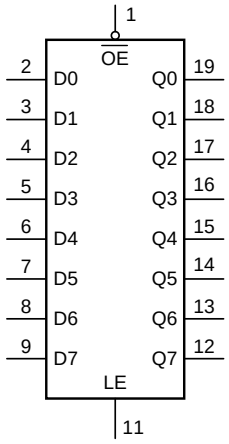


Figure 8-1 Logic symbol

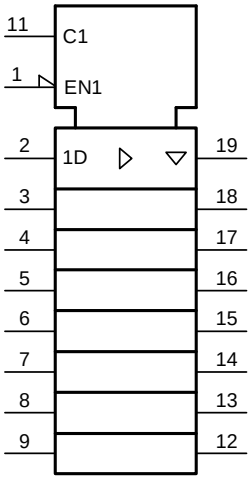


Figure 8-2 IEC logic symbol

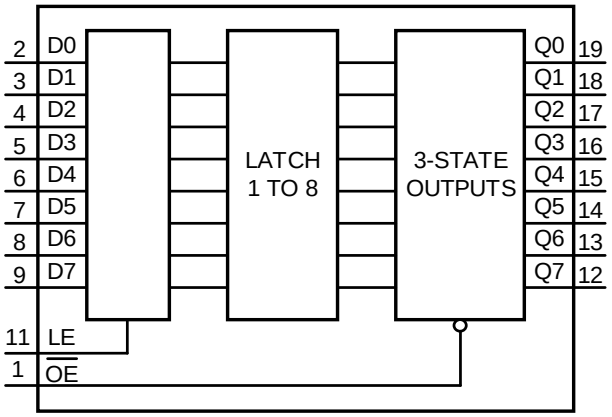


Figure 8-3 Functional diagram

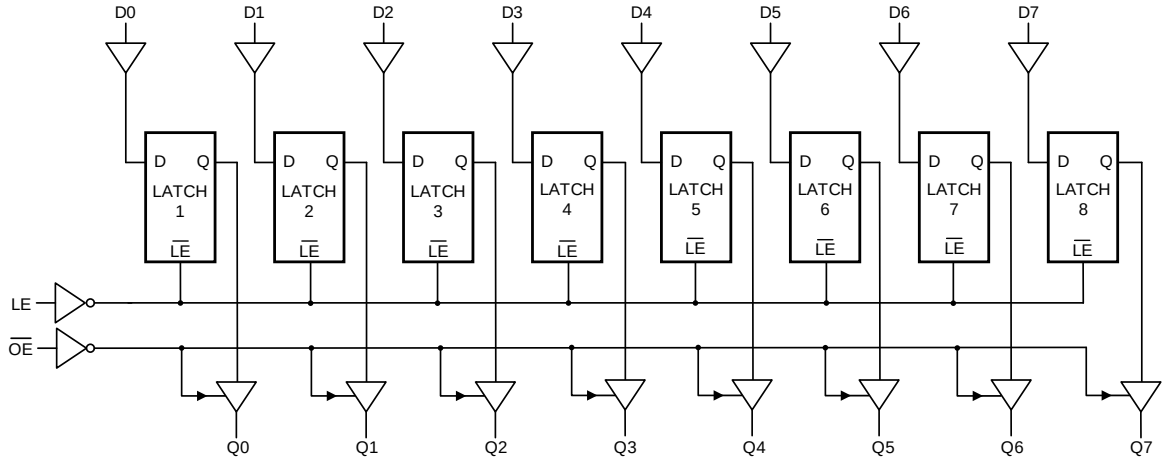


Figure 8-4 Logic diagram

8.3 Function Table

OPERATING MODE	CONTROL		INPUT	INTERNAL LATCHES	OUTPUT
	$\overline{OE}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

Note:

(1) H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state;

(2) h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;

(3) l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

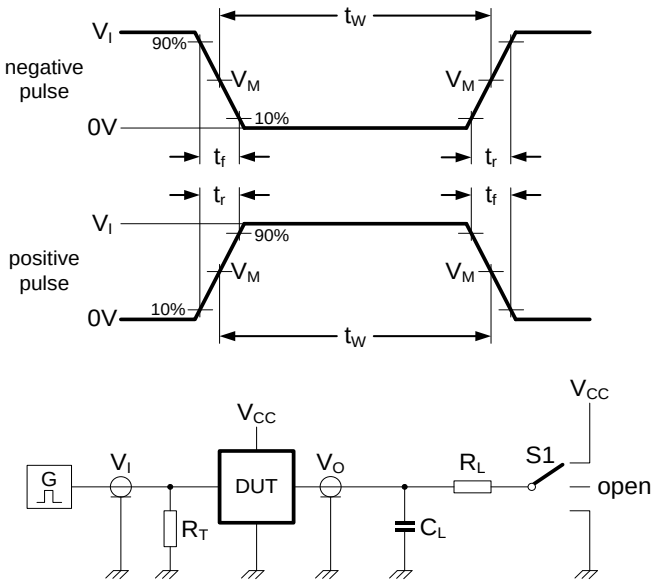


Figure 8-5 Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

8.4.2 AC Testing Waveforms

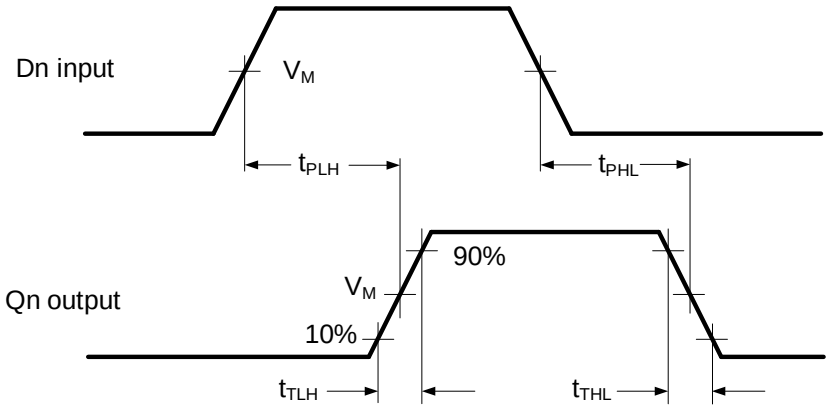


Figure 8-6 Propagation delay data input (Dn) to output (Qn) and output transition time

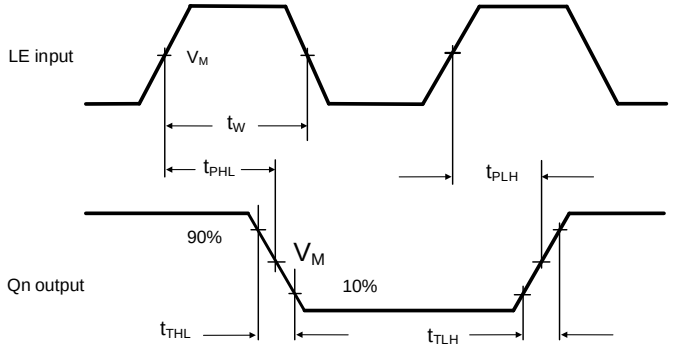


Figure 8-7 Pulse width latch enable input (LE), propagation delay latch enable input (LE) to output (Qn) and output transition time

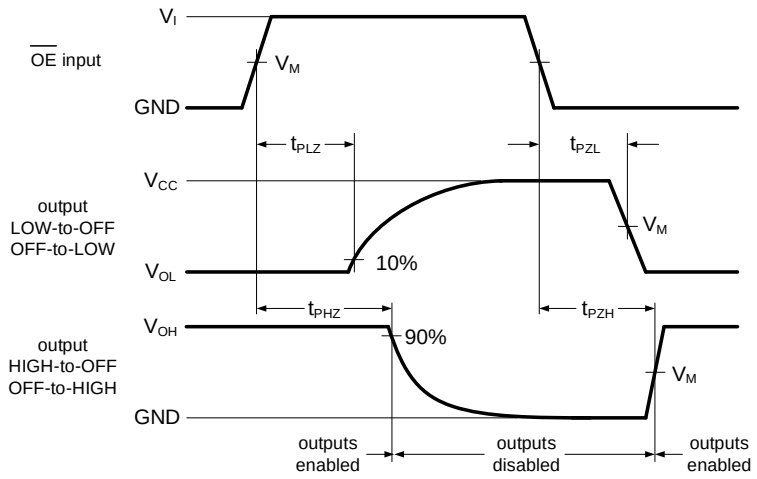


Figure 8-8 Enable and disable times

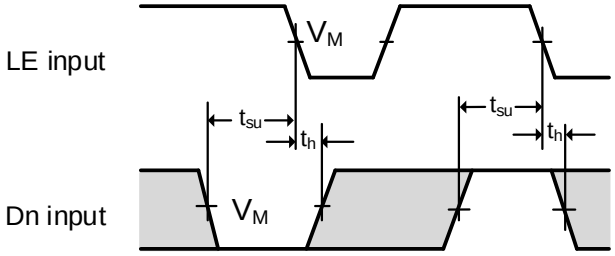


Figure 8-9 Set-up and hold times for data input (Dn) to latch input (LE)

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT
	V_M	V_M
CJ74HC573	0.5xV_{CC}	0.5xV_{CC}
CJ74HCT573	1.3V	1.3V

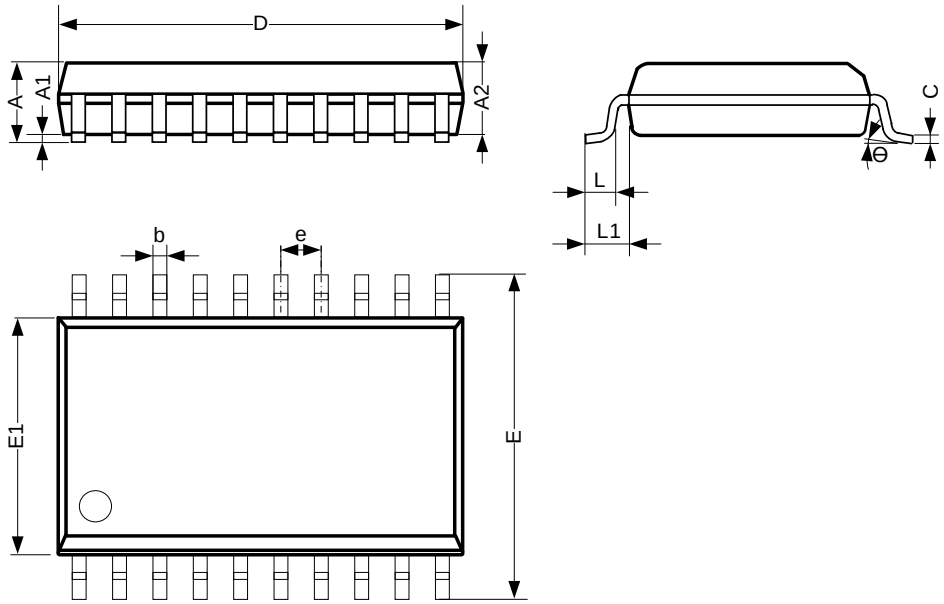
8.4.4 Test Data

TYPE	INPUT		LOAD		S1 POSITION		
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
CJ74HC573	V_{CC}	6ns	15pF,50pF	1kΩ	Open	GND	V_{CC}
CJ74HCT573	3V	6ns	15pF,50pF	1kΩ	Open	GND	V_{CC}

9 Mechanical Information

9.1 SOP20 Mechanical Information

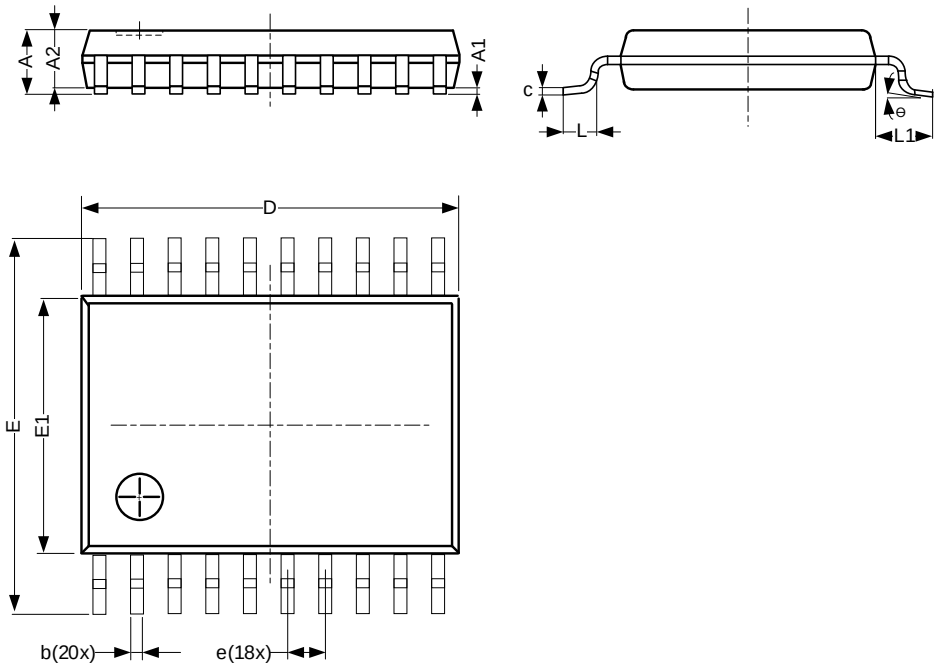
9.1.1 SOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	2.47	-	2.65
A1	0.05	-	0.30
A2	2.20	-	2.44
b	0.35	-	0.50
c	0.15	-	0.30
D	12.54	-	12.94
E	10.00	-	10.60
E1	7.30	-	7.70
e	1.27 BSC		
L	0.40	-	1.05
L1	1.30	-	1.50
θ	0°	-	8°
Unit: mm			

9.2 TSSOP20 Mechanical Information

9.2.1 TSSOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	-	6.60
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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