8-Bit Serial or Parallel-Input/Serial-Output Shift Register with 3-State Output

CJ74HC589 Logic

1 Introduction

The CJ74HC589 device consists of an 8−bit storage latch which feeds parallel data to an 8−bit shift register.Inputs include clamp diodes. It enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC589	SOP16
	TSSOP16

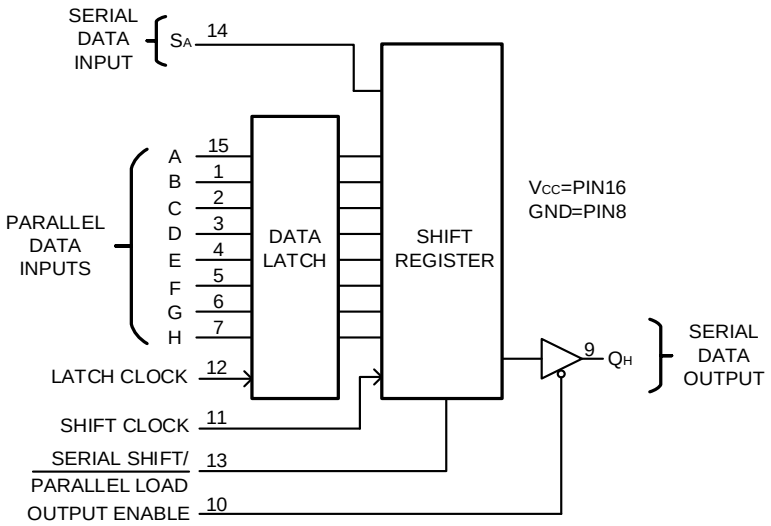
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Supply voltage range from 2.0 to 6.0 V
- Specified from -40°C to +125°C

4 Applications

- LED displays
- Network switches



Logic Diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC589AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC589BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

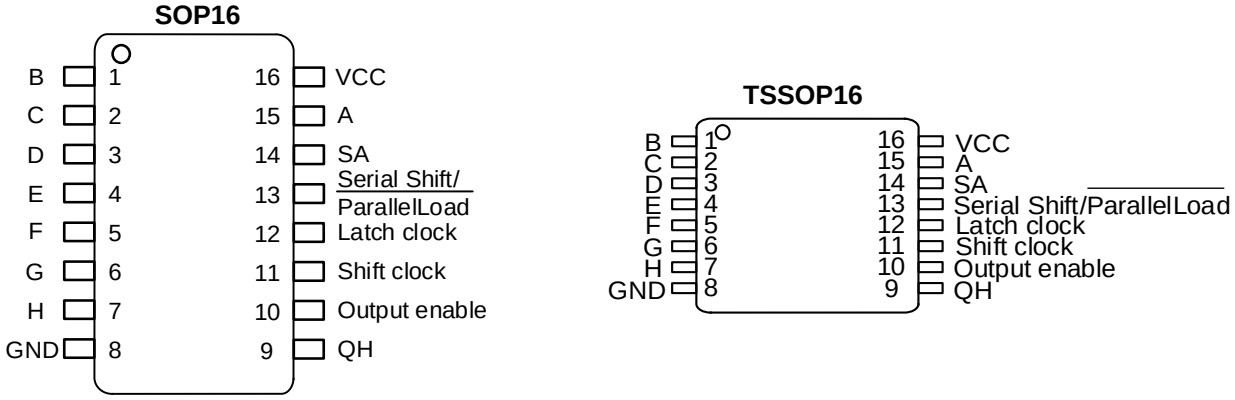


Figure 6-1 Pin Configuration

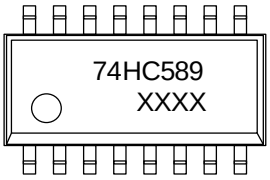
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	B	I	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
2	C	I	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
3	D	I	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
4	E	I	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
5	F	I	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
6	G	I	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
7	H	I	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
8	GND	G	Ground (0V)
9	QH	O	Serial data output. This pin is the output from the last stage of the shift register. This is a 3−state output.
10	Output Enable	I	Active−low output enable A high level applied to this pin forces the QH output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.
11	Shift Clock	I	Serial shift clock. A low−to−high transition on this input shifts data on the serial data input into the shift register and data in stage H is shifted out QH, being replaced by the data previously stored in stage G.
12	Latch Clock	I	Data latch clock. A low−to−high transition on this input loads the parallel data on inputs A−H into the data latch.
13	Serial Shift/ $\overline{\text{ParallelLoad}}$	I	Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.
14	SA	I	Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/$\overline{\text{ParallelLoad}}$ is high. Data on this input is ignored when Serial Shift/$\overline{\text{ParallelLoad}}$ is low.
15	A	I	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
16	VCC	P	Supply voltage

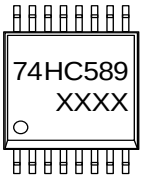
(1) I-Input, O-Output, P-Power, G-Ground.

6.3 Marking Information

SOP16



TSSOP16



74HC589: Device number.

XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

T_{amb}=25°C, All voltage referenced to GND, unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7.0	V
V_I	Input voltage	-		-0.5	V_{CC}+0.5	V
V_O	Output voltage	-		-0.5	V_{CC}+0.5	V
I_I	Input current	-		-	±20	mA
I_O	Output current	-		-	±35	mA
I_{CC}	Supply current	-		-	+75	mA
I_{GND}	Ground current	-		-	+75	mA
T_{stg}	Storage temperature	-		-65	+150	°C
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	Typ.	MAX.	UNIT
V_{CC}	Supply voltage	-	2.0	-	6.0	V
$V_{I/O}$	Input/output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±4000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Minimum HIGH-level input voltage	V_{CC}=2.0V	1.5	-	-	V
		V_{CC}=4.5V	3.15	-	-	V
		V_{CC}=6.0V	4.2	-	-	V
V_{IL}	Maximum LOW-level input voltage	V_{CC}=2.0V	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	V
V_{OH}	Minimum HIGH-level	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V

	output voltage	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
		I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
		I_O=-6.0mA; V_{CC}=4.5V	3.84	3.98	-	V
		I_O=-7.8mA; V_{CC}=6.0V	5.34	5.48	-	V
V_{OL}	Maximum LOW-level output voltage	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
		I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
		I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
		I_O=6.0mA; V_{CC}=4.5V	-	0.26	0.33	V
		I_O=7.8mA; V_{CC}=6.0V	-	0.26	0.33	V
I_I	Maximum input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V	-	-	±1.0	uA
I_{OZ}	Maximum three-state leakage current	V_I=V_{IL} or V_{IH}; V_O=V_{CC} or GND; V_{CC}=6.0V	-	-	±5.0	uA
I_{CC}	Maximum quiescent supply current	V_I=V_{CC} or GND; I_O=0uA; V_{CC}=6.0V	-	-	40	uA

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Minimum HIGH-level input voltage	V_{CC}=2.0V	1.5	-	-	V
		V_{CC}=4.5V	3.15	-	-	V
		V_{CC}=6.0V	4.2	-	-	V
V_{IL}	Maximum LOW-level input voltage	V_{CC}=2.0V	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	V
V_{OH}	Minimum HIGH-level output voltage	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
		I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
		I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
		I_O=-6.0mA; V_{CC}=4.5V	3.70	-	-	V
		I_O=-7.8mA; V_{CC}=6.0V	5.20	-	-	V
V_{OL}	Maximum LOW-level output voltage	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
		I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
		I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
		I_O=6.0mA; V_{CC}=4.5V	-	-	0.40	V
		I_O=7.8mA; V_{CC}=6.0V	-	-	0.40	V
I_I	Maximum input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V	-	-	±1.0	uA
I_{OZ}	Maximum three-state leakage current	V_I=V_{IL} or V_{IH}; V_O=V_{CC} or GND; V_{CC}=6.0V	-	-	±10	uA
I_{CC}	Maximum quiescent supply current	V_I=V_{CC} or GND; I_O=0uA; V_{CC}=6.0V	-	-	160	uA

7.4.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, C_L=50pF, input t_r=t_f=6ns, unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS		MIN.	TYP.	MAX.	UNIT
f_{max}	Maximum clock frequency (50% duty cycle)	See Figure 8-3 and Figure 8-6	V_{CC}=2.0V	4.8	6	-	MHz
			V_{CC}=4.5V	24	30	-	MHz
			V_{CC}=6.0V	28	35	-	MHz
t_{PLH}, t_{PHL}	Maximum propagation delay	Latch clock to Q_H, see Figure 8-3 and Figure 8-5	V_{CC}=2.0V	-	175	225	ns
			V_{CC}=4.5V	-	40	50	ns
			V_{CC}=6.0V	-	30	40	ns
t_{PLH}, t_{PHL}	Maximum propagation delay	Shift clock to Q_H, see Figure 8-3 and Figure 8-6	V_{CC}=2.0V	-	160	200	ns
			V_{CC}=4.5V	-	30	40	ns
			V_{CC}=6.0V	-	25	30	ns
		Serial shift/$\overline{\text{Parallel Load}}$ to Q_H, see Figure 8-3 and Figure 8-8	V_{CC}=2.0V	-	160	200	ns
			V_{CC}=4.5V	-	30	40	ns
			V_{CC}=6.0V	-	25	30	ns
t_{PLZ}, t_{PHZ}	Maximum propagation delay	Output enable to Q_H, see Figure 8-4 and Figure 8-7	V_{CC}=2.0V	-	150	170	ns
			V_{CC}=4.5V	-	27	30	ns
			V_{CC}=6.0V	-	23	25	ns
t_{PZL}, t_{PZH}	Maximum propagation delay	Output enable to Q_H, see Figure 8-4 and Figure 8-7	V_{CC}=2.0V	-	150	170	ns
			V_{CC}=4.5V	-	27	30	ns
			V_{CC}=6.0V	-	23	25	ns
t_{TLH}, t_{THL}	Maximum output transition time	Any output, see Figure 8-3 and Figure 8-5	V_{CC}=2.0V	-	60	75	ns
			V_{CC}=4.5V	-	12	15	ns
			V_{CC}=6.0V	-	10	13	ns
t_{su}	Minimum setup time	A-H to latch clock, see Figure 8-9	V_{CC}=2.0V	125	100	-	ns
			V_{CC}=4.5V	25	20	-	ns
			V_{CC}=6.0V	21	17	-	ns
		Serial data input S_A to shift clock, see Figure 8-10	V_{CC}=2.0V	125	100	-	ns
			V_{CC}=4.5V	25	20	-	ns
			V_{CC}=6.0V	21	17	-	ns
		Serial shift/$\overline{\text{Parallel Load}}$ to shift clock, see Figure 8-11	V_{CC}=2.0V	125	100	-	ns
			V_{CC}=4.5V	25	20	-	ns
			V_{CC}=6.0V	21	17	-	ns
t_h	Minimum hold time	Latch clock to A-H, see Figure 8-9	V_{CC}=2.0V	30	25	-	ns
			V_{CC}=4.5V	6	5	-	ns
			V_{CC}=6.0V	6	5	-	ns
		Shift clock to serial data input S_A, see Figure 8-10	V_{CC}=2.0V	5	5	-	ns
			V_{CC}=4.5V	5	5	-	ns

			V_{CC}=6.0V	5	5	-	ns
t_W	Minimum pulse width	Shift clock, see Figure 8-6	V_{CC}=2.0V	95	75	-	ns
			V_{CC}=4.5V	19	15	-	ns
			V_{CC}=6.0V	16	13	-	ns
		Latch clock, see Figure 8-5	V_{CC}=2.0V	100	80	-	ns
			V_{CC}=4.5V	20	16	-	ns
			V_{CC}=6.0V	17	14	-	ns
		Serial shift/$\overline{\text{ParallelLoad}}$, see Figure 8-8	V_{CC}=2.0V	100	80	-	ns
			V_{CC}=4.5V	20	16	-	ns
			V_{CC}=6.0V	17	14	-	ns
t_r, t_f	Maximum input rise and fall time	See Figure 8-5	V_{CC}=2.0V	-	-	1000	ns
			V_{CC}=4.5V	-	-	500	ns
			V_{CC}=6.0V	-	-	400	ns

7.4.4 AC Characteristics 2

T_{amb}=-40°C to +125°C, C_L=50pF, input t_r=t_f=6ns, unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS		MIN.	TYP.	MAX.	UNIT
f_{max}	Maximum clock frequency (50% duty cycle)	See Figure 8-3 and Figure 8-6	V_{CC}=2.0V	4	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
t_{PLH}, t_{PHL}	Maximum propagation delay	Latch clock to Q_H, see Figure 8-3 and Figure 8-5	V_{CC}=2.0V	-	-	275	ns
			V_{CC}=4.5V	-	-	60	ns
			V_{CC}=6.0V	-	-	50	ns
t_{PLH}, t_{PHL}	Maximum propagation delay	Shift clock to Q_H, see Figure 8-3 and Figure 8-6	V_{CC}=2.0V	-	-	240	ns
			V_{CC}=4.5V	-	-	48	ns
			V_{CC}=6.0V	-	-	40	ns
		Serial shift/$\overline{\text{ParallelLoad}}$ to Q_H, see Figure 8-3 and Figure 8-8	V_{CC}=2.0V	-	-	240	ns
			V_{CC}=4.5V	-	-	48	ns
			V_{CC}=6.0V	-	-	40	ns
t_{PLZ}, t_{PHZ}	Maximum propagation delay	Output enable to Q_H, see Figure 8-4 and Figure 8-7	V_{CC}=2.0V	-	-	200	ns
			V_{CC}=4.5V	-	-	40	ns
			V_{CC}=6.0V	-	-	30	ns
t_{PZL}, t_{PZH}	Maximum propagation delay	Output enable to Q_H, see Figure 8-4 and Figure 8-7	V_{CC}=2.0V	-	-	200	ns
			V_{CC}=4.5V	-	-	40	ns
			V_{CC}=6.0V	-	-	30	ns
t_{TLH}, t_{THL}	Maximum output transition time	Any output, see Figure 8-3 and Figure 8-5	V_{CC}=2.0V	-	-	90	ns
			V_{CC}=4.5V	-	-	18	ns
			V_{CC}=6.0V	-	-	15	ns

t_{su}	Minimum setup time	A-H to latch clock, see Figure 8-9	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		Serial data input S_A to shift clock, see Figure 8-10	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		Serial shift/$\overline{\text{ParallelLoad}}$ to shift clock, see Figure 8-11	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
t_h	Minimum hold time	Latch clock to A-H, see Figure 8-9	V_{CC}=2.0V	40	-	-	ns
			V_{CC}=4.5V	8	-	-	ns
			V_{CC}=6.0V	7	-	-	ns
		Shift clock to serial data input S_A, see Figure 8-10	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
t_W	Minimum pulse width	Shift clock, see Figure 8-6	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	23	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
		Latch clock, see Figure 8-5	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		Serial shift/$\overline{\text{ParallelLoad}}$, see Figure 8-8	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns

8 Detailed Description

8.1 Overview

The CJ74HC589 device consists of an 8−bit storage latch which feeds parallel data to an 8−bit shift register.Inputs include clamp diodes. It enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

8.2 Functional Block Diagram

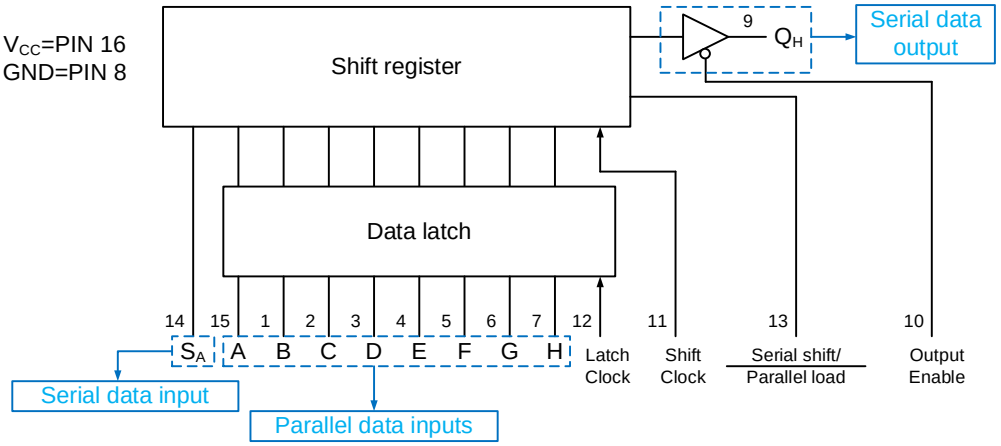
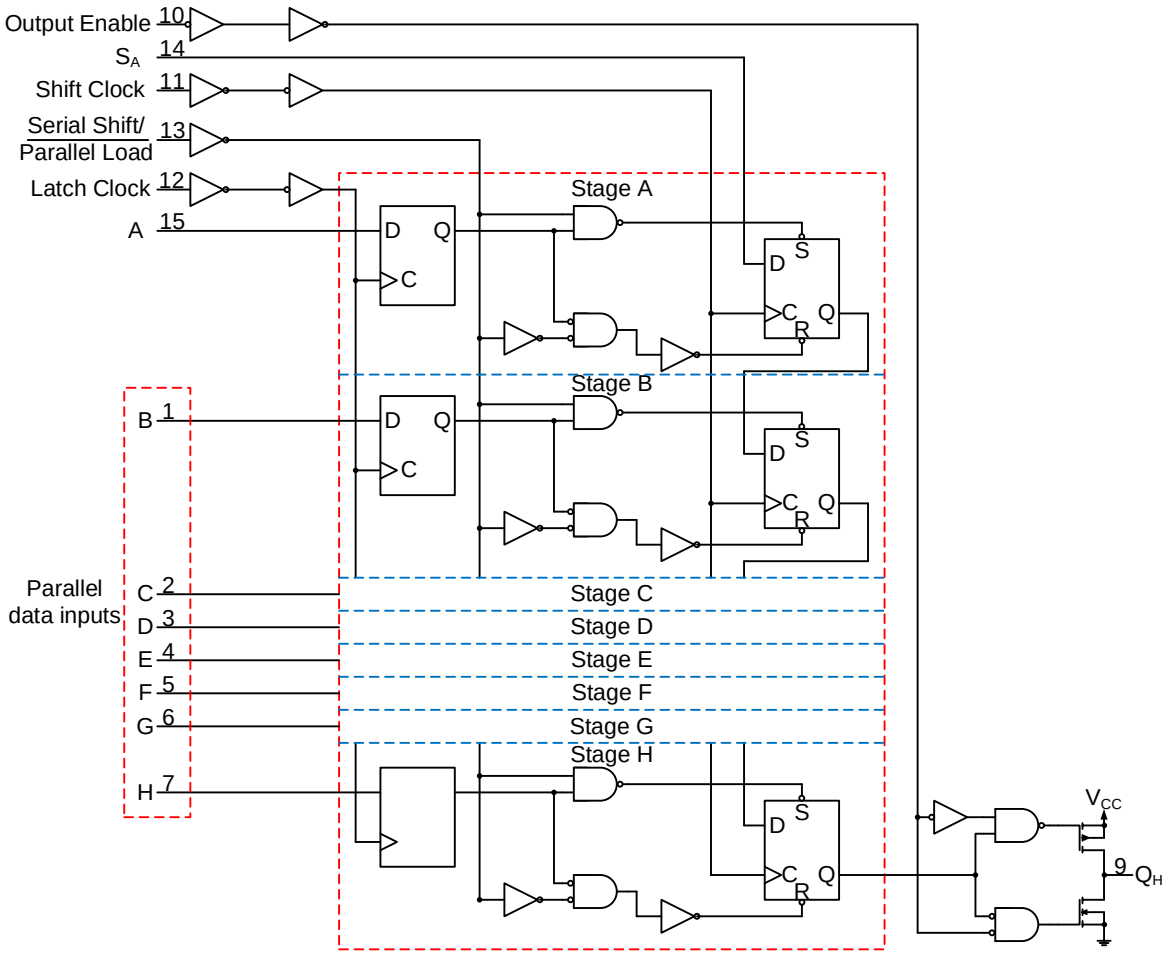


Figure 8-1 Logic diagram



*Stages C thru G (not shown in detail) are identical to stages A and B above.

Figure 8-2 Logic detail

8.3 Function Table(1)

OPERATION	INPUTS						RESULTING FUNCTION		
	Output Enable	Serial Shift/ ParallelLoad	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A-H	Data Latch Contents	Shift Register Contents	Output Q_H
Force output into high impedance state	H	X	X	X	X	X	X	X	Z
Load parallel data into data latch	L	H	⎍	L, H, ⎎	X	a-h	a-h	U	U
Transfer latch contents to shift register	L	L	L, H, ⎎	X	X	X	U	$LR_N \rightarrow SR_N$	LR_H
Contents of Input latch and shift register are unchanged	L	H	L, H, ⎎	L, H, ⎎	X	X	U	U	U
Load parallel data into data latch and shift register	L	L	⎍	X	X	a-h	a-h	a-h	h
Shift serial data into shift register	L	H	X	⎍	D	X	*	SR_A=D, $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$
Load parallel data in data latch and shift serial data into shift register	L	H	⎍	⎍	D	a-h	a-h	SR_A=D, $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$

(1) LR=latch register contents
SR=shift register contents
a-h=data at parallel data inputs A-H
D=data (L, H) at serial data input SA
U=remains unchanged
X=don't care
Z=high impedance
*=depends on Latch Clock input

8.4 Testing Circuit

8.4.1 AC Testing Circuit

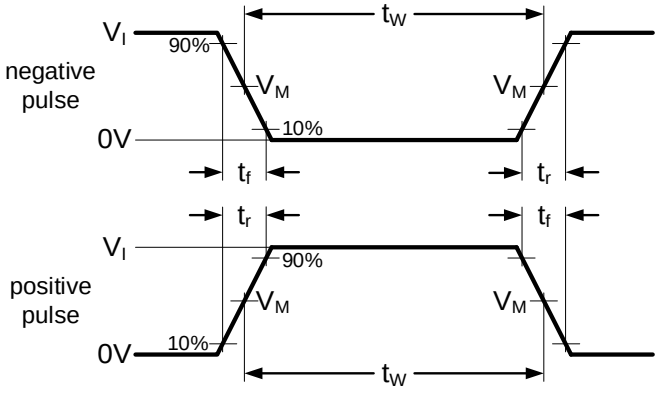


Figure 8-3

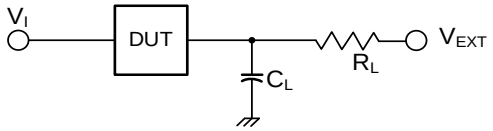


Figure 8-4 Test circuit for measuring switching times

Definitions for test circuit:

C_L includes probe and jig capacitance.

8.4.2 AC Testing Waveforms

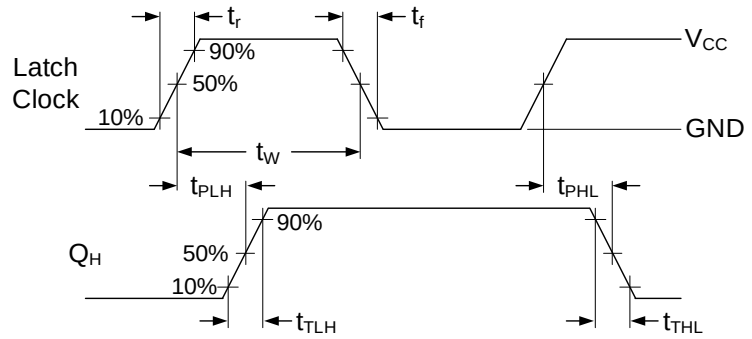


Figure 8-5 Serial Shift/$\overline{\text{ParallelLoad}}$=L

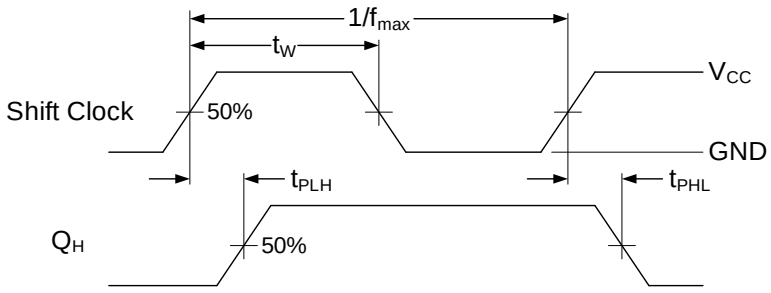


Figure 8-6 Serial Shift/$\overline{\text{ParallelLoad}}$=H

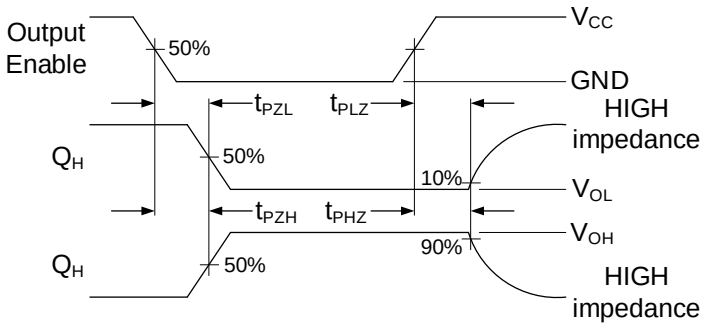


Figure 8-7

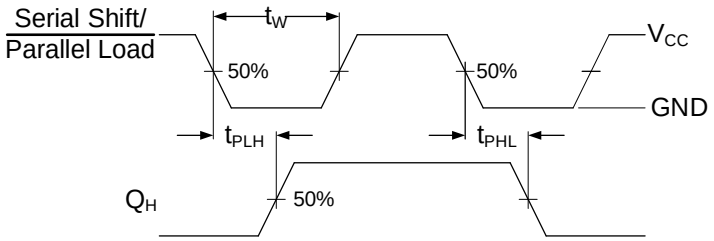


Figure 8-8

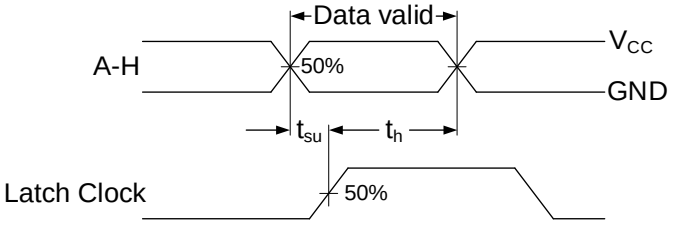


Figure 8-9

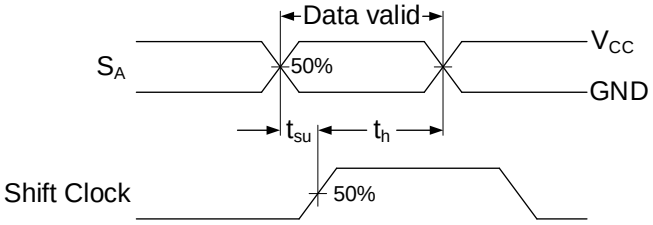


Figure 8-10

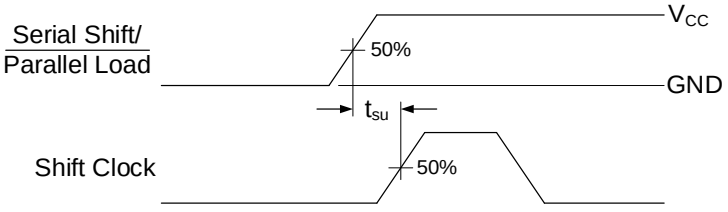


Figure 8-11

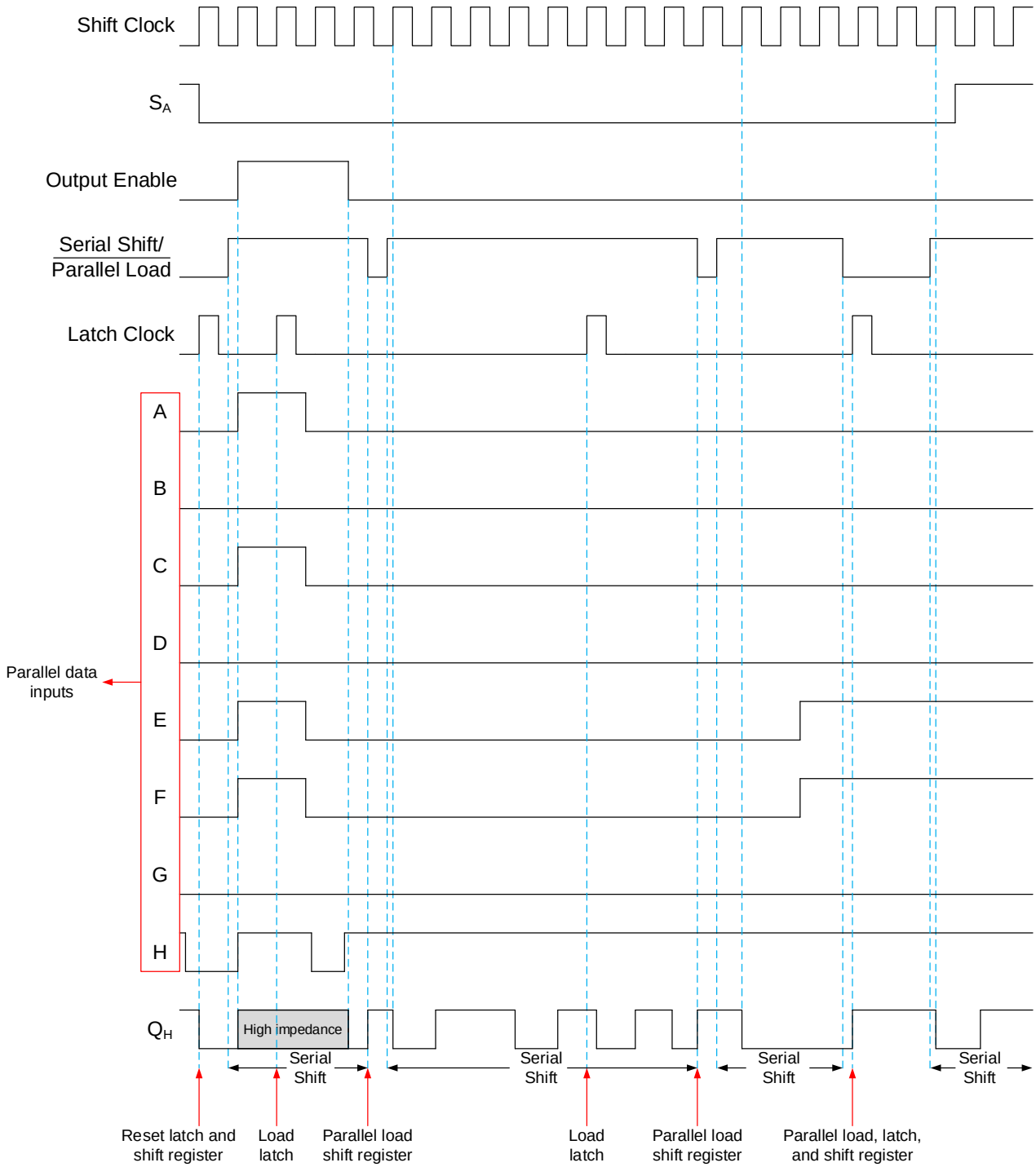


Figure 8-12 Timing Diagram

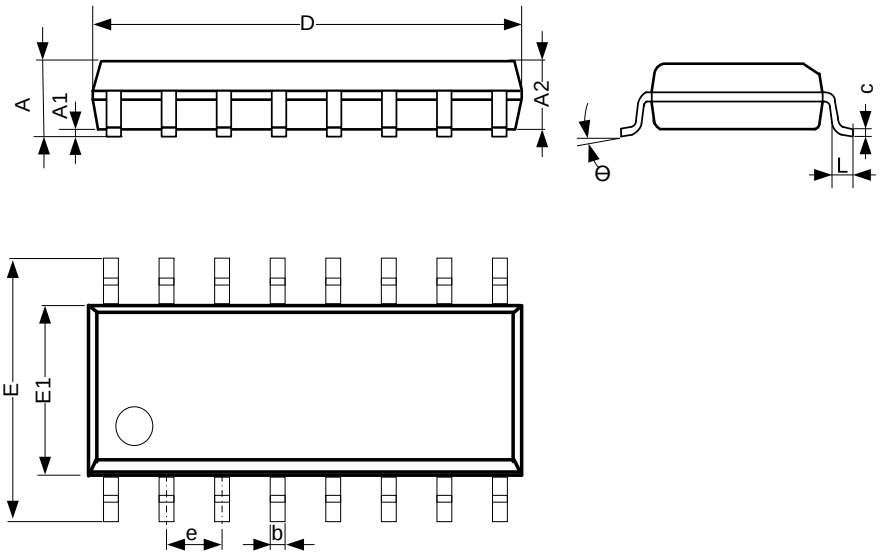
8.4.3 Test Data

TYPE	INPUT		LOAD		S1 POSITION		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
CJ74HC589	V_{CC}	3.0ns	50pF	1kΩ	Open	V_{CC}	GND

9 Mechanical Information

9.1 SOP16 Mechanical Information

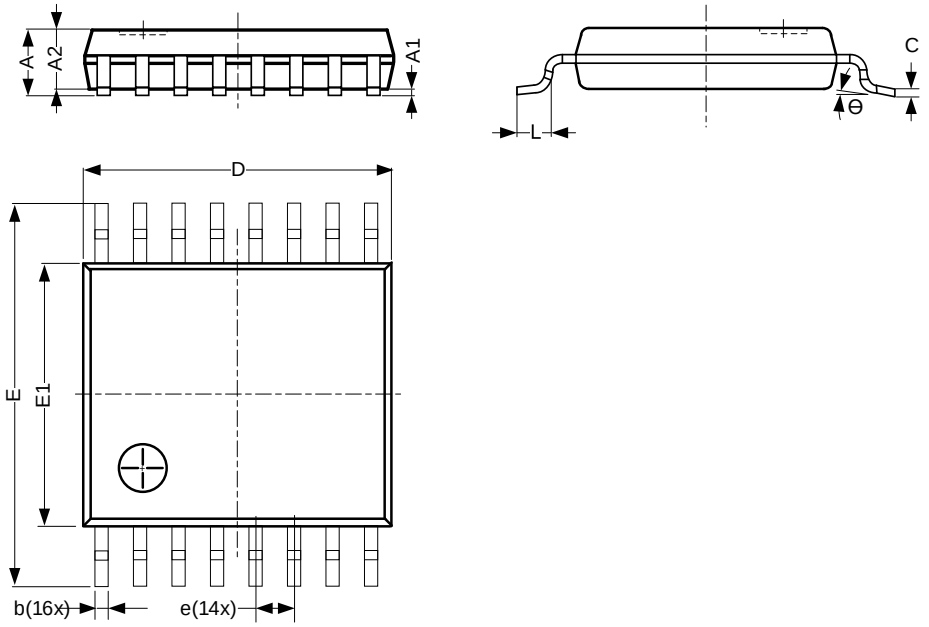
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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