8-bit Shift Register with Input Flip-flops

CJ74HC/HCT597 Logic

1 Introduction

The CJ74HC597/74HCT597 is an 8-bit shift register with input flip-flops.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC597	SOP16
	TSSOP16
CJ74HCT597	SOP16
	TSSOP16

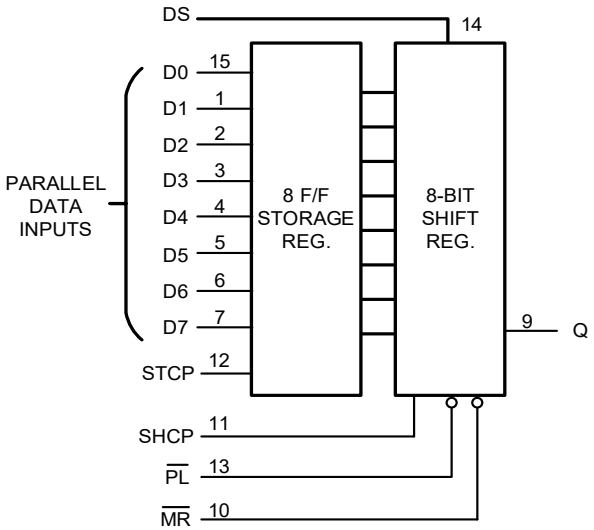
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Supply voltage range:
  - CJ74HC597: 2~6V
  - CJ74HCT597: 4.5~5.5V
- Input levels:
  - CJ74HC597: CMOS level
  - CJ74HCT597: TTL level
- Temperature range: -40°C to +125°C

4 Applications

- Increase the number of inputs on a microcontroller



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC597AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT597AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC597BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74HCT597BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

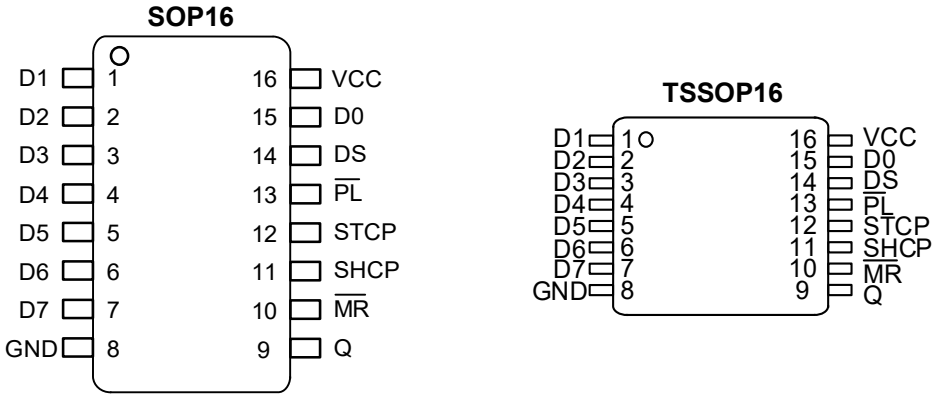


Figure 6-1 Pin configuration

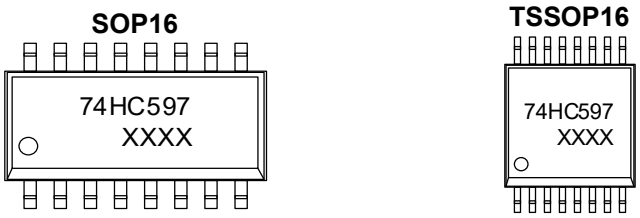
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	D1	I	Parallel data input
2	D2	I	Parallel data input
3	D3	I	Parallel data input
4	D4	I	Parallel data input
5	D5	I	Parallel data input
6	D6	I	Parallel data input
7	D7	I	Parallel data input
8	GND	G	Ground (0V)
9	Q	O	Serial data output
10	$\overline{MR}$	I	Asynchronous master reset input (active LOW)
11	SHCP	I	Shift register clock input (LOW-to-HIGH, edge-triggered)
12	STCP	I	Storage register clock input (LOW-to-HIGH, edge-triggered)
13	$\overline{PL}$	I	Parallel load input (active LOW)
14	DS	I	Serial data input
15	D0	I	Parallel data inputs
16	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground.

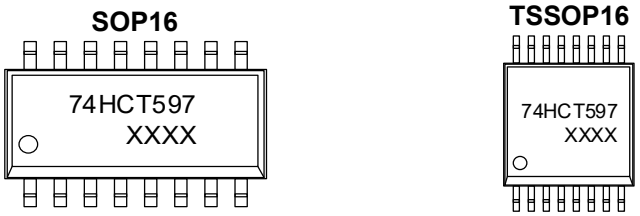
6.3 Marking Information

6.3.1 CJ74HC597



XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT597



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND(ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7.0	V
I_{CC}	Supply current	-		-	+50	mA
I_{GND}	Ground current	-		-50	-	mA
I_{IK}	Input clamping current	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
I_{OK}	Output clamping current	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
I_O	Output current	-0.5V < V_O < V_{CC}+0.5V		-	±25	mA
T_{stg}	Storage temperature	-		-65	+150	°C
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC597						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT597						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±1000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC597						
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V	1.5	-	-	V
		V_{CC}=4.5V	3.15	-	-	V
		V_{CC}=6.0V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
		I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
		I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
		I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
		I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	-	V
V_{OL}	LOW-level output voltage	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
		I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
		I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
		I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
		I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V	-	-	±2	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V	-	-	80	uA
CJ74HCT597						
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
		I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
V_{OL}	LOW-level output voltage	I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
		I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V	-	-	±2	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V	-	-	80	uA
ΔI_{CC}	Additional supply current	One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	-	-	135	uA

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC597						
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V	1.5	-	-	V
		V_{CC}=4.5V	3.15	-	-	V
		V_{CC}=6.0V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
		I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
		I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
		I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
		I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
		I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
		I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
		I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
		I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V	-	-	±4	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V	-	-	160	uA
CJ74HCT597						
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
		I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
V_{OL}	LOW-level output voltage	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
		I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V	-	-	±4	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V	-	-	160	uA
ΔI_{CC}	Additional supply current	One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	-	-	147	uA

7.4.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC597							
t_{PLH}, t_{PHL}	SHCP to Q propagation delay	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	55	220	ns
			V_{CC}=4.5V; C_L=50pF	-	20	44	ns
			V_{CC}=5.0V; C_L=15pF	-	17	-	ns
			V_{CC}=6.0V; C_L=50pF	-	16	37	ns
	$\overline{MR}$ to Q propagation delay	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	-	58	220	ns
			V_{CC}=4.5V; C_L=50pF	-	21	44	ns
			V_{CC}=6.0V; C_L=50pF	-	17	37	ns
	STCP to Q propagation delay	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	80	315	ns
			V_{CC}=4.5V; C_L=50pF	-	29	63	ns
			V_{CC}=5.0V; C_L=15pF	-	25	-	ns
			V_{CC}=6.0V; C_L=50pF	-	23	54	ns
	$\overline{PL}$ to Q propagation delay	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	-	69	270	ns
			V_{CC}=4.5V; C_L=50pF	-	25	54	ns
			V_{CC}=5.0V; C_L=15pF	-	21	-	ns
			V_{CC}=6.0V; C_L=50pF	-	20	46	ns
t_t	Transition time	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	19	95	ns
			V_{CC}=4.5V; C_L=50pF	-	7	19	ns
			V_{CC}=6.0V; C_L=50pF	-	6	16	ns
t_W	STCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	100	-	-	ns
			V_{CC}=4.5V; C_L=50pF	20	-	-	ns
			V_{CC}=6.0V; C_L=50pF	17	-	-	ns
	SHCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	100	-	-	ns
			V_{CC}=4.5V; C_L=50pF	20	-	-	ns
			V_{CC}=6.0V; C_L=50pF	17	-	-	ns
	$\overline{MR}$ LOW	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	100	-	-	ns
			V_{CC}=4.5V; C_L=50pF	20	-	-	ns
			V_{CC}=6.0V; C_L=50pF	17	-	-	ns
	$\overline{PL}$ LOW	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	100	-	-	ns
			V_{CC}=4.5V; C_L=50pF	20	-	-	ns
			V_{CC}=6.0V; C_L=50pF	17	-	-	ns
t_{su}	Dn to STCP Set_up time	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	75	-	-	ns
			V_{CC}=4.5V; C_L=50pF	15	-	-	ns
			V_{CC}=6.0V; C_L=50pF	13	-	-	ns
	DS to SHCP	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	75	-	-	ns

	Set_up time		V_{CC}=4.5V; C_L=50pF	15	-	-	ns
			V_{CC}=6.0V; C_L=50pF	13	-	-	ns
	$\overline{PL}$ to SHCP Set_up time	See Figure 8-8	V_{CC}=2.0V; C_L=50pF	75	-	-	ns
			V_{CC}=4.5V; C_L=50pF	15	-	-	ns
			V_{CC}=6.0V; C_L=50pF	13	-	-	ns
t_h	Dn to STCP hold time	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	5	-	-	ns
			V_{CC}=4.5V; C_L=50pF	5	-	-	ns
			V_{CC}=6.0V; C_L=50pF	5	-	-	ns
	DS to SHCP hold time	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	5	-	-	ns
			V_{CC}=4.5V; C_L=50pF	5	-	-	ns
			V_{CC}=6.0V; C_L=50pF	5	-	-	ns
	$\overline{PL}$ to SHCP hold time	See Figure 8-8	V_{CC}=2.0V; C_L=50pF	5	-	-	ns
			V_{CC}=4.5V; C_L=50pF	5	-	-	ns
			V_{CC}=6.0V; C_L=15pF	5	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-6	V_{CC}=2.0V; C_L=50pF	75	-	-	ns
			V_{CC}=4.5V; C_L=50pF	15	-	-	ns
			V_{CC}=6.0V; C_L=50pF	13	-	-	ns
f_{max}	SHCP maximum frequency	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	4.8	29	-	MHz
			V_{CC}=4.5V; C_L=50pF	24	87	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	96	-	MHz
			V_{CC}=6.0V; C_L=50pF	28	104	-	MHz
CJ74HCT597							
t_{PLH}, t_{PHL}	SHCP to Q propagation delay	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	23	50	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
	$\overline{MR}$ to Q propagation delay	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	-	28	61	ns
	STCP to Q propagation delay	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	33	71	ns
			V_{CC}=5.0V; C_L=15pF	-	29	-	ns
	$\overline{PL}$ to Q propagation delay	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	-	30	65	ns
			V_{CC}=5.0V; C_L=15pF	-	26	-	ns
t_t	Transition time	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	7	19	ns
t_W	STCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	20	-	-	ns
	SHCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	20	-	-	ns
	$\overline{MR}$ LOW	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	31	-	-	ns
	$\overline{PL}$ LOW	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	25	-	-	ns
t_{su}	Dn to STCP Set_up time	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	15	-	-	ns
	DS to SHCP Set_up time	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	15	-	-	ns

	$\overline{PL}$ to SHCP Set_up time	See Figure 8-8	V_{CC}=4.5V; C_L=50pF	15	-	-	ns
t_h	Dn to SHCP hold time	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	5	-	-	ns
	DS to SHCP hold time	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	5	-	-	ns
	$\overline{PL}$ to SHCP hold time	See Figure 8-8	V_{CC}=4.5V; C_L=50pF	5	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-6	V_{CC}=4.5V; C_L=50pF	15	-	-	ns
f_{max}	Maximum frequency	See Figure 8-3	V_{CC}=4.5V; C_L=15pF	24	75	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	83	-	MHz

7.4.4 AC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC597							
t_{PLH}, t_{PHL}	SHCP to Q propagation delay	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	-	265	ns
			V_{CC}=4.5V; C_L=50pF	-	-	53	ns
			V_{CC}=6.0V; C_L=50pF	-	-	45	ns
	$\overline{MR}$ to Q propagation delay	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	-	-	265	ns
			V_{CC}=4.5V; C_L=50pF	-	-	53	ns
			V_{CC}=6.0V; C_L=50pF	-	-	45	ns
	STCP to Q propagation delay	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	-	375	ns
			V_{CC}=4.5V; C_L=50pF	-	-	75	ns
			V_{CC}=6.0V; C_L=50pF	-	-	64	ns
	$\overline{PL}$ to Q propagation delay	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	-	-	325	ns
			V_{CC}=4.5V; C_L=50pF	-	-	65	ns
			V_{CC}=6.0V; C_L=50pF	-	-	55	ns
t_t	Transition time	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	-	110	ns
			V_{CC}=4.5V; C_L=50pF	-	-	22	ns
			V_{CC}=6.0V; C_L=50pF	-	-	19	ns
t_W	STCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	120	-	-	ns
			V_{CC}=4.5V; C_L=50pF	24	-	-	ns
			V_{CC}=6.0V; C_L=50pF	20	-	-	ns
	SHCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	120	-	-	ns
			V_{CC}=4.5V; C_L=50pF	24	-	-	ns
			V_{CC}=6.0V; C_L=50pF	20	-	-	ns
	$\overline{MR}$ LOW	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	120	-	-	ns
			V_{CC}=4.5V; C_L=50pF	24	-	-	ns
			V_{CC}=6.0V; C_L=50pF	20	-	-	ns

	$\overline{PL}$ LOW	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	120	-	-	ns
			V_{CC}=4.5V; C_L=50pF	24	-	-	ns
			V_{CC}=6.0V; C_L=50pF	20	-	-	ns
t_{su}	Dn to STCP Set_up time	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	90	-	-	ns
			V_{CC}=4.5V; C_L=50pF	18	-	-	ns
			V_{CC}=6.0V; C_L=50pF	15	-	-	ns
	DS to SHCP Set_up time	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	90	-	-	ns
			V_{CC}=4.5V; C_L=50pF	18	-	-	ns
			V_{CC}=6.0V; C_L=50pF	15	-	-	ns
	$\overline{PL}$ to SHCP Set_up time	See Figure 8-8	V_{CC}=2.0V; C_L=50pF	90	-	-	ns
			V_{CC}=4.5V; C_L=50pF	18	-	-	ns
			V_{CC}=6.0V; C_L=50pF	15	-	-	ns
t_h	Dn to STCP hold time	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	5	-	-	ns
			V_{CC}=4.5V; C_L=50pF	5	-	-	ns
			V_{CC}=6.0V; C_L=50pF	5	-	-	ns
	DS to SHCP hold time	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	5	-	-	ns
			V_{CC}=4.5V; C_L=50pF	5	-	-	ns
			V_{CC}=6.0V; C_L=50pF	5	-	-	ns
	$\overline{PL}$ to SHCP hold time	See Figure 8-8	V_{CC}=2.0V; C_L=50pF	5	-	-	ns
			V_{CC}=4.5V; C_L=50pF	5	-	-	ns
			V_{CC}=6.0V; C_L=15pF	5	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-6	V_{CC}=2.0V; C_L=50pF	90	-	-	ns
			V_{CC}=4.5V; C_L=50pF	18	-	-	ns
			V_{CC}=6.0V; C_L=50pF	15	-	-	ns
f_{max}	SHCP maximum frequency	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	4.8	-	-	MHz
			V_{CC}=4.5V; C_L=50pF	24	-	-	MHz
			V_{CC}=6.0V; C_L=50pF	28	-	-	MHz
CJ74HCT597							
t_{PLH}, t_{PHL}	SHCP to Q propagation delay	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	-	60	ns
	$\overline{MR}$ to Q propagation delay	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	-	-	74	ns
	STCP to Q propagation delay	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	-	86	ns
	$\overline{PL}$ to Q propagation delay	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	-	-	78	ns
t_t	Transition time	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	-	22	ns
t_W	STCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	24	-	-	ns
	SHCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	24	-	-	ns
	$\overline{MR}$ LOW	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	38	-	-	ns

	$\overline{PL}$ LOW	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	30	-	-	ns
t_{su}	Dn to STCP Set_up time	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	18	-	-	ns
	DS to SHCP Set_up time	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	18	-	-	ns
	$\overline{PL}$ to SHCP Set_up time	See Figure 8-8	V_{CC}=4.5V; C_L=50pF	18	-	-	ns
t_h	Dn to SHCP hold time	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	5	-	-	ns
	DS to SHCP hold time	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	5	-	-	ns
	$\overline{PL}$ to SHCP hold time	See Figure 8-8	V_{CC}=4.5V; C_L=50pF	5	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-6	V_{CC}=4.5V; C_L=50pF	18	-	-	ns
f_{max}	Maximum frequency	See Figure 8-3	V_{CC}=4.5V; C_L=15pF	20	-	-	MHz

8 Detailed Description

8.1 Overview

The CJ74HC597/74HCT597 is an 8-bit shift register with input flip-flops.

8.2 Functional Block Diagram

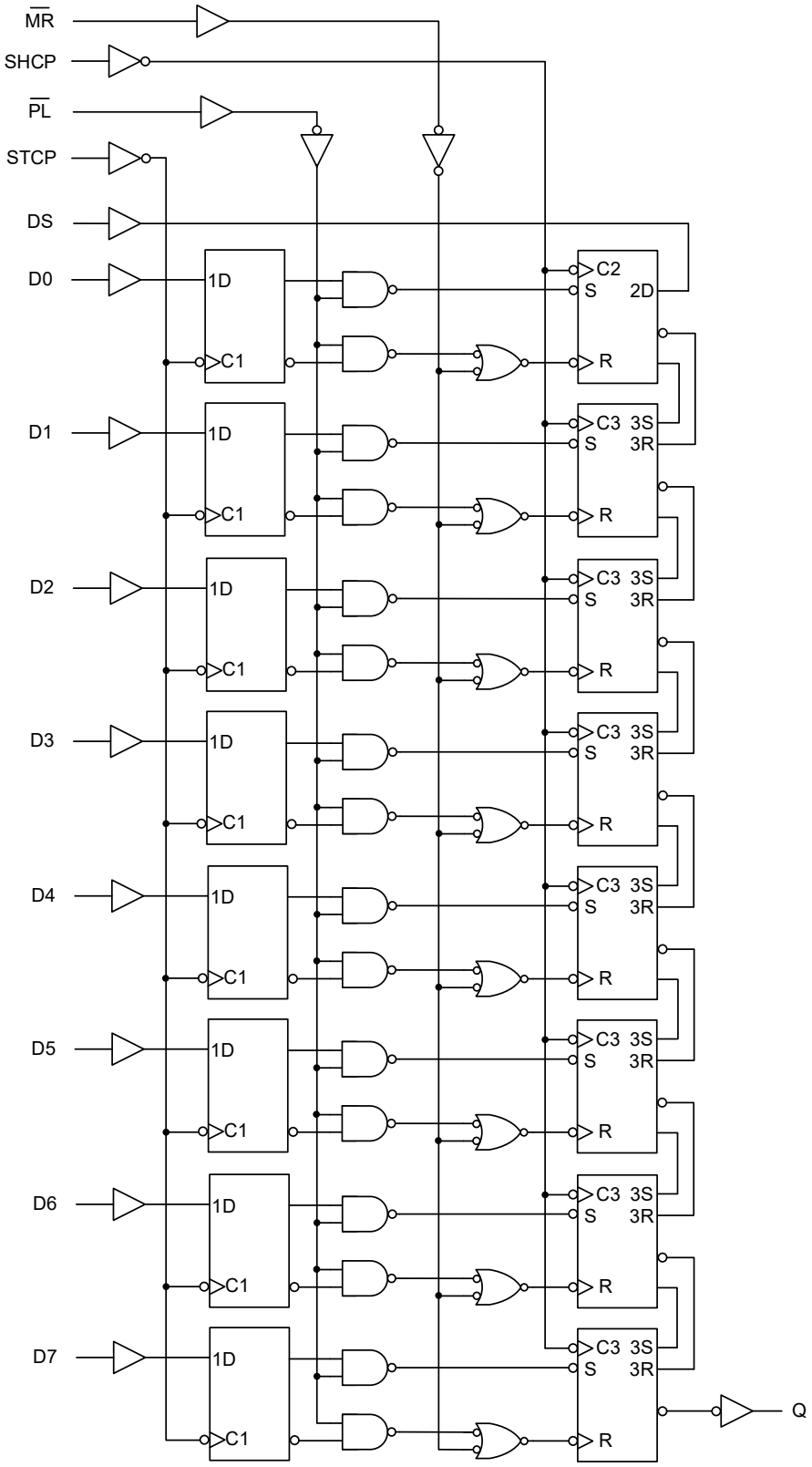


Figure 8-1 Logic symbol

8.3 Function Table(1)

INPUT				FUNCTION
STCP	SHCP	$\overline{PL}$	$\overline{MR}$	
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input flip-flops to shift register
X	X	L	L	Invalid logic, state of shift register is indeterminate When signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked Qn=Qn-1, Q0=DS

(1) H=HIGH voltage level; L=LOW voltage level; ↑=LOW-to-HIGH transition; X=don't care.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

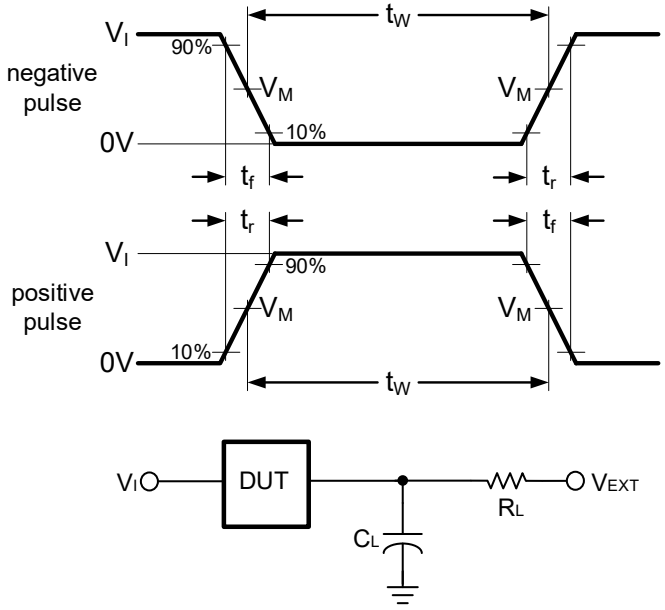


Figure 8-2 Test circuit for measuring switching times

Definitions for test circuit:

C_L includes probe and jig capacitance.

8.4.2 AC Testing Waveforms

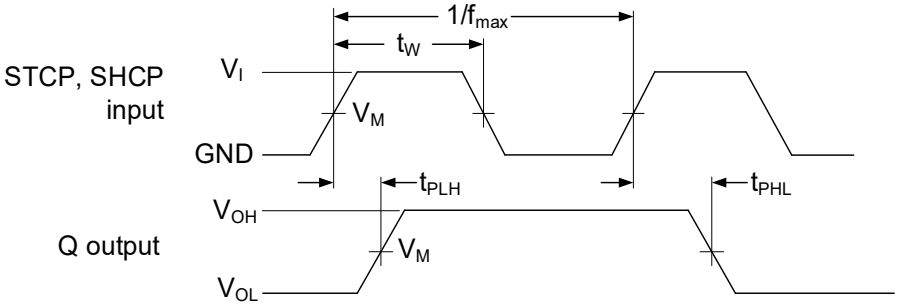


Figure 8-3 Shift clock and storage clock inputs to output, propagation delays, pulse widths and maximum clock frequency

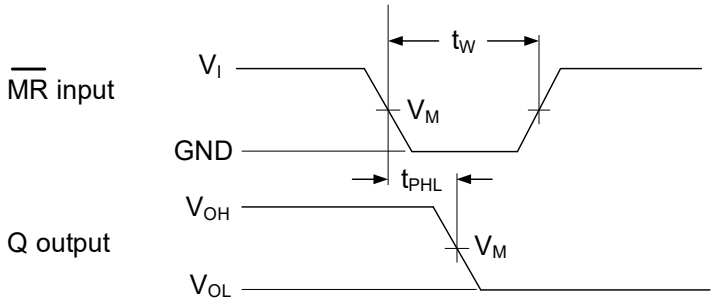


Figure 8-4 Input ($\overline{MR}$) to (Q), output propagation delays and ($\overline{MR}$) pulse width

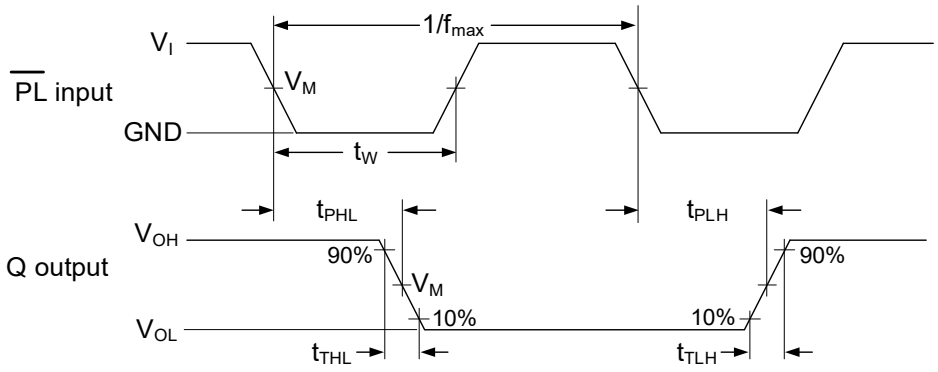


Figure 8-5 Input ($\overline{PL}$) to (Q), output propagation delays, $\overline{PL}$ pulse width and output transition times

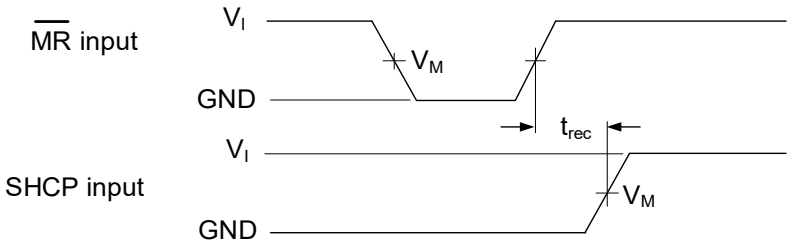


Figure 8-6 Input ($\overline{MR}$) to shift clock (SHCP) and storage clock (STCP) recovery times

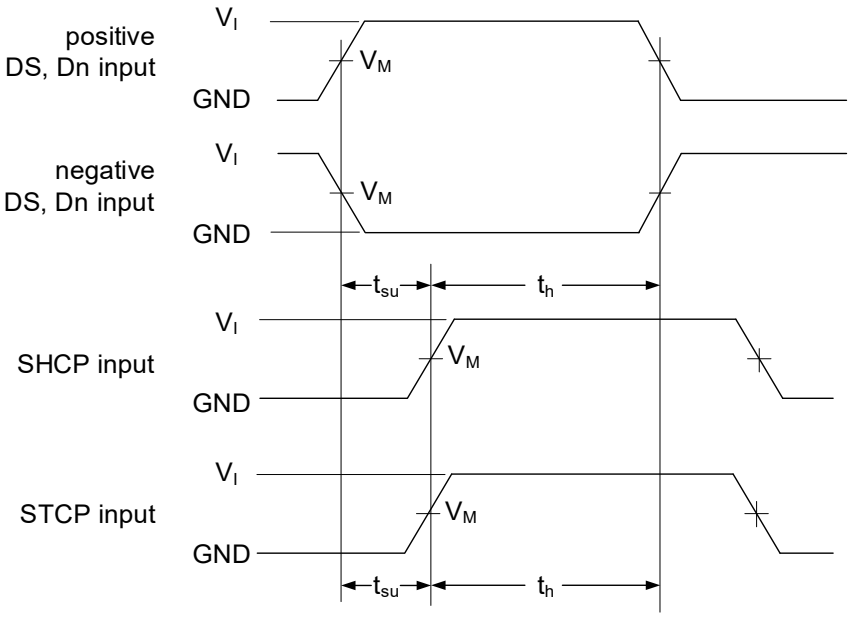


Figure 8-7 Hold and set-up times for (DS), (Dn) inputs to (SHCP), (STCP) inputs

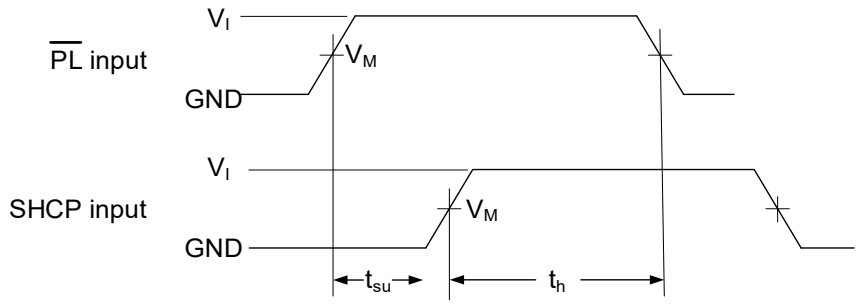


Figure 8-8 Set-up times for ($\overline{PL}$) input to (SHCP) input

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT		
	V_M	V_M	V_X	V_Y
CJ74HC597	0.5xV_{CC}	0.5xV_{CC}	0.1xV_{CC}	0.9xV_{CC}
CJ74HCT597	1.3V	1.3V	0.1xV_{CC}	0.9xV_{CC}

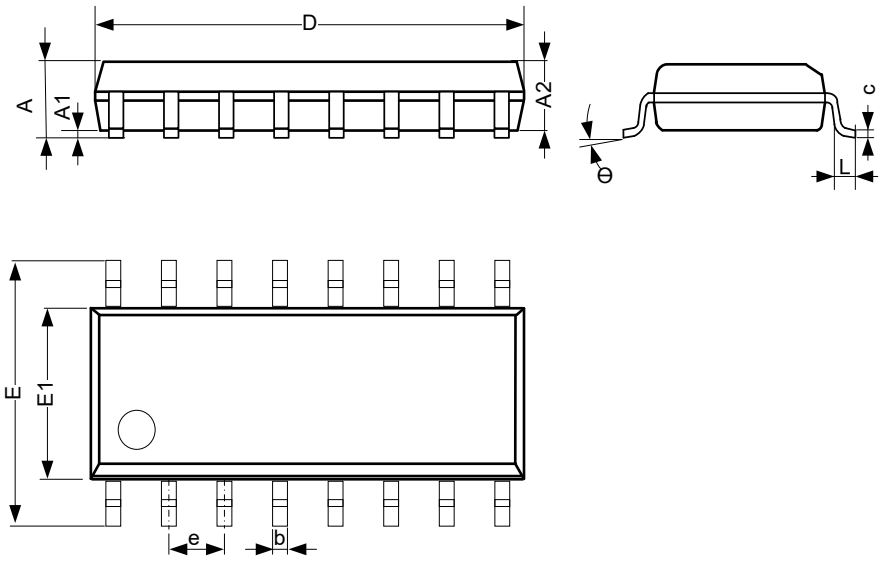
8.4.4 Test Data

TYPE	INPUT		LOAD		V_{EXT}		
	V_I	t_r=t_f	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
CJ74HC597	V_{CC}	3.0ns	15pF, 50pF	1kΩ	Open	V_{CC}	GND
CJ74HCT597	3.0V	3.0ns	15pF, 50pF	1kΩ	Open	V_{CC}	GND

9 Mechanical Information

9.1 SOP16 Mechanical Information

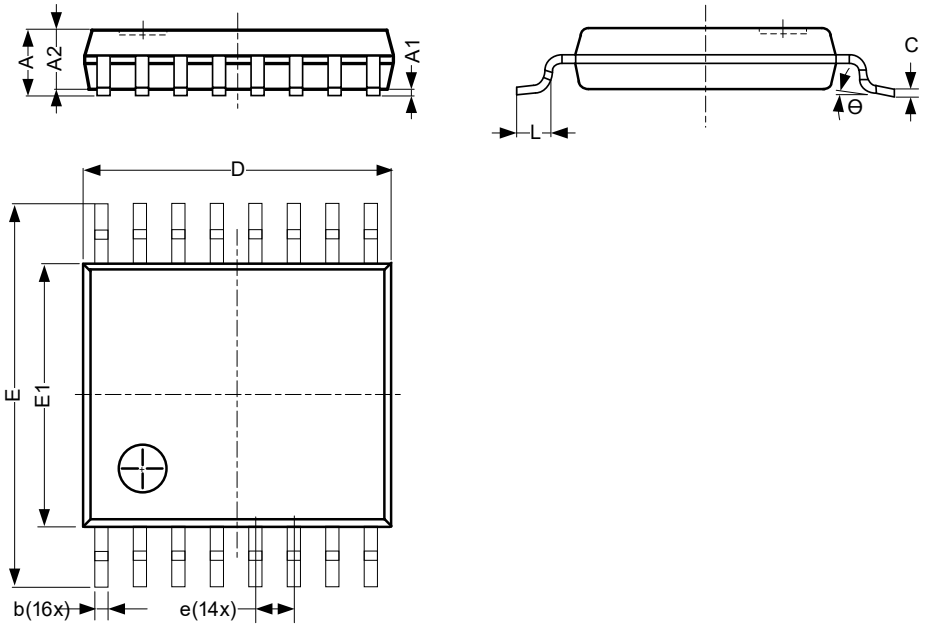
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
e	1.27 BSC		
E	5.80	-	6.30
E1	3.70	-	4.10
L	0.35	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

July, 2025: rev - 1.1, Correct unit from Ns to ns.

August, 2025: rev - 1.2, Correct 6.2 pin function.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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