Dual D-type Flip-flop with Set and Reset; Positive-edge Trigger

CJ74HC/HCT74 Logic

1 Introduction

The CJ74HC/HCT74 are dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set (n/SD) and reset (n/RD) inputs, and complementary nQ and n/Q outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Schmitt-trigger action in the clock input, makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC74	SOP14
	TSSOP14
CJ74HCT74	SOP14
	TSSOP14

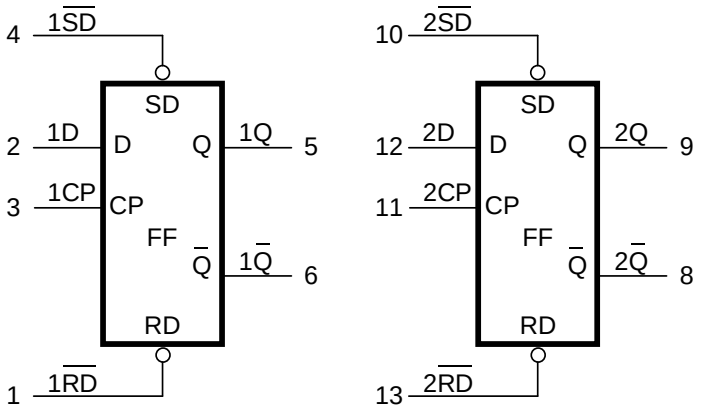
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
  - For CJ74HC74: CMOS level
  - For CJ74HCT74: TTL level
- Symmetrical output impedance
- Low power dissipation
- Balanced propagation delays
- Specified from -40°C to +125°C

4 Applications

- Convert a momentary switch to a toggle switch
- Divide a clock signal by 2 or 4



Functional diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC74ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT74ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC74BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74HCT74BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

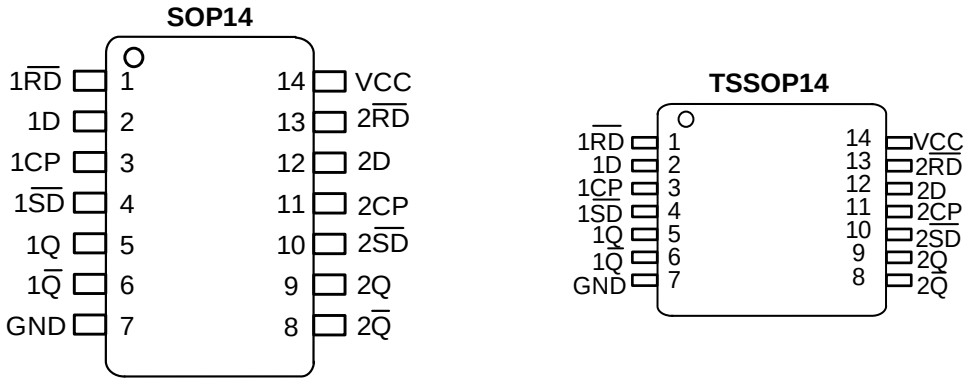


Figure 6-1 Pin configuration

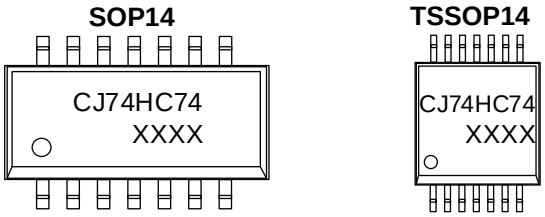
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	1$\overline{RD}$	I	Asynchronous reset-direct input (active LOW)
2	1D	I	Data input
3	1CP	I	Clock input (LOW-to-HIGH, edge-triggered)
4	1$\overline{SD}$	I	Asynchronous set-direct input (active LOW)
5	1Q	O	Output
6	1$\overline{Q}$	O	Complement output
7	GND	G	Ground (0V)
8	2$\overline{Q}$	O	Complement output
9	2Q	O	Output
10	2$\overline{SD}$	I	Asynchronous set-direct input (active LOW)
11	2CP	I	Clock input (LOW-to-HIGH, edge-triggered)
12	2D	I	Data input
13	2$\overline{RD}$	I	Asynchronous reset-direct input (active LOW)
14	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground.

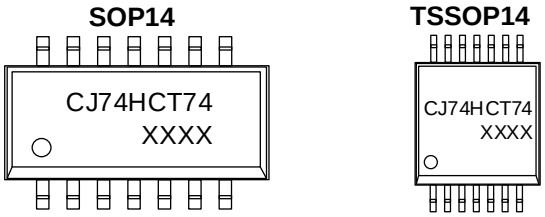
6.3 Marking Information

6.3.1 CJ74HC74



XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT74



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7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND(ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7	V
I_{IK}	Input clamping current	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
I_{OK}	Output clamping current	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
I_O	Output current	$-0.5V < V_O < V_{CC}+0.5V$		-	±25	mA
I_{CC}	Supply current	-		-	100	mA
I_{GND}	Ground current	-		-100	-	mA
P_{tot}	Total power dissipation	-		-	500	mW
T_{stg}	Storage temperature	-		-65	+150	°C
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC74						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT74						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC74							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	40	uA
C_I	Input capacitance	-		-	3.5	-	pF
CJ74HCT74							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=5.2mA; V_{CC}=4.5V	-	0.15	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	40	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; I_O=0A; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	Per input pin; nD, nRD inputs	-	-	315	uA
			Per input pin; nSD, nCP input	-	-	360	uA
C_I	Input capacitance	-		-	3.5	-	pF

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC74							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
CJ74HCT74							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=5.2mA; V_{CC}=4.5V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; I_O=0A; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	Per input pin; nD, nRD inputs	-	-	343	uA
			Per input pin; nSD, nCP input	-	-	392	uA

7.4.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC74							
t_{pd}	nCP to nQ,n$\overline{Q}$ propagation delay	See Figure 8-6(1)	V_{CC}=2.0V	-	47	220	ns
			V_{CC}=4.5V	-	17	44	ns
			V_{CC}=5.0V; C_L=15pF	-	14	-	ns
			V_{CC}=6.0V	-	14	37	ns
t_{pd}	n$\overline{SD}$ to nQ,n$\overline{Q}$ propagation delay	See Figure 8-7(1)	V_{CC}=2.0V	-	50	250	ns
			V_{CC}=4.5V	-	18	50	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	43	ns
t_{pd}	n$\overline{RD}$ to nQ,n$\overline{Q}$ propagation delay	See Figure 8-7(1)	V_{CC}=2.0V	-	52	250	ns
			V_{CC}=4.5V	-	19	50	ns
			V_{CC}=5.0V; C_L=15pF	-	16	-	ns
			V_{CC}=6.0V	-	15	43	ns
t_t	nQ,n$\overline{Q}$ transition time	See Figure 8-6(2)	V_{CC}=2.0V	-	19	95	ns
			V_{CC}=4.5V	-	7	19	ns
			V_{CC}=6.0V	-	6	16	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
t_W	n$\overline{SD}$, n$\overline{RD}$ pulse width	See Figure 8-7	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
t_{rec}	n$\overline{SD}$, n$\overline{RD}$ recovery time	See Figure 8-7	V_{CC}=2.0V	40	-	-	ns
			V_{CC}=4.5V	8	-	-	ns
			V_{CC}=6.0V	7	-	-	ns
t_{su}	nD to nCP set-up time	See Figure 8-6	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
t_h	nD to nCP hold time	See Figure 8-6	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
f_{max}	nCP maximum frequency	See Figure 8-6	V_{CC}=2.0V	4.8	23	-	MHz
			V_{CC}=4.5V	24	69	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	76	-	MHz
			V_{CC}=6.0V	28	82	-	MHz

C_{PD}	Power dissipation capacitance	C_L=50pF; f=1 MHz; V_I= GND to V_{CC}(3)		-	24	-	pF
CJ74HCT74							
t_{pd}	nCP to nQ,n$\overline{Q}$ propagation delay	See Figure 8-6(1)	V_{CC}=4.5V	-	18	44	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
t_{pd}	n$\overline{SD}$ to nQ,n$\overline{Q}$ propagation delay	See Figure 8-7(1)	V_{CC}=4.5V	-	23	50	ns
			V_{CC}=5.0V; C_L=15pF	-	18	-	ns
t_{pd}	n$\overline{RD}$ to nQ,n$\overline{Q}$ propagation delay	See Figure 8-7(1)	V_{CC}=4.5V	-	24	50	ns
			V_{CC}=5.0V; C_L=15pF	-	18	-	ns
t_t	nQ,n$\overline{Q}$ transition time	See Figure 8-6(2)	V_{CC}=4.5V	-	7	19	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=4.5V	23	-	-	ns
t_W	n$\overline{SD}$, n$\overline{RD}$ pulse width	See Figure 8-7	V_{CC}=4.5V	20	-	-	ns
t_{rec}	n$\overline{SD}$, n$\overline{RD}$ recovery time	See Figure 8-7	V_{CC}=4.5V	8	-	-	ns
t_{su}	nD to nCP set-up time	See Figure 8-6	V_{CC}=4.5V	15	-	-	ns
t_h	nD to nCP hold time	See Figure 8-6	V_{CC}=4.5V	3	-	-	ns
f_{max}	CP maximum frequency	See Figure 8-6	V_{CC}=4.5V	22	54	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	59	-	MHz
C_{PD}	Power dissipation capacitance	C_L=50pF; f=1 MHz; V_I= GND to V_{CC}-1.5V(3)		-	29	-	pF

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_t is the same as t_{THL} and t_{TLH}.

(3) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}xV_{CC}^2xf_ixN)+\sum(C_LxV_{CC}^2xf_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_LxV_{CC}^2xf_o)$=sum of outputs.

7.4.4 AC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC74							
t_{pd}	nCP to nQ,n$\overline{Q}$ propagation delay	See Figure 8-6(1)	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
t_{pd}	n$\overline{SD}$ to nQ,n$\overline{Q}$ propagation delay	See Figure 8-7(1)	V_{CC}=2.0V	-	-	300	ns
			V_{CC}=4.5V	-	-	60	ns
			V_{CC}=6.0V	-	-	51	ns
t_{pd}	n$\overline{RD}$ to nQ,n$\overline{Q}$ propagation delay	See Figure 8-7(1)	V_{CC}=2.0V	-	-	300	ns
			V_{CC}=4.5V	-	-	60	ns

			V_{CC}=6.0V	-	-	51	ns
t_t	nQ,n$\overline{Q}$ transition time	See Figure 8-6(2)	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
t_W	n$\overline{SD}$, n$\overline{RD}$ pulse width	See Figure 8-7	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
t_{rec}	n$\overline{SD}$, n$\overline{RD}$ recovery time	See Figure 8-7	V_{CC}=2.0V	45	-	-	ns
			V_{CC}=4.5V	9	-	-	ns
			V_{CC}=6.0V	8	-	-	ns
t_{su}	nD to nCP set-up time	See Figure 8-6	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
t_h	nD to nCP hold time	See Figure 8-6	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
f_{max}	nCP maximum frequency	See Figure 8-6	V_{CC}=2.0V	4.0	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
CJ74HCT74							
t_{pd}	nCP to nQ,n$\overline{Q}$ propagation delay	See Figure 8-6(1)	V_{CC}=4.5V	-	-	53	ns
t_{pd}	n$\overline{SD}$ to nQ,n$\overline{Q}$ propagation delay	See Figure 8-7(1)	V_{CC}=4.5V	-	-	60	ns
t_{pd}	n$\overline{RD}$ to nQ,n$\overline{Q}$ propagation delay	See Figure 8-7(1)	V_{CC}=4.5V	-	-	60	ns
t_t	nQ,n$\overline{Q}$ transition time	See Figure 8-6(2)	V_{CC}=4.5V	-	-	22	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=4.5V	27	-	-	ns
t_W	n$\overline{SD}$, n$\overline{RD}$ pulse width	See Figure 8-7	V_{CC}=4.5V	24	-	-	ns
t_{rec}	n$\overline{SD}$, n$\overline{RD}$ recovery time	See Figure 8-7	V_{CC}=4.5V	9	-	-	ns
t_{su}	nD to nCP set-up time	See Figure 8-6	V_{CC}=4.5V	18	-	-	ns
t_h	nD to nCP hold time	See Figure 8-6	V_{CC}=4.5V	3	-	-	ns
f_{max}	CP maximum frequency	See Figure 8-6	V_{CC}=4.5V	18	-	-	MHz

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_t is the same as t_{THL} and t_{TLH}.

8 Detailed Description

8.1 Overview

The CJ74HC/HCT74 are dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set (n/SD) and reset (n/RD) inputs, and complementary nQ and n/Q outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Schmitt-trigger action in the clock input, makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

8.2 Functional Block Diagram

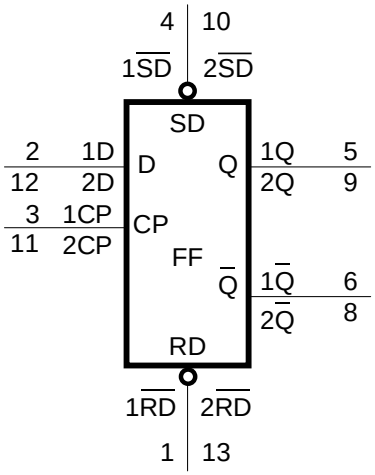


Figure 8-1 Logic symbol

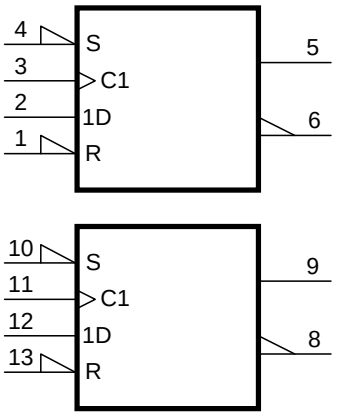


Figure 8-2 IEC logic symbol

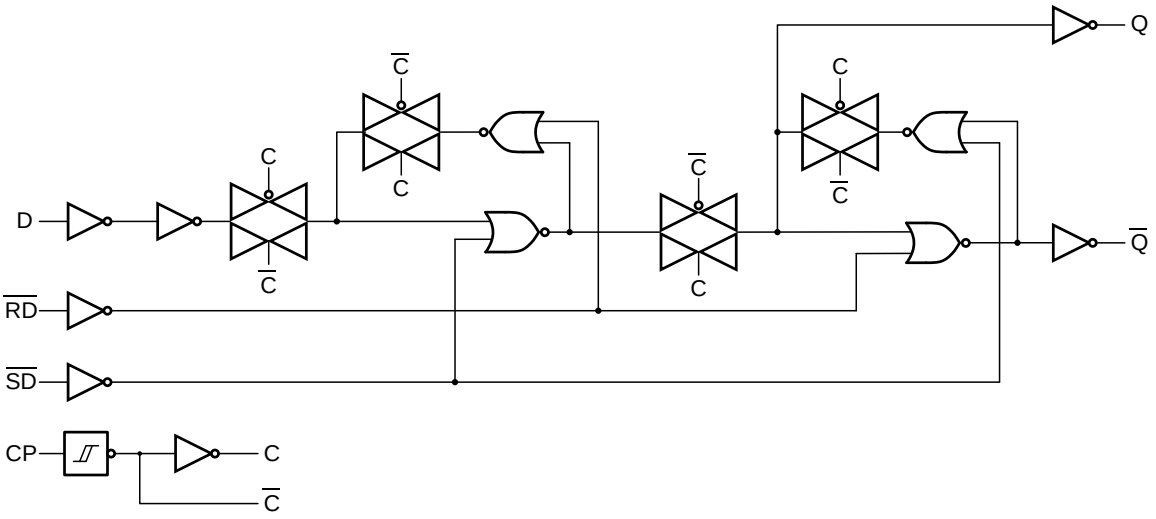


Figure 8-3 Logic diagram for one flip-flop

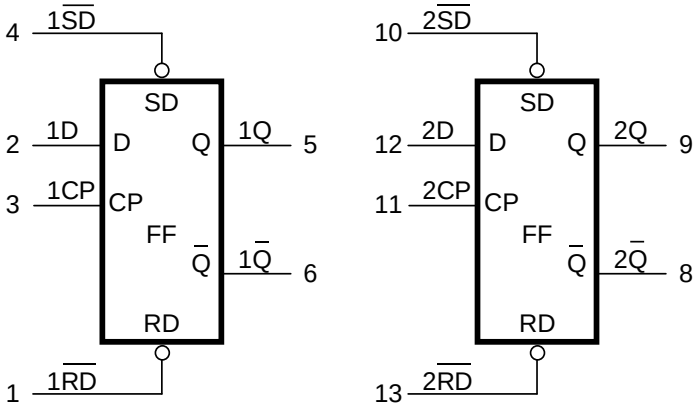


Figure 8-4 Functional diagram

8.3 Function Table(1)

INPUT				OUTPUT	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUT				OUTPUT	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ_{n+1}	$n\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH transition; Qn+1=state after the next LOW-to-HIGH CP transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

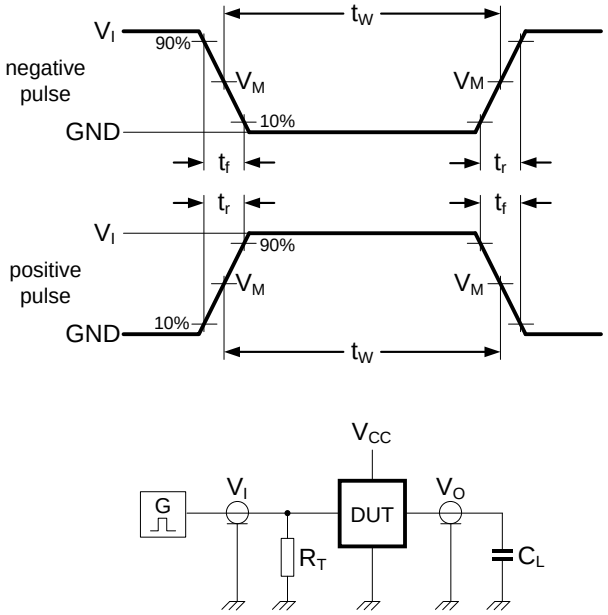


Figure 8-5 Test circuit for measuring switching times

Definitions for test circuit:

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

8.4.2 AC Testing Waveforms

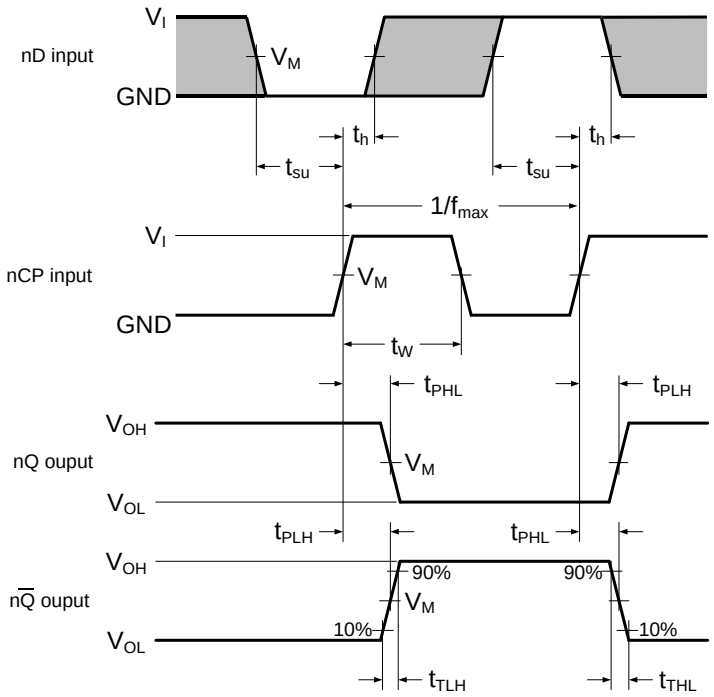


Figure 8-6 Input to output propagation delays

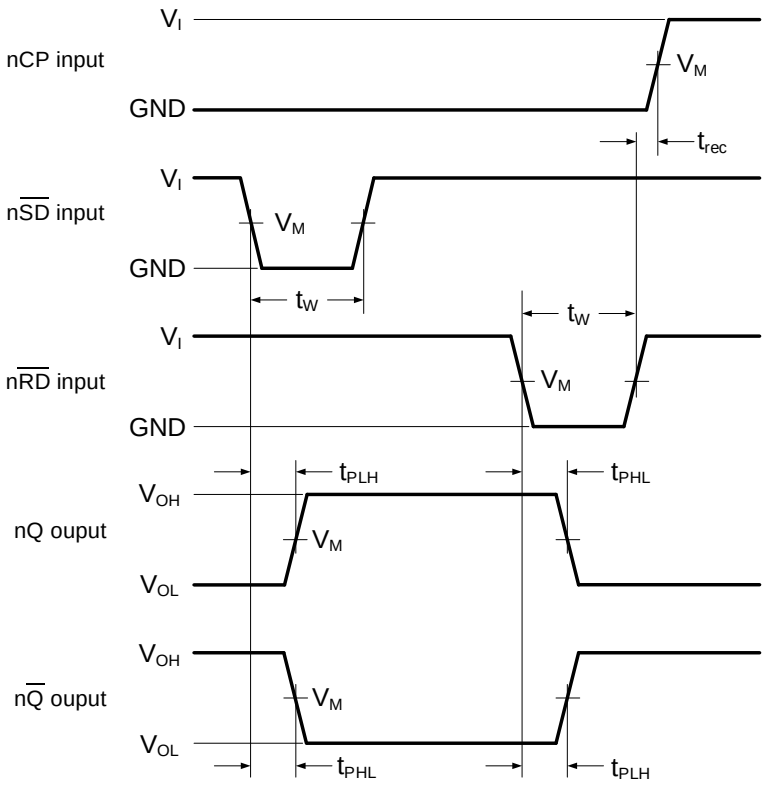


Figure 8-7 Set and reset propogation delays, pulse widths and recovery time

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT
	V_M	V_M
CJ74HC74	0.5xV_{CC}	0.5xV_{CC}
CJ74HCT74	1.3V	1.3V

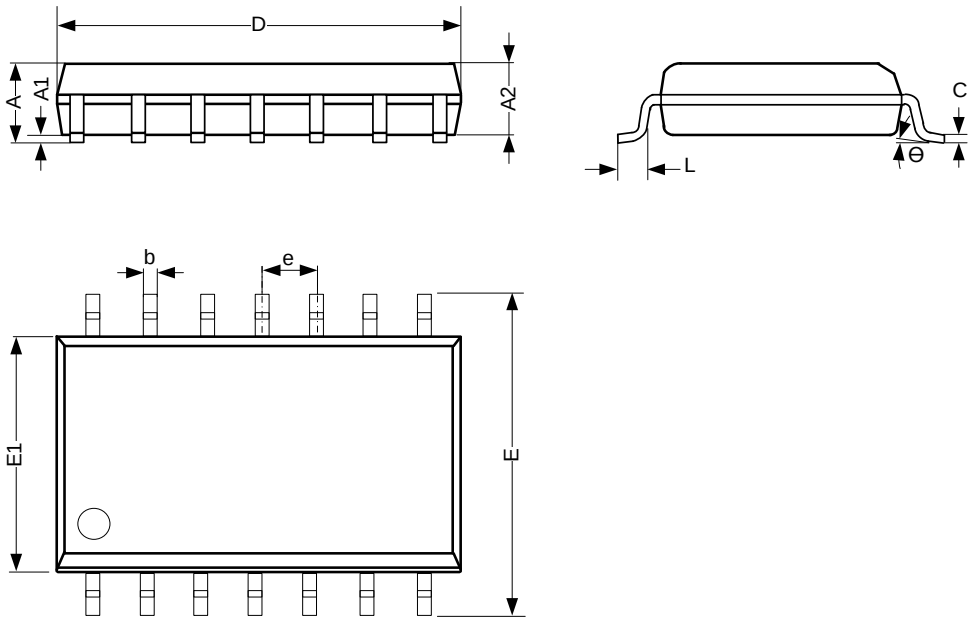
8.4.4 Test Data

TYPE	INPUT		LOAD		TEST
	V_I	t_r , t_f	C_L	R_L	
CJ74HC74	V_{CC}	6.0ns	15pF, 50pF	1kΩ	t_{PLH}, t_{PHL}
CJ74HCT74	3V	6.0ns	15pF, 50pF	1kΩ	t_{PLH}, t_{PHL}

9 Mechanical Information

9.1 SOP14 Mechanical Information

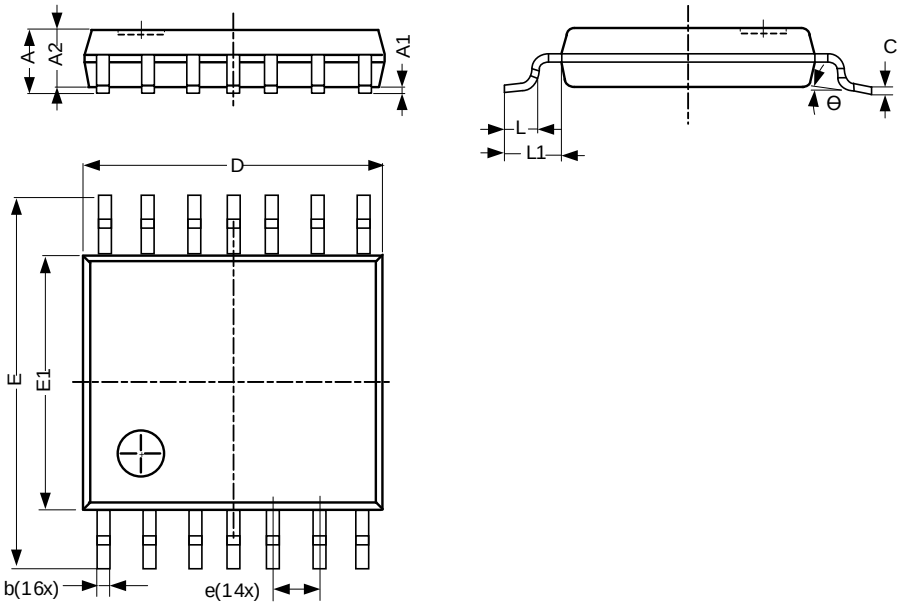
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

August, 2025: rev - 1.1, Change marking information.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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