



Hex Inverter

CJ74HC/HCT04 Logic

1 Introduction

The CJ74HC/HCT04 is a hex inverter. The inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC04	SOP14
	TSSOP14
CJ74HCT04	SOP14
	TSSOP14

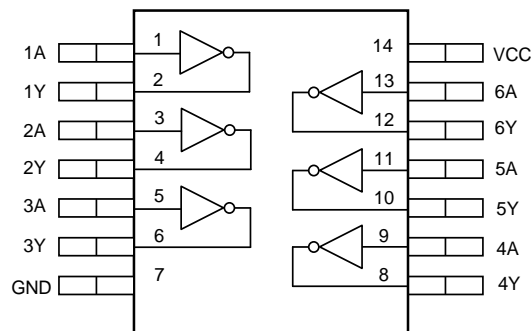
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
 - For CJ74HC04: CMOS level
 - For CJ74HCT04: TTL level
- Specified from -40°C to +125°C

4 Applications

- Synchronize inverted clock inputs
- Debounce a switch
- Invert a digital signal



Functional pinout

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC04ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CJ74HCT04ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CJ74HC04BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active
CJ74HCT04BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

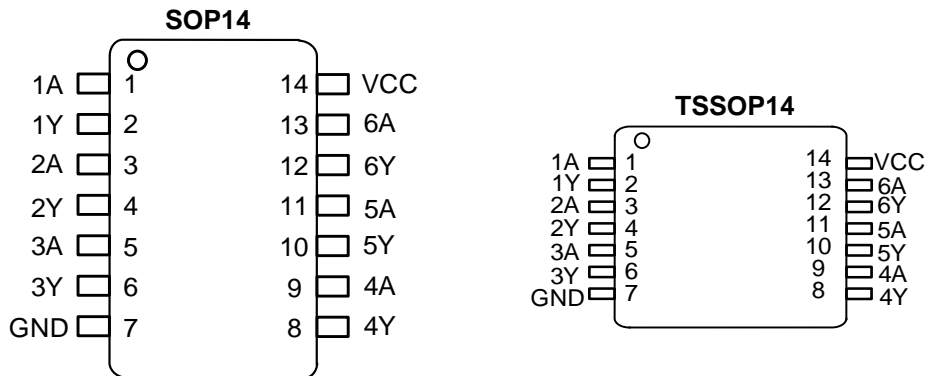


Figure 6-1 Pin configuration

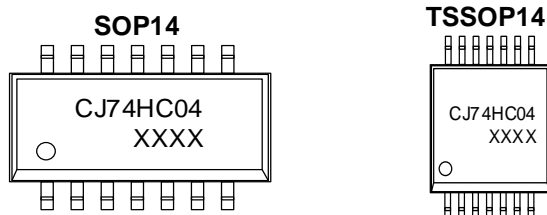
6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	1A	I	Data input
2	1Y	O	Data output
3	2A	I	Data input
4	2Y	O	Data output
5	3A	I	Data input
6	3Y	O	Data output
7	GND	G	Ground (0V)
8	4Y	O	Data output
9	4A	I	Data input
10	5Y	O	Data output
11	5A	I	Data input
12	6Y	O	Data output
13	6A	I	Data input
14	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

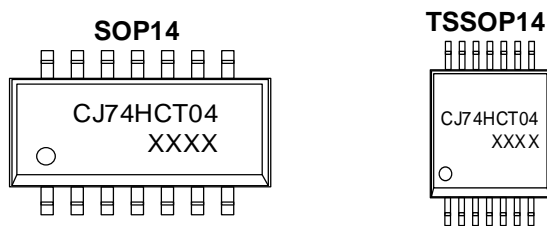
6.3 Marking Information

6.3.1 CJ74HC04



XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT04



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V _{CC}	Supply voltage	-		-0.5	+7	V
I _{IK}	Input clamping current	V _I < -0.5V or V _I > V _{CC} +0.5V		-	±20	mA
I _{OK}	Output clamping current	V _O < -0.5V or V _O > V _{CC} +0.5V		-	±20	mA
I _O	Output current	-0.5V < V _O < V _{CC} +0.5V		-	±25	mA
I _{CC}	Supply current	-		-	50	mA
I _{GND}	Ground current	-		-50	-	mA
P _{tot}	Total power dissipation	-		-	500	mW
T _{stg}	Storage temperature	-		-65	+150	°C
T _L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC04						
V _{CC}	Supply voltage	-	2.0	5.0	6.0	V
V _I	Input voltage	-	0	-	V _{CC}	V
V _O	Output voltage	-	0	-	V _{CC}	V
Δt/ΔV	Input transition rise and fall rate	V _{CC} =2.0V	-	-	625	ns/V
		V _{CC} =4.5V	-	1.67	139	ns/V
		V _{CC} =6.0V	-	-	83	ns/V
T _{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT04						
V _{CC}	Supply voltage	-	4.5	5.0	5.5	V
V _I	Input voltage	-	0	-	V _{CC}	V
V _O	Output voltage	-	0	-	V _{CC}	V
Δt/ΔV	Input transition rise and fall rate	V _{CC} =2.0V	-	-	-	ns/V
		V _{CC} =4.5V	-	1.67	139	ns/V
		V _{CC} =6.0V	-	-	-	ns/V
T _{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics
7.4.1 DC Characteristics 1

$T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC04							
V_{IH}	HIGH-level input voltage	$V_{CC}=2.0V$		1.5	-	-	V
		$V_{CC}=4.5V$		3.15	-	-	V
		$V_{CC}=6.0V$		4.2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC}=2.0V$		-	-	0.5	V
		$V_{CC}=4.5V$		-	-	1.35	V
		$V_{CC}=6.0V$		-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	2.0	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	6.0	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.98	4.32	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=2.0V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	0	0.1	V
			$I_O=4.0mA; V_{CC}=4.5V$	-	0.15	0.26	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	0.16	0.26	V
I_I	Input leakage current	$V_I=V_{CC} \text{ or } GND; V_{CC}=6.0V$		-	-	±1	uA
I_{CC}	Supply current	$V_I=V_{CC} \text{ or } GND; I_O=0A; V_{CC}=6.0V$		-	-	2.0	uA
C_I	Input capacitance	-		-	3.5	-	pF
CJ74HCT04							
V_{IH}	HIGH-level input voltage	$V_{CC}=4.5V \text{ to } 5.5V$		2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC}=4.5V \text{ to } 5.5V$		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu A; V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=5.2mA; V_{CC}=4.5V$	-	0.15	0.26	V
I_I	Input leakage current	$V_I=V_{CC} \text{ or } GND; V_{CC}=6.0V$		-	-	±1	uA
I_{CC}	Supply current	$V_I=V_{CC} \text{ or } GND; I_O=0A; V_{CC}=5.5V$		-	-	2.0	uA

ΔI_{CC}	Additional supply current	Per input pin; $V_I = V_{CC} - 2.1V$; $I_O = 0A$; Other inputs at V_{CC} or GND; $V_{CC} = 4.5V$ to $5.5V$	-	-	432	μA
C_i	Input capacitance	-	-	3.5	-	pF

7.4.2 DC Characteristics 2

$T_{amb} = -40^\circ C$ to $+85^\circ C$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
CJ74HC04							
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0V$	1.5	-	-	V	
		$V_{CC} = 4.5V$	3.15	-	-	V	
		$V_{CC} = 6.0V$	4.2	-	-	V	
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0V$	-	-	0.5	V	
		$V_{CC} = 4.5V$	-	-	1.35	V	
		$V_{CC} = 6.0V$	-	-	1.8	V	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_O = -20\mu A$; $V_{CC} = 2.0V$	1.9	-	-	V
			$I_O = -20\mu A$; $V_{CC} = 4.5V$	4.4	-	-	V
			$I_O = -20\mu A$; $V_{CC} = 6.0V$	5.9	-	-	V
			$I_O = -4.0mA$; $V_{CC} = 4.5V$	3.84	-	-	V
			$I_O = -5.2mA$; $V_{CC} = 6.0V$	5.34	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_O = 20\mu A$; $V_{CC} = 2.0V$	-	-	0.1	V
			$I_O = 20\mu A$; $V_{CC} = 4.5V$	-	-	0.1	V
			$I_O = 20\mu A$; $V_{CC} = 6.0V$	-	-	0.1	V
			$I_O = 4.0mA$; $V_{CC} = 4.5V$	-	-	0.33	V
			$I_O = 5.2mA$; $V_{CC} = 6.0V$	-	-	0.33	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0V$	-	-	± 1	μA	
I_{CC}	Supply current	$V_I = V_{CC}$ or GND; $I_O = 0A$; $V_{CC} = 6.0V$	-	-	20	μA	
CJ74HCT04							
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5V$ to $5.5V$	2.0	-	-	V	
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5V$ to $5.5V$	-	-	0.8	V	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_O = -20\mu A$; $V_{CC} = 4.5V$	4.4	-	-	V
			$I_O = -4.0mA$; $V_{CC} = 4.5V$	3.84	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_O = 20\mu A$; $V_{CC} = 4.5V$	-	-	0.1	V
			$I_O = 5.2mA$; $V_{CC} = 4.5V$	-	-	0.33	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0V$	-	-	± 1	μA	
I_{CC}	Supply current	$V_I = V_{CC}$ or GND; $I_O = 0A$; $V_{CC} = 5.5V$	-	-	20	μA	
ΔI_{CC}	Additional supply current	Per input pin; $V_I = V_{CC} - 2.1V$; $I_O = 0A$; Other inputs at V_{CC} or GND; $V_{CC} = 4.5V$ to $5.5V$	-	-	540	μA	

7.4.3 DC Characteristics 3
 $T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
CJ74HC04							
V_{IH}	HIGH-level input voltage	$V_{CC}=2.0\text{V}$	1.5	-	-	V	
		$V_{CC}=4.5\text{V}$	3.15	-	-	V	
		$V_{CC}=6.0\text{V}$	4.2	-	-	V	
V_{IL}	LOW-level input voltage	$V_{CC}=2.0\text{V}$	-	-	0.5	V	
		$V_{CC}=4.5\text{V}$	-	-	1.35	V	
		$V_{CC}=6.0\text{V}$	-	-	1.8	V	
V_{OH}	HIGH-level output voltage	$V_i = V_{IH}$ or V_{IL}	$I_o = -20\mu\text{A}; V_{CC}=2.0\text{V}$	1.9	-	-	V
			$I_o = -20\mu\text{A}; V_{CC}=4.5\text{V}$	4.4	-	-	V
			$I_o = -20\mu\text{A}; V_{CC}=6.0\text{V}$	5.9	-	-	V
			$I_o = -4.0\text{mA}; V_{CC}=4.5\text{V}$	3.7	-	-	V
			$I_o = -5.2\text{mA}; V_{CC}=6.0\text{V}$	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_i = V_{IH}$ or V_{IL}	$I_o = 20\mu\text{A}; V_{CC}=2.0\text{V}$	-	-	0.1	V
			$I_o = 20\mu\text{A}; V_{CC}=4.5\text{V}$	-	-	0.1	V
			$I_o = 20\mu\text{A}; V_{CC}=6.0\text{V}$	-	-	0.1	V
			$I_o = 4.0\text{mA}; V_{CC}=4.5\text{V}$	-	-	0.4	V
			$I_o = 5.2\text{mA}; V_{CC}=6.0\text{V}$	-	-	0.4	V
I_i	Input leakage current	$V_i = V_{CC}$ or GND; $V_{CC}=6.0\text{V}$	-	-	± 1	μA	
I_{CC}	Supply current	$V_i = V_{CC}$ or GND; $I_o = 0\text{A}; V_{CC}=6.0\text{V}$	-	-	40	μA	
CJ74HCT04							
V_{IH}	HIGH-level input voltage	$V_{CC}=4.5\text{V}$ to 5.5V	2.0	-	-	V	
V_{IL}	LOW-level input voltage	$V_{CC}=4.5\text{V}$ to 5.5V	-	-	0.8	V	
V_{OH}	HIGH-level output voltage	$V_i = V_{IH}$ or V_{IL}	$I_o = -20\mu\text{A}; V_{CC}=4.5\text{V}$	4.4	-	-	V
			$I_o = -4.0\text{mA}; V_{CC}=4.5\text{V}$	3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_i = V_{IH}$ or V_{IL}	$I_o = 20\mu\text{A}; V_{CC}=4.5\text{V}$	-	-	0.1	V
			$I_o = 5.2\text{mA}; V_{CC}=4.5\text{V}$	-	-	0.4	V
I_i	Input leakage current	$V_i = V_{CC}$ or GND; $V_{CC}=6.0\text{V}$	-	-	± 1	μA	
I_{CC}	Supply current	$V_i = V_{CC}$ or GND; $I_o = 0\text{A}; V_{CC}=5.5\text{V}$	-	-	40	μA	
ΔI_{CC}	Additional supply current	Per input pin; $V_i = V_{CC} - 2.1\text{V}; I_o = 0\text{A};$ Other inputs at V_{CC} or GND; $V_{CC}=4.5\text{V}$ to 5.5V	-	-	590	μA	

7.4.4 AC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
CJ74HC04							
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5 ⁽¹⁾	V _{CC} =2.0V	-	25	85	ns
			V _{CC} =4.5V	-	9	17	ns
			V _{CC} =5.0V; C _L =15pF	-	7	-	ns
			V _{CC} =6.0V	-	7	14	ns
t _t	Transition time	See Figure 8-5 ⁽²⁾	V _{CC} =2.0V	-	19	75	ns
			V _{CC} =4.5V	-	7	15	ns
			V _{CC} =6.0V	-	6	13	ns
C _{PD}	Power dissipation capacitance	Per package; V _I = GND to V _{CC} ⁽³⁾	-	21	-	pF	
CJ74HCT04							
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5 ⁽¹⁾	V _{CC} =4.5V	-	10	19	ns
			V _{CC} =5.0V; C _L =15pF	-	8	-	ns
t _t	Transition time	See Figure 8-5 ⁽²⁾	V _{CC} =4.5V	-	7	15	ns
C _{PD}	Power dissipation capacitance	Per package; V _I = GND to V _{CC} -1.5V ⁽³⁾	-	24	-	pF	

- (1) t_{pd} is the same as t_{PLH} and t_{PHL}.
- (2) t_t is the same as t_{THL} and t_{TLH}.
- (3) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
 $P_D = (C_{PD} \times V_{CC}^2 \times f_i \times N) + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i=input frequency in MHz;
 f_o=output frequency in MHz;
 C_L=output load capacitance in pF;
 V_{CC}=supply voltage in V;
 N=number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

7.4.5 AC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
CJ74HC04							
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5 ⁽¹⁾	V _{CC} =2.0V	-	-	105	ns
			V _{CC} =4.5V	-	-	21	ns
			V _{CC} =6.0V	-	-	18	ns
t _t	Transition time	See Figure 8-5 ⁽²⁾	V _{CC} =2.0V	-	-	95	ns
			V _{CC} =4.5V	-	-	19	ns
			V _{CC} =6.0V	-	-	16	ns
CJ74HCT04							
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5 ⁽¹⁾	V _{CC} =4.5V	-	-	24	ns
t _t	Transition time	See Figure 8-5 ⁽²⁾	V _{CC} =4.5V	-	-	19	ns

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_t is the same as t_{THL} and t_{TLH}.

7.4.6 AC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
CJ74HC04							
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5 ⁽¹⁾	V _{CC} =2.0V	-	-	130	ns
			V _{CC} =4.5V	-	-	26	ns
			V _{CC} =6.0V	-	-	22	ns
t _t	Transition time	See Figure 8-5 ⁽²⁾	V _{CC} =2.0V	-	-	110	ns
			V _{CC} =4.5V	-	-	22	ns
			V _{CC} =6.0V	-	-	19	ns
CJ74HCT04							
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5 ⁽¹⁾	V _{CC} =4.5V	-	-	29	ns
t _t	Transition time	See Figure 8-5 ⁽²⁾	V _{CC} =4.5V	-	-	22	ns

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_t is the same as t_{THL} and t_{TLH}.

8 Detailed Description

8.1 Overview

The CJ74HC/HCT04 is a hex inverter. The inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

8.2 Functional Block Diagram

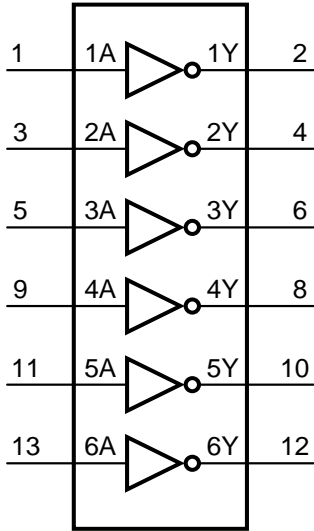


Figure 8-1 Logic symbol

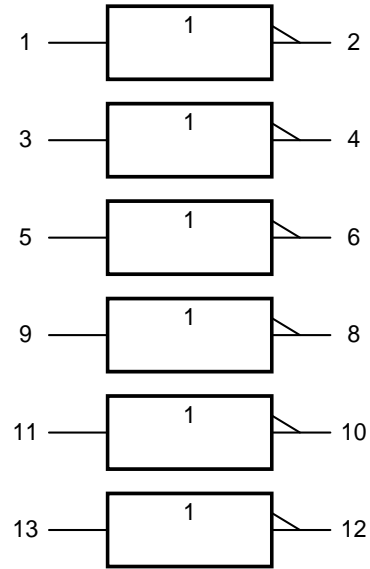


Figure 8-2 IEC logic symbol

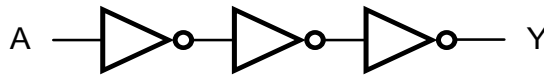


Figure 8-3 Logic diagram for one gate

8.3 Function Table⁽¹⁾

INPUT	OUTPUT
nA	nY
L	H
H	L

(1) H=HIGH voltage level; L=LOW voltage level.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

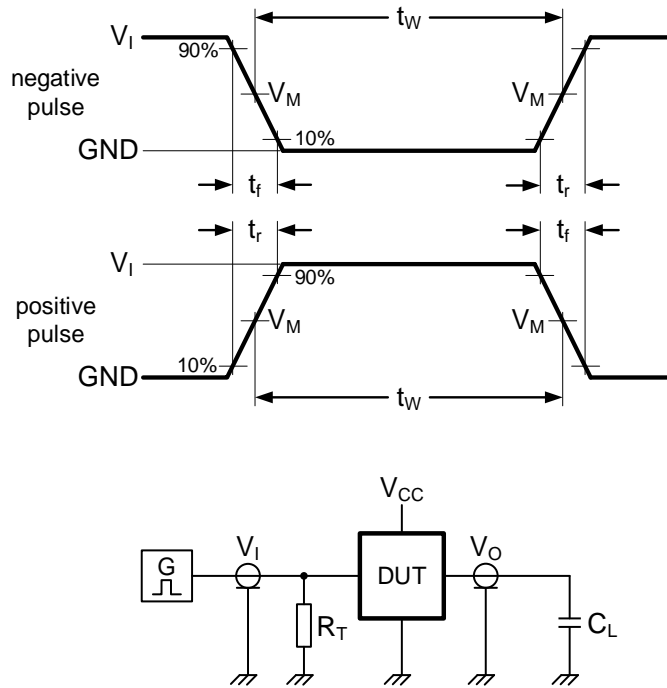


Figure 8-4 Test circuit for measuring switching times

Definitions for test circuit:

C_L =load capacitance including jig and probe capacitance.

R_T =termination resistance should be equal to the output impedance Z_o of the pulse generator.

8.4.2 AC Testing Waveforms

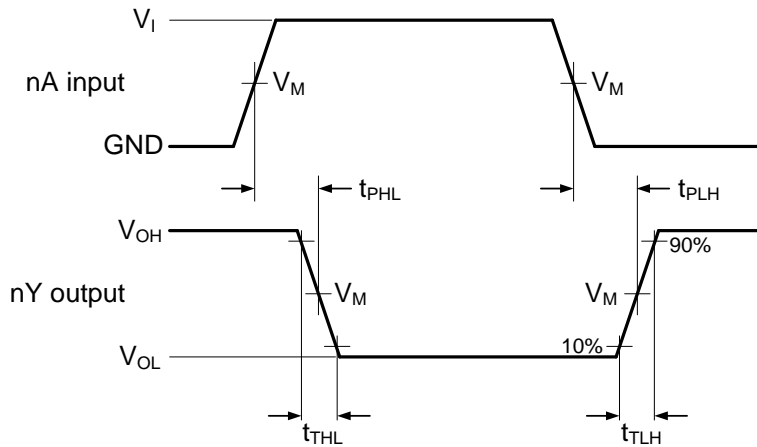


Figure 8-5 The input (nA) to output (nY) propagation delay times

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT
	V_M	V_M
CJ74HC04	0.5xV _{CC}	0.5xV _{CC}
CJ74HCT04	1.3V	1.3V

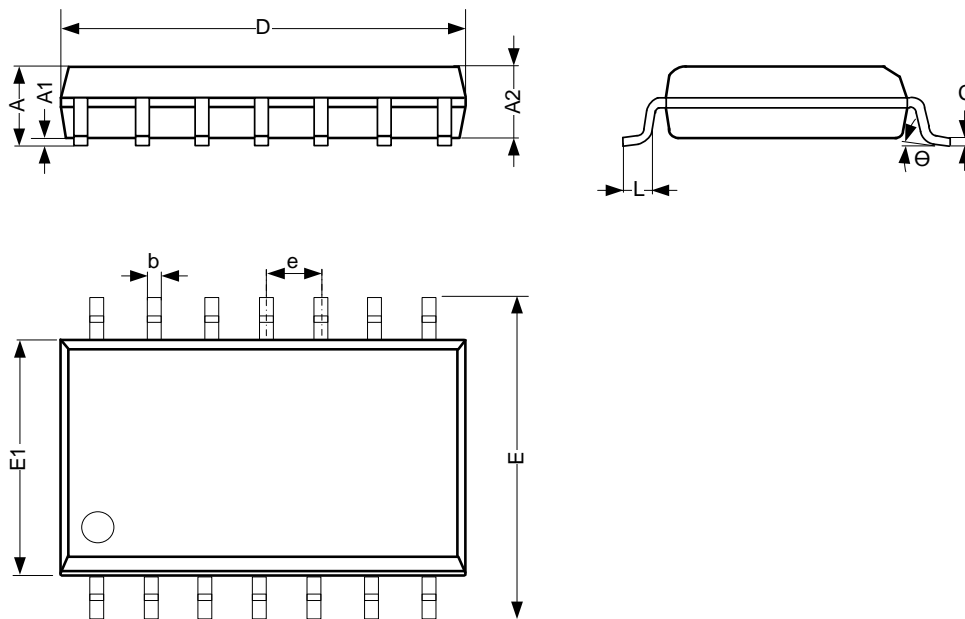
8.4.4 Test Data

TYPE	INPUT		LOAD	TEST
	V_I	t_r, t_f	C_L	
CJ74HC04	V _{CC}	6.0ns	15pF, 50pF	t_{PLH}, t_{PHL}
CJ74HCT04	3.0V	6.0ns	15pF, 50pF	t_{PLH}, t_{PHL}

9 Mechanical Information

9.1 SOP14 Mechanical Information

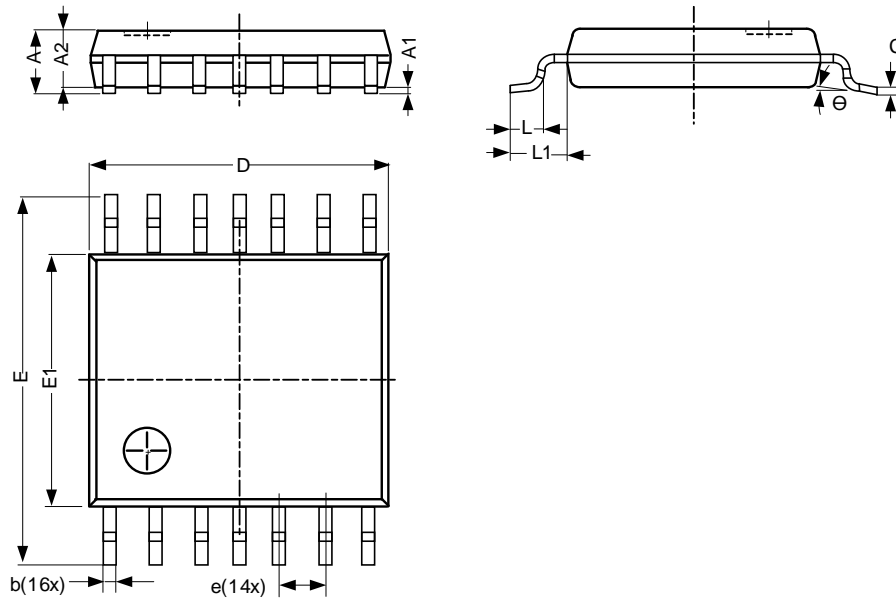
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

November, 2025: rev - 1.1, Change marking information.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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