JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

8-bit Serial-in, Serial or Parallel-out Shift Register

with Output Latches; 3-state

CJ74HC/HCT595 Logic

1 Introduction

The CJ74HC/HCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset /MR input. A LOW on /MR will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input (/OE) is LOW.

A HIGH on /OE causes the outputs to assume a high-impedance OFF-state. Operation of the /OE input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC595	SOP16
	TSSOP16
CJ74HCT595	SOP16
	TSSOP16

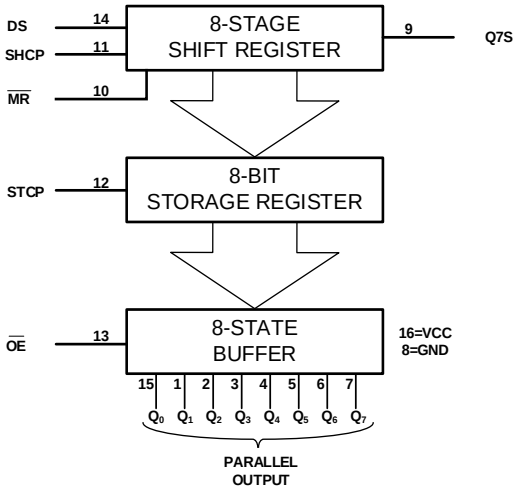
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
  - For CJ74HC595: CMOS level
  - For CJ74HCT595: TTL level
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- Specified from -40°C to +125°C

4 Applications

- Network switches
- Power infrastructure
- LED displays
- Servers



Block diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC595AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT595AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC595BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74HCT595BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

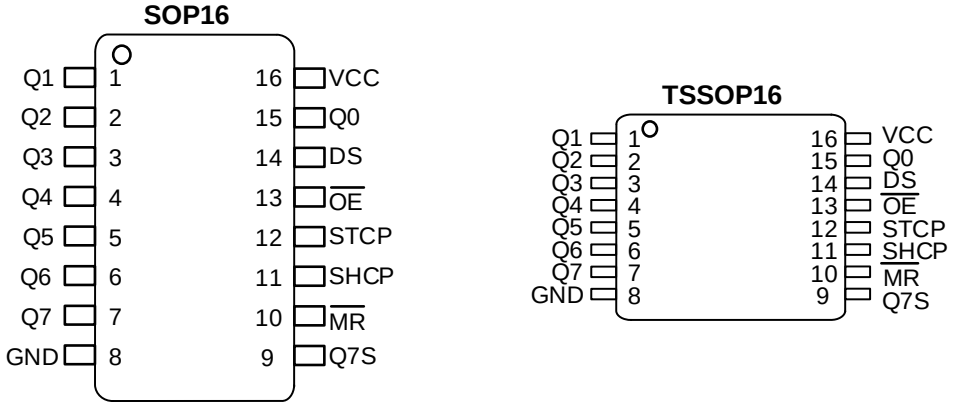


Figure 6-1 Pin configuration

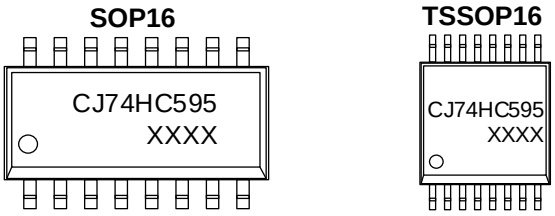
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	Q1	O	Parallel data output
2	Q2	O	Parallel data output
3	Q3	O	Parallel data output
4	Q4	O	Parallel data output
5	Q5	O	Parallel data output
6	Q6	O	Parallel data output
7	Q7	O	Parallel data output
8	GND	G	Ground (0V)
9	Q7S	O	Serial data output
10	$\overline{MR}$	I	Master reset (active LOW)
11	SHCP	I	Shift register clock input
12	STCP	I	Storage register clock input
13	$\overline{OE}$	I	Output enable input (active LOW)
14	DS	I	Serial data input
15	Q0	O	Parallel data output
16	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

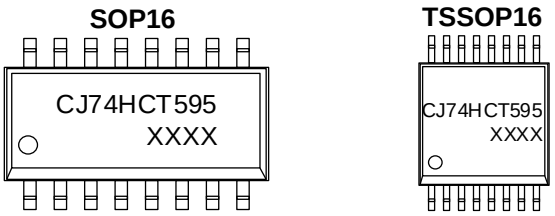
6.3 Marking Information

6.3.1 CJ74HC595



XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT595



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7.0	V
I_{IK}	Input clamping current	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
I_{OK}	Output clamping current	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
I_O	Output current	V_O= -0.5V to (V_{CC}+0.5V)	Pin Q7S	-	±25	mA
			Pins Qn	-	±35	mA
I_{CC}	Supply current	-		-	70	mA
I_{GND}	Ground current	-		-70	-	mA
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC595						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT595						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC595							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.0	V
		V_{CC}=6.0V		-	-	1.5	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	All outputs; I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			All outputs; I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			All outputs; I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			Q7S output; I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			Q7S output; I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	-	V
			Qn bus driver outputs; I_O=-6.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			Qn bus driver outputs; I_O=-7.8mA; V_{CC}=6.0V	5.34	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	All outputs; I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			All outputs; I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			All outputs; I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			Q7S output; I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			Q7S output; I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.33	V
			Qn bus driver outputs; I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			Qn bus driver outputs; I_O=7.8mA; V_{CC}=6.0V	-	0.16	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±5.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
C_I	Input capacitance	-		-	3.5	-	pF
CJ74HCT595							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	All outputs; I_O=-20uA	4.4	4.5	-	V
			Q7S output; I_O=-4.0mA	3.84	4.32	-	V
			Qn bus driver outputs; I_O=-6.0mA	3.7	4.32	-	V

V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC}=4.5V	All outputs; I_O=20uA	-	0	0.1	V
			Q7S output; I_O=4.0mA	-	0.15	0.33	V
			Qn bus driver outputs; I_O=6.0mA	-	0.16	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±5.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	Pins $\overline{MR}$, SHCP, $\overline{STCP}$, $\overline{OE}$	-	150	675	uA
			Pin DS	-	25	113	uA
C_I	Input capacitance	-		-	3.5	-	pF

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC595							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.0	V
		V_{CC}=6.0V		-	-	1.5	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}	All outputs; I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			All outputs; I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			All outputs; I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			Q7S output; I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			Q7S output; I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
			Qn bus driver outputs; I_O=-6.0mA; V_{CC}=4.5V	3.7	-	-	V
			Qn bus driver outputs; I_O=-7.8mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}	All outputs; I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			All outputs; I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			All outputs; I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			Q7S output; I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			Q7S output; I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
			Qn bus driver outputs;	-	-	0.4	V

			I_O=6.0mA; V_{CC}=4.5V				
			Qn bus driver outputs; I_O=7.8mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±10	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
CJ74HCT595							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	All outputs; I_O=-20uA	4.4	-	-	V
			Q7S output; I_O=-4.0mA	3.7	-	-	V
			Qn bus driver outputs; I_O=-6.0mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	All outputs; I_O=20uA	-	-	0.1	V
			Q7S output; I_O=4.0mA	-	-	0.4	V
			Qn bus driver outputs; I_O=6.0mA	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±10	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	Pins $\overline{MR}$, SHCP, STCP, $\overline{OE}$	-	-	735	uA
			Pin DS	-	-	123	uA

7.4.3 AC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
CJ74HC595							
t_{PLH}, t_{PHL}	Propagation delay	SHCP to Q7S; See Figure 8-6	V_{CC}=2.0V	-	75	160	ns
			V_{CC}=4.5V	-	19	32	ns
			V_{CC}=6.0V	-	15	27	ns
		STCP to Qn; See Figure 8-7	V_{CC}=2.0V	-	85	175	ns
			V_{CC}=4.5V	-	20	35	ns
			V_{CC}=6.0V	-	16	30	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; See Figure 8-9	V_{CC}=2.0V	-	47	175	ns
			V_{CC}=4.5V	-	17	35	ns
			V_{CC}=6.0V	-	14	30	ns
t_{PZH}, t_{PZL}	$\overline{OE}$ to Qn enable time	See Figure 8-10	V_{CC}=2.0V	-	47	150	ns
			V_{CC}=4.5V	-	17	30	ns

			V_{CC}=6.0V	-	14	26	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$ to Qn disable time	See Figure 8-10	V_{CC}=2.0V	-	41	150	ns
			V_{CC}=4.5V	-	15	30	ns
			V_{CC}=6.0V	-	12	27	ns
t_W	Pulse width	SHCP HIGH or LOW; See Figure 8-6	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
		STCP HIGH or LOW; See Figure 8-7	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
		$\overline{MR}$ LOW; See Figure 8-9	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
t_{su}	Set-up time	DS to SHCP; See Figure 8-8	V_{CC}=2.0V	50	-	-	ns
			V_{CC}=4.5V	10	-	-	ns
			V_{CC}=6.0V	9	-	-	ns
		SHCP to STCP; See Figure 8-7	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
t_h	DS to SHCP hold time	See Figure 8-8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-9	V_{CC}=2.0V	50	-	-	ns
			V_{CC}=4.5V	10	-	-	ns
			V_{CC}=6.0V	9	-	-	ns
f_{max}	Maximum frequency	SHCP or STCP; See Figure 8-6 and Figure 8-7	V_{CC}=2.0V	9	-	-	MHz
			V_{CC}=4.5V	30	-	-	MHz
			V_{CC}=6.0V	35	-	-	MHz
CJ74HCT595; V_{CC}=4.5V to 5.5V							
t_{PLH}, t_{PHL}	Propagation delay	SHCP to Q7S; See Figure 8-6		-	25	42	ns
		STCP to Qn; See Figure 8-7		-	24	40	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; See Figure 8-9		-	23	40	ns
t_{PZH}, t_{PZL}	$\overline{OE}$ to Qn enable time	See Figure 8-10		-	21	35	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$ to Qn disable time	See Figure 8-10		-	18	30	ns
t_W	Pulse width	SHCP HIGH or LOW; See Figure 8-6		16	-	-	ns
		STCP HIGH or LOW; See Figure 8-7		16	-	-	ns
		$\overline{MR}$ LOW; See Figure 8-9		20	-	-	ns

t_{su}	Set-up time	DS to SHCP; See Figure 8-8	16	-	-	ns
		SHCP to STCP; See Figure 8-7	16	-	-	ns
t_h	DS to SHCP hold time	See Figure 8-8	3	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-9	10	-	-	ns
f_{max}	Maximum frequency	SHCP or STCP; See Figure 8-6 and Figure 8-7	30	-	-	MHz

(1) Typical values are measured at nominal supply voltage.

7.4.4 AC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC595							
t_{PLH}, t_{PHL}	Propagation delay	SHCP to Q7S; See Figure 8-6	V_{CC}=2.0V	-	-	200	ns
			V_{CC}=4.5V	-	-	40	ns
			V_{CC}=6.0V	-	-	34	ns
		STCP to Qn; See Figure 8-7	V_{CC}=2.0V	-	-	220	ns
			V_{CC}=4.5V	-	-	44	ns
			V_{CC}=6.0V	-	-	37	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; See Figure 8-9	V_{CC}=2.0V	-	-	220	ns
			V_{CC}=4.5V	-	-	44	ns
			V_{CC}=6.0V	-	-	37	ns
t_{PZH}, t_{PZL}	$\overline{OE}$ to Qn enable time	See Figure 8-10	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$ to Qn disable time	See Figure 8-10	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
t_W	Pulse width	SHCP HIGH or LOW; See Figure 8-6	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
		STCP HIGH or LOW; See Figure 8-7	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
		$\overline{MR}$ LOW; See Figure 8-9	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
t_{su}	Set-up time	DS to SHCP; See Figure 8-8	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns

			V_{CC}=6.0V	11	-	-	ns
		SHCP to STCP; See Figure 8-7	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
t_h	DS to SHCP hold time	See Figure 8-8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-9	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
f_{max}	Maximum frequency	SHCP or STCP; See Figure 8-6 and Figure 8-7	V_{CC}=2.0V	4.8	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
CJ74HCT595; V_{CC}=4.5V to 5.5V							
t_{PLH}, t_{PHL}	Propagation delay	SHCP to Q7S; See Figure 8-6		-	-	53	ns
		STCP to Qn; See Figure 8-7		-	-	50	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; See Figure 8-9		-	-	50	ns
t_{PZH}, t_{PZL}	$\overline{OE}$ to Qn enable time	See Figure 8-10		-	-	44	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$ to Qn disable time	See Figure 8-10		-	-	38	ns
t_W	Pulse width	SHCP HIGH or LOW; See Figure 8-6		20	-	-	ns
		STCP HIGH or LOW; See Figure 8-7		20	-	-	ns
		$\overline{MR}$ LOW; See Figure 8-9		25	-	-	ns
t_{su}	Set-up time	DS to SHCP; See Figure 8-8		20	-	-	ns
		SHCP to STCP; See Figure 8-7		20	-	-	ns
t_h	DS to SHCP hold time	See Figure 8-8		3	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-9		13	-	-	ns
f_{max}	Maximum frequency	SHCP or STCP; See Figure 8-6 and Figure 8-7		24	-	-	MHz

7.4.5 AC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC595							
t_{PLH}, t_{PHL}	Propagation delay	SHCP to Q7S; See Figure 8-6	V_{CC}=2.0V	-	-	240	ns
			V_{CC}=4.5V	-	-	48	ns
			V_{CC}=6.0V	-	-	41	ns
		STCP to Qn; See Figure 8-7	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns

			V_{CC}=6.0V	-	-	45	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; See Figure 8-9	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
t_{PZH}, t_{PZL}	$\overline{OE}$ to Qn enable time	See Figure 8-10	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$ to Qn disable time	See Figure 8-10	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
t_W	Pulse width	SHCP HIGH or LOW; See Figure 8-6	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
		STCP HIGH or LOW; See Figure 8-7	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
		$\overline{MR}$ LOW; See Figure 8-9	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
t_{su}	Set-up time	DS to SHCP; See Figure 8-8	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
		SHCP to STCP; See Figure 8-7	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
t_h	DS to SHCP hold time	See Figure 8-8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-9	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
f_{max}	Maximum frequency	SHCP or STCP; See Figure 8-6 and Figure 8-7	V_{CC}=2.0V	4	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
CJ74HCT595; V_{CC}=4.5V to 5.5V							
t_{PLH}, t_{PHL}	Propagation delay	SHCP to Q7S; See Figure 8-6		-	-	63	ns
		STCP to Qn; See Figure 8-7		-	-	60	ns

t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; See Figure 8-9	-	-	60	ns
t_{PZH}, t_{PZL}	$\overline{OE}$ to Qn enable time	See Figure 8-10	-	-	53	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$ to Qn disable time	See Figure 8-10	-	-	45	ns
t_W	Pulse width	SHCP HIGH or LOW; See Figure 8-6	24	-	-	ns
		STCP HIGH or LOW; See Figure 8-7	24	-	-	ns
		$\overline{MR}$ LOW; See Figure 8-9	30	-	-	ns
t_{su}	Set-up time	DS to SHCP; See Figure 8-8	24	-	-	ns
		SHCP to STCP; See Figure 8-7	24	-	-	ns
t_h	DS to SHCP hold time	See Figure 8-8	3	-	-	ns
t_{rec}	$\overline{MR}$ to SHCP recovery time	See Figure 8-9	15	-	-	ns
f_{max}	Maximum frequency	SHCP or STCP; See Figure 8-6 and Figure 8-7	20	-	-	MHz

8 Detailed Description

8.1 Overview

The CJ74HC/HCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset /MR input. A LOW on /MR will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input (/OE) is LOW.

A HIGH on /OE causes the outputs to assume a high-impedance OFF-state. Operation of the /OE input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

8.2 Functional Block Diagram

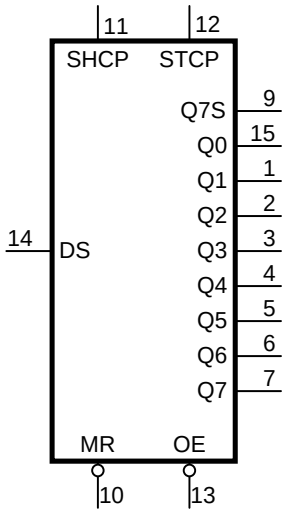


Figure 8-1 Logic symbol

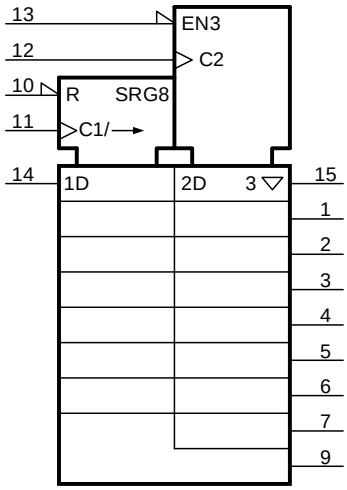


Figure 8-2 IEC logic symbol

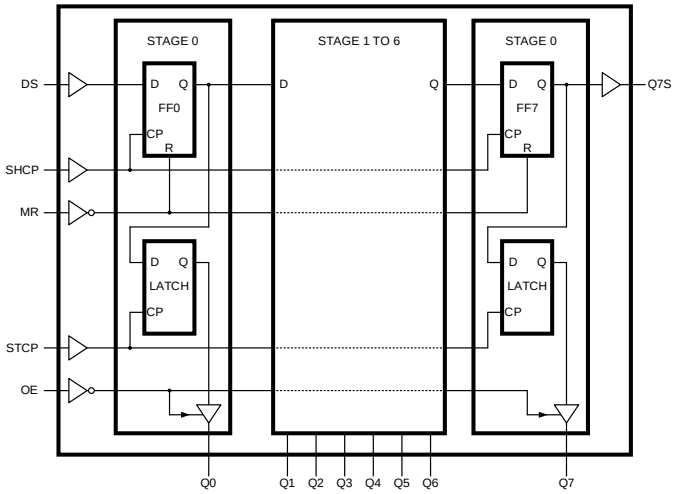


Figure 8-3 Logic diagram

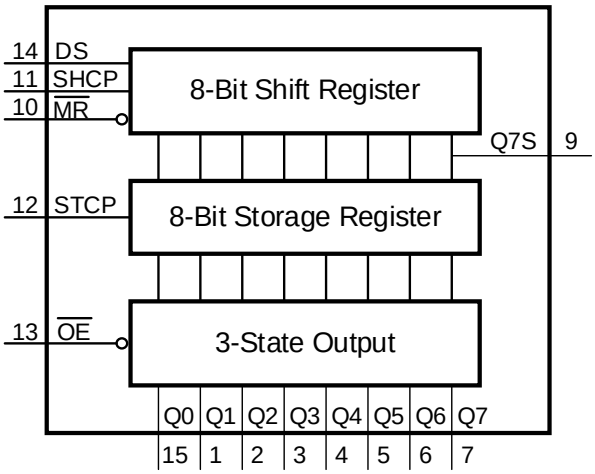


Figure 8-4 Function diagram

8.3 Function Table(1)

CONTROL				INPUT	OUTPUT		FUNCTION
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	A LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	Empty shift register loaded into storage register
X	X	H	L	X	L	Z	Shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	Logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. Previous state of stage 6 (internal Q6S) appears on the serial output (Q7S)
X	↑	L	H	X	NC	QnS	Contents of shift register stages (internal qns) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	Contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

(1) H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state; ↑ =LOW-to-HIGH transition; X=don't care; NC=no change.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

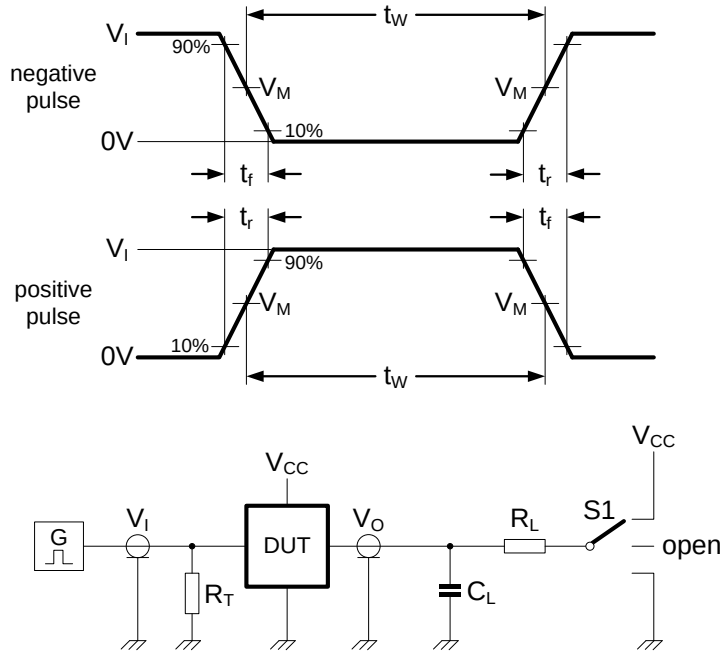


Figure 8-5 Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

8.4.2 AC Testing Waveforms

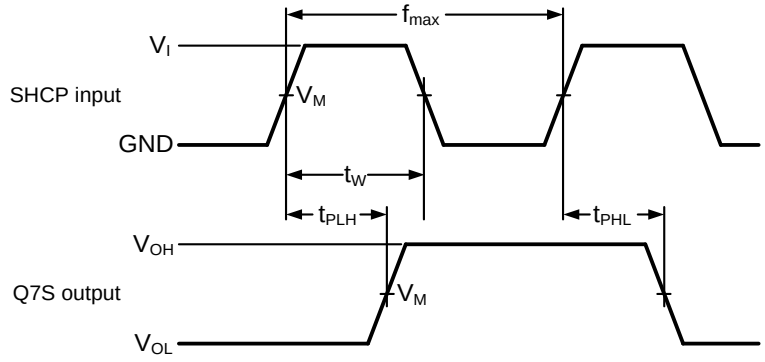


Figure 8-6 Shift clock pulse, maximum frequency and input to output propagation delays

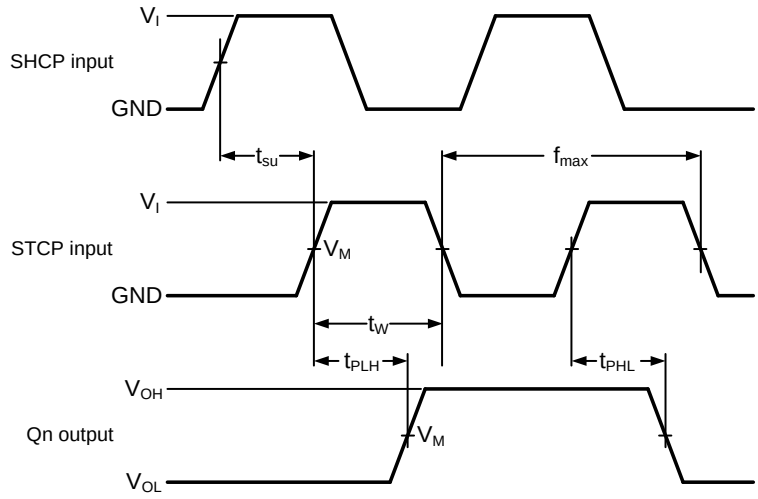


Figure 8-7 Storage clock to output propagation delays

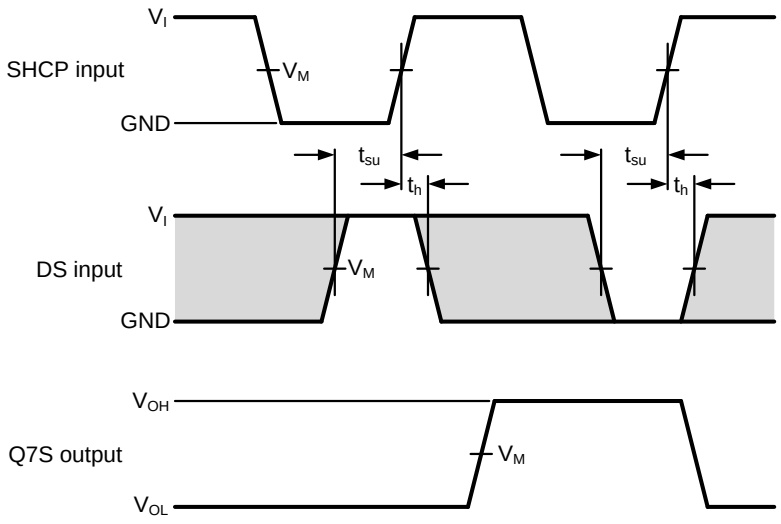


Figure 8-8 Data set-up and hold times

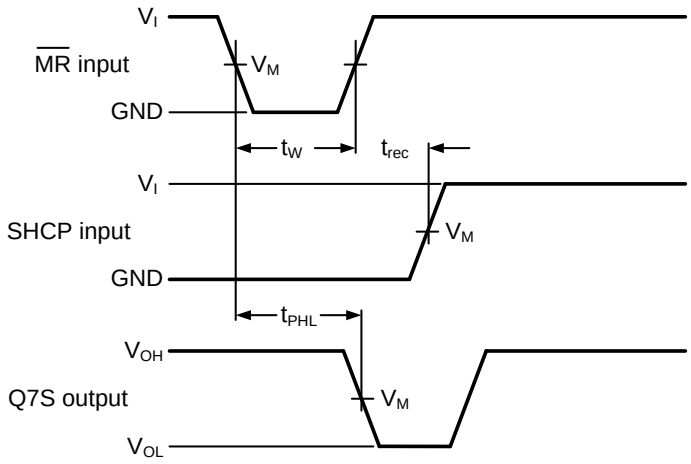


Figure 8-9 Master reset to output propagation delays

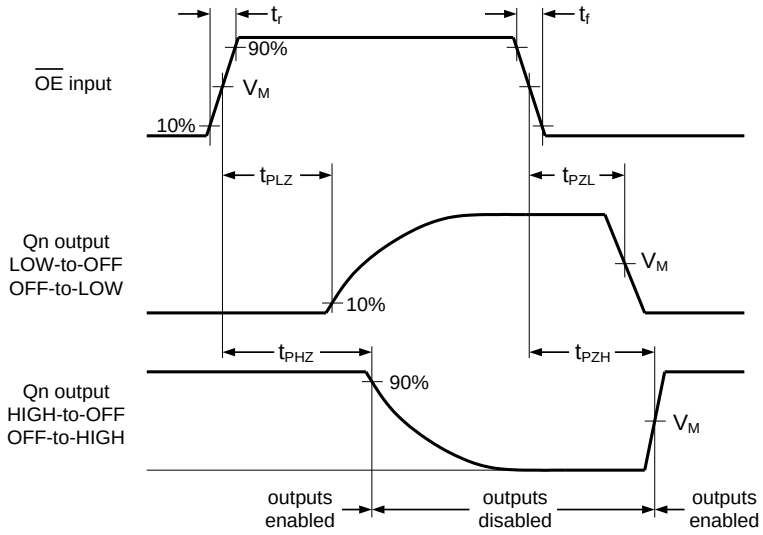


Figure 8-10 Enable and disable times

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT
	V_M	V_M
CJ74HC595	0.5xV_{CC}	0.5xV_{CC}
CJ74HCT595	1.3V	1.3V

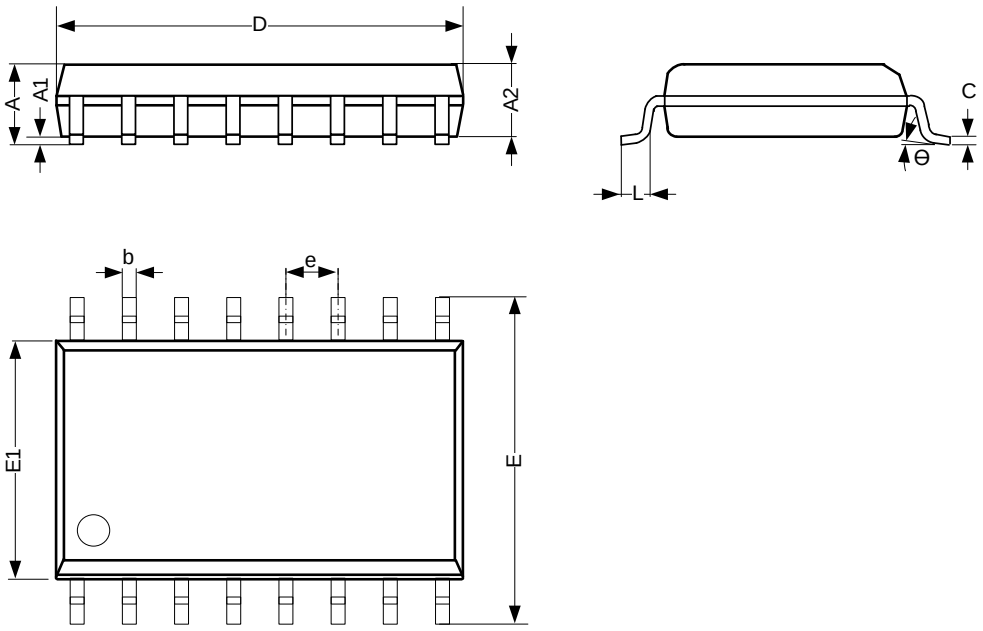
8.4.4 Test Data

TYPE	INPUT		LOAD		S1 POSITION		
	V_I	t_r,t_f	C_L	R_L	t_{PHL},t_{PLH}	t_{PZH},t_{PHZ}	t_{PZL},t_{PLZ}
CJ74HC595	V_{CC}	6ns	50pF	1kΩ	Open	GND	V_{CC}
CJ74HCT595	3V	6ns	50pF	1kΩ	Open	GND	V_{CC}

9 Mechanical Information

9.1 SOP16 Mechanical Information

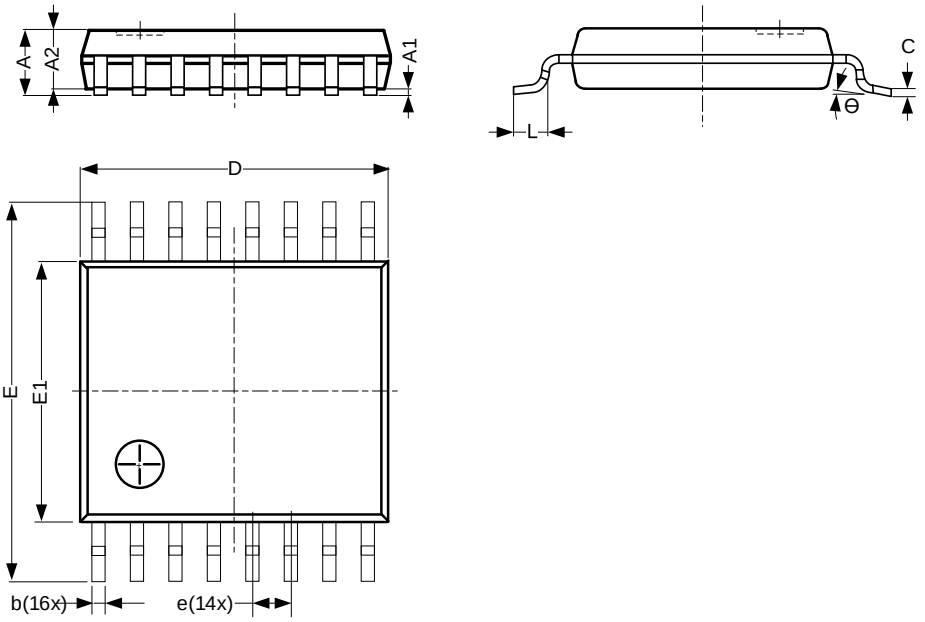
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

June, 2025: rev - 1.2, Correct the Figure 8-4.

September, 2025: rev - 1.3, Change marking information.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

Official Website: www.jscj-elec.com