

**8-bit Serial-in/Parallel-out Shift Register**

**CJ74LV164**

**Logic**

**1 Introduction**

The CJ74LV164 is a low-voltage, Si-gate CMOS device and is pin and function compatible with the CJ74HC164 and CJ74HCT164.

The CJ74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB) and either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock input (CP) and enters into Q0, which is the logical AND-function of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset input (MR) overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

**2 Available Packages**

PART NUMBER	PACKAGE
CJ74LV164	SOP14
	TSSOP14

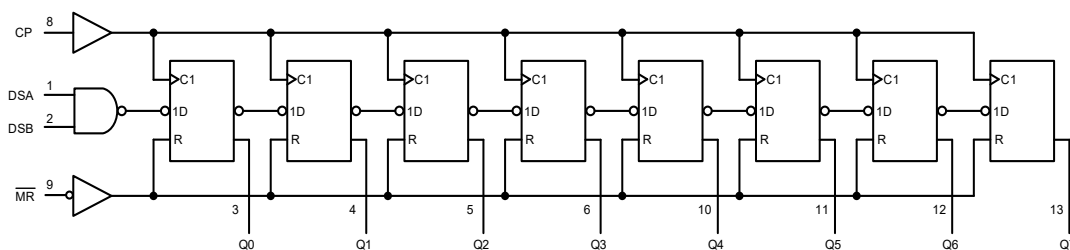
**Note:** For all available packages, please refer to the part Orderable Information.

**3 Features**

- Operating voltage: 1.0V to 5.5V
- 5.5V tolerant inputs/outputs
- Power-down mode
- Specified from -40°C to +125°C

**4 Applications**

- IP routers
- Enterprise switches
- Access control and security: access keypads and biometrics
- Smart meters: power line communication



Logic diagram

**5 Orderable Information**

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LV164ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74LV164BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

**Note:**

**ECO PLAN:** For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

**MSL:** Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

**SORT:** Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

## 6 Pin Configuration and Marking Information

### 6.1 Pin Configuration

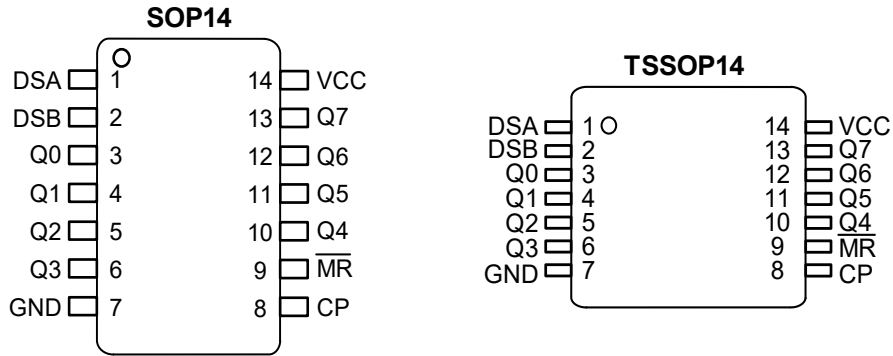


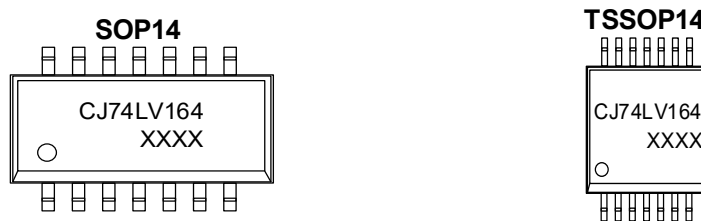
Figure 6-1 Pin configuration

### 6.2 Pin Function

PIN		I/O <sup>(1)</sup>	DESCRIPTION
No.	NAME		
1	DSA	I	Data input SA
2	DSB	I	Data input SB
3	Q0	O	Output 0
4	Q1	O	Output 1
5	Q2	O	Output 2
6	Q3	O	Output 3
7	GND	G	Ground (0V)
8	CP	I	Clock input (edge triggered LOW-to-HIGH)
9	$\overline{\text{MR}}$	I	Master reset input (active LOW)
10	Q4	O	Output 4
11	Q5	O	Output 5
12	Q6	O	Output 6
13	Q7	O	Output 7
14	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

### 6.3 Marking Information



XXXX: Code, indicates weekly record information.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

$T_{amb}=25^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$V_{CC}$	Supply voltage	-		-0.5	+7.0	V
$I_{IK}$	Input clamping current	$V_I < -0.5\text{V}$ or $V_I > V_{CC} + 0.5\text{V}^{(1)}$		-	$\pm 20$	mA
$I_{OK}$	Output clamping current	$V_O < -0.5\text{V}$ or $V_O > V_{CC} + 0.5\text{V}^{(1)}$		-	$\pm 50$	mA
$I_O$	Output current	$V_O = -0.5\text{V}$ to $(V_{CC} + 0.5\text{V})$		-	$\pm 25$	mA
$I_{CC}$	Supply current	-		-	50	mA
$I_{GND}$	Ground current	-		-50	-	mA
$T_{amb}$	Operating temperature	-		-40	+125	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature	-		-65	+150	$^{\circ}\text{C}$
$P_{tot}$	Total power dissipation	-		-	500	mW
$T_L$	Soldering temperature	10s	SOP/TSSOP	-	260	$^{\circ}\text{C}$

(1) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 Recommended Operating Conditions

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	Supply voltage	-(1)	1.0	3.3	5.5	V
$V_I$	Input voltage	-	0	-	$V_{CC}$	V
$V_O$	Output voltage	-	0	-	$V_{CC}$	V
$T_{amb}$	Ambient temperature	-	-40	-	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input transition rise and fall rate	$V_{CC}=1.0\text{V}$ to $2.0\text{V}$	-	-	500	ns/V
		$V_{CC}=2.0\text{V}$ to $2.7\text{V}$	-	-	200	ns/V
		$V_{CC}=2.7\text{V}$ to $3.6\text{V}$	-	-	100	ns/V
		$V_{CC}=3.6\text{V}$ to $5.5\text{V}$	-	-	50	ns/V

(1) The static characteristics are guaranteed from  $V_{CC}=1.2\text{V}$  to  $V_{CC}=5.5\text{V}$ , but LV devices are guaranteed to function down to  $V_{CC}=1.0\text{V}$  (with input levels GND or  $V_{CC}$ ).

**7.3 Electrical Characteristics**
**7.3.1 DC Characteristics 1**
 $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT	
$V_{IH}$	HIGH-level input voltage	$V_{CC}=1.2\text{V}$	0.9	-	-	V	
		$V_{CC}=2.0\text{V}$	1.4	-	-	V	
		$V_{CC}=2.7\text{V}$ to $3.6\text{V}$	2.0	-	-	V	
		$V_{CC}=4.5\text{V}$ to $5.5\text{V}$	$0.7V_{CC}$	-	-	V	
$V_{IL}$	LOW-level input voltage	$V_{CC}=1.2\text{V}$	-	-	0.3	V	
		$V_{CC}=2.0\text{V}$	-	-	0.6	V	
		$V_{CC}=2.7\text{V}$ to $3.6\text{V}$	-	-	0.8	V	
		$V_{CC}=4.5\text{V}$ to $5.5\text{V}$	-	-	$0.3V_{CC}$	V	
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_o = -100\mu\text{A}; V_{CC}=1.2\text{V}$	-	1.2	-	V
			$I_o = -100\mu\text{A}; V_{CC}=2.0\text{V}$	1.8	2.0	-	V
			$I_o = -100\mu\text{A}; V_{CC}=2.7\text{V}$	2.5	2.7	-	V
			$I_o = -100\mu\text{A}; V_{CC}=3.0\text{V}$	2.8	3.0	-	V
			$I_o = -100\mu\text{A}; V_{CC}=4.5\text{V}$	4.3	4.5	-	V
			$I_o = -6\text{mA}; V_{CC}=3.0\text{V}$	2.4	2.82	-	V
			$I_o = -12\text{mA}; V_{CC}=4.5\text{V}$	3.6	4.2	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_o = 100\mu\text{A}; V_{CC}=1.2\text{V}$	-	0	-	V
			$I_o = 100\mu\text{A}; V_{CC}=2.0\text{V}$	-	0	0.2	V
			$I_o = 100\mu\text{A}; V_{CC}=2.7\text{V}$	-	0	0.2	V
			$I_o = 100\mu\text{A}; V_{CC}=3.0\text{V}$	-	0	0.2	V
			$I_o = 100\mu\text{A}; V_{CC}=4.5\text{V}$	-	0	0.2	V
			$I_o = 6\text{mA}; V_{CC}=3.0\text{V}$	-	0.25	0.40	V
			$I_o = 12\text{mA}; V_{CC}=4.5\text{V}$	-	0.35	0.55	V
$I_I$	Input leakage current	$V_I = V_{CC}$ or GND; $V_{CC}=5.5\text{V}$	-	-	1.0	$\mu\text{A}$	
$I_{CC}$	Supply current	$V_I = V_{CC}$ or GND; $I_o = 0\text{A}; V_{CC}=5.5\text{V}$	-	-	20.0	$\mu\text{A}$	
$\Delta I_{CC}$	Additional supply current	Per input; $V_I = V_{CC} - 0.6\text{V}; V_{CC}=2.7\text{V}$ to $3.6\text{V}$	-	-	500	$\mu\text{A}$	
$C_i$	Input capacitance	-	-	3.5	-	pF	

(1) Typical values are measured at  $T_{amb} = 25^{\circ}\text{C}$ .

**7.3.2 DC Characteristics 2**

$T_{amb} = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT	
$V_{IH}$	HIGH-level input voltage	$V_{CC}=1.2\text{V}$	0.9	-	-	V	
		$V_{CC}=2.0\text{V}$	1.4	-	-	V	
		$V_{CC}=2.7\text{V}$ to $3.6\text{V}$	2.0	-	-	V	
		$V_{CC}=4.5\text{V}$ to $5.5\text{V}$	$0.7V_{CC}$	-	-	V	
$V_{IL}$	LOW-level input voltage	$V_{CC}=1.2\text{V}$	-	-	0.3	V	
		$V_{CC}=2.0\text{V}$	-	-	0.6	V	
		$V_{CC}=2.7\text{V}$ to $3.6\text{V}$	-	-	0.8	V	
		$V_{CC}=4.5\text{V}$ to $5.5\text{V}$	-	-	$0.3V_{CC}$	V	
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_O = -100\mu\text{A}; V_{CC} = 2.0\text{V}$	1.8	-	-	V
			$I_O = -100\mu\text{A}; V_{CC} = 2.7\text{V}$	2.5	-	-	V
			$I_O = -100\mu\text{A}; V_{CC} = 3.0\text{V}$	2.8	-	-	V
			$I_O = -100\mu\text{A}; V_{CC} = 4.5\text{V}$	4.3	-	-	V
			$I_O = -6\text{mA}; V_{CC} = 3.0\text{V}$	2.2	-	-	V
			$I_O = -12\text{mA}; V_{CC} = 4.5\text{V}$	3.5	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_O = 100\mu\text{A}; V_{CC} = 2.0\text{V}$	-	-	0.2	V
			$I_O = 100\mu\text{A}; V_{CC} = 2.7\text{V}$	-	-	0.2	V
			$I_O = 100\mu\text{A}; V_{CC} = 3.0\text{V}$	-	-	0.2	V
			$I_O = 100\mu\text{A}; V_{CC} = 4.5\text{V}$	-	-	0.2	V
			$I_O = 6\text{mA}; V_{CC} = 3.0\text{V}$	-	-	0.50	V
			$I_O = 12\text{mA}; V_{CC} = 4.5\text{V}$	-	-	0.65	V
$I_I$	Input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{V}$	-	-	1.0	$\mu\text{A}$	
$I_{CC}$	Supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{A}; V_{CC} = 5.5\text{V}$	-	-	160	$\mu\text{A}$	
$\Delta I_{CC}$	Additional supply current	Per input; $V_I = V_{CC} - 0.6\text{V}; V_{CC} = 2.7\text{V}$ to $3.6\text{V}$	-	-	850	$\mu\text{A}$	

(1) Typical values are measured at  $T_{amb} = 25^{\circ}\text{C}$ .

7.3.3 AC Characteristics 1

T<sub>amb</sub>=-40°C to +85°C, GND=0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP. (1)	MAX.	UNIT
t <sub>pd</sub>	Propagation delay	CP to Qn; See Figure 8-5(2)	V <sub>CC</sub> =1.2V	-	75	-	ns
			V <sub>CC</sub> =2.0V	-	26	39	ns
			V <sub>CC</sub> =2.7V	-	19	29	ns
			V <sub>CC</sub> =3.3V; C <sub>L</sub> =15pF	-	12	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	-	14	23	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	-	12	19	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR̄ to Qn; See Figure 8-6	V <sub>CC</sub> =1.2V	-	75	-	ns
			V <sub>CC</sub> =2.0V	-	26	39	ns
			V <sub>CC</sub> =2.7V	-	19	29	ns
			V <sub>CC</sub> =3.3V; C <sub>L</sub> =15pF	-	12	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	-	14	23	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	-	12	19	ns
t <sub>w</sub>	Pulse width	CP; See Figure 8-5	V <sub>CC</sub> =2.0V	34	-	-	ns
			V <sub>CC</sub> =2.7V	25	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	20	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	13	-	-	ns
		MR̄; See Figure 8-6	V <sub>CC</sub> =2.0V	34	-	-	ns
			V <sub>CC</sub> =2.7V	25	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	20	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	13	-	-	ns
t <sub>rec</sub>	Recovery time	MR̄ to CP; See Figure 8-6	V <sub>CC</sub> =1.2V	-	30	-	ns
			V <sub>CC</sub> =2.0V	19	-	-	ns
			V <sub>CC</sub> =2.7V	14	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	11	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	8	-	-	ns
t <sub>su</sub>	Set-up time	Dn to CP; See Figure 8-7	V <sub>CC</sub> =1.2V	-	15	-	ns
			V <sub>CC</sub> =2.0V	22	-	-	ns
			V <sub>CC</sub> =2.7V	16	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	13	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	9	-	-	ns
t <sub>h</sub>	Hold time Dn to CP	See Figure 8-7	V <sub>CC</sub> =1.2V	-	-10	-	ns
			V <sub>CC</sub> =2.0V	5	-	-	ns
			V <sub>CC</sub> =2.7V	5	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	5	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	5	-	-	ns

f <sub>max</sub>	Maximum frequency	See Figure 8-5	V <sub>CC</sub> =2.0V	14	40	-	MHz
			V <sub>CC</sub> =2.7V	19	58	-	MHz
			V <sub>CC</sub> =3.3V; C <sub>L</sub> =15pF	-	78	-	MHz
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	24	70	-	MHz
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	36	100	-	MHz
C <sub>PD</sub>	Power dissipation capacitance	V <sub>CC</sub> =3.3V; C <sub>L</sub> =50pF; f <sub>i</sub> =1MHz; V <sub>I</sub> =GND to V <sub>CC</sub> <sup>(4)</sup>	-	40	-	pF	

- (1) Typical values are measured at T<sub>amb</sub>=25°C.
- (2) t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- (3) Typical values are measured at nominal supply voltage (V<sub>CC</sub>=3.3V and V<sub>CC</sub>=5.0V).
- (4) C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub>=input frequency in MHz, f<sub>o</sub>=output frequency in MHz  
 C<sub>L</sub>=output load capacitance in pF  
 V<sub>CC</sub>=supply voltage in V  
 N=number of inputs switching  
 $\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of the outputs.

**7.3.4 AC Characteristics 2**

T<sub>amb</sub>=-40°C to +125°C, GND=0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT	
t <sub>pd</sub>	Propagation delay	CP to Qn; See Figure 8-5 <sup>(2)</sup>	V <sub>CC</sub> =2.0V	-	-	49	ns
			V <sub>CC</sub> =2.7V	-	-	36	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	-	-	29	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	-	-	24	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR to Qn; See Figure 8-6	V <sub>CC</sub> =2.0V	-	-	49	ns
			V <sub>CC</sub> =2.7V	-	-	36	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	-	-	29	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	-	-	24	ns
t <sub>w</sub>	Pulse width	CP; See Figure 8-5	V <sub>CC</sub> =2.0V	41	-	-	ns
			V <sub>CC</sub> =2.7V	30	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	24	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	16	-	-	ns
		MR; See Figure 8-6	V <sub>CC</sub> =2.0V	41	-	-	ns
			V <sub>CC</sub> =2.7V	30	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	24	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	16	-	-	ns
t <sub>rec</sub>	Recovery time	MR to CP; See Figure 8-6	V <sub>CC</sub> =2.0V	24	-	-	ns
			V <sub>CC</sub> =2.7V	18	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	14	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	10	-	-	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT	SYMBOL
t <sub>su</sub>	Set-up time	Dn to CP; See Figure 8-7	V <sub>CC</sub> =2.0V	26	-	-	ns
			V <sub>CC</sub> =2.7V	19	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	15	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	10	-	-	ns
t <sub>h</sub>	Hold time Dn to CP	See Figure 8-7	V <sub>CC</sub> =2.0V	5	-	-	ns
			V <sub>CC</sub> =2.7V	5	-	-	ns
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	5	-	-	ns
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	5	-	-	ns
f <sub>max</sub>	Maximum frequency	See Figure 8-5	V <sub>CC</sub> =2.0V	12	-	-	MHz
			V <sub>CC</sub> =2.7V	16	-	-	MHz
			V <sub>CC</sub> =3.0V to 3.6V <sup>(3)</sup>	20	-	-	MHz
			V <sub>CC</sub> =4.5V to 5.5V <sup>(3)</sup>	30	-	-	MHz

(1) All typical values are measured at T<sub>amb</sub>=25°C.

(2) t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

(3) Typical values are measured at nominal supply voltage (V<sub>CC</sub>=3.3V and V<sub>CC</sub>=5.0V).

## 8 Detailed Description

### 8.1 Overview

The CJ74LV164 is a low-voltage, Si-gate CMOS device and is pin and function compatible with the CJ74HC164 and CJ74HCT164.

The CJ74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB) and either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock input (CP) and enters into Q0, which is the logical AND-function of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset input (MR) overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

### 8.2 Functional Block Diagram

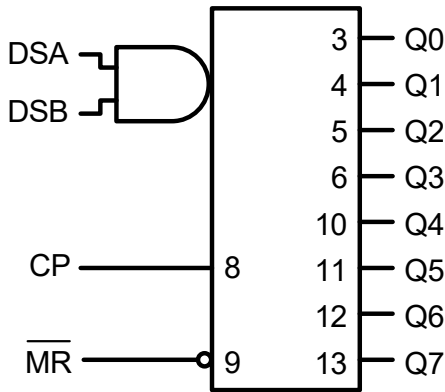


Figure 8-1 Logic symbol

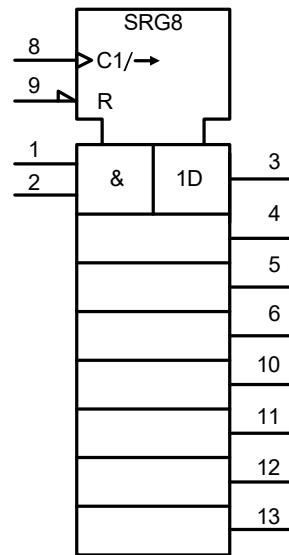


Figure 8-2 IEC logic symbol

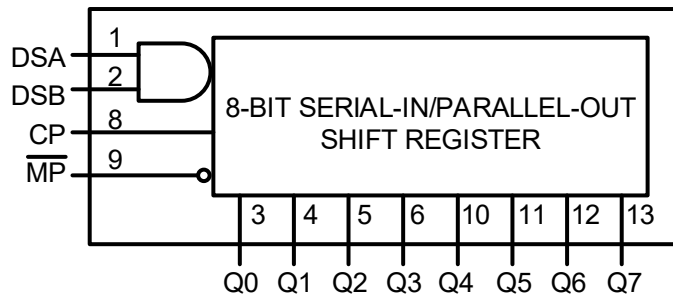


Figure 8-3 Functional diagram

8.3 Function Table

OPERATING MODE	INPUT				OUTPUT	
	MR	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

Note:

- (1) H=HIGH voltage level; L=LOW voltage level;
- (2) ↑=LOW-to-HIGH clock transition;
- (3) h=HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
- (4) l=LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
- (5) q=lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

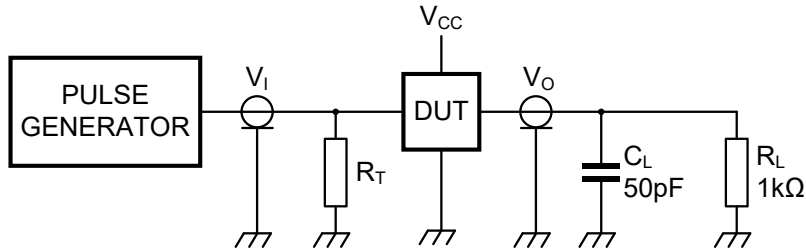


Figure 8-4 Test circuit for measuring switching times

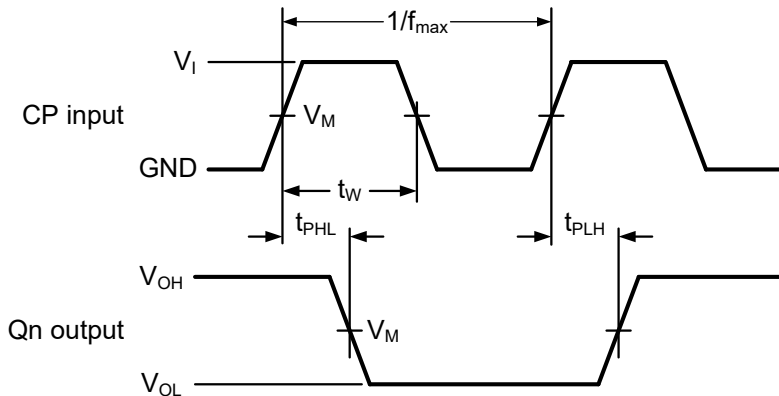
Definitions for test circuit:

R<sub>L</sub>=Load resistance.

C<sub>L</sub>=Load capacitance including jig and probe capacitance.

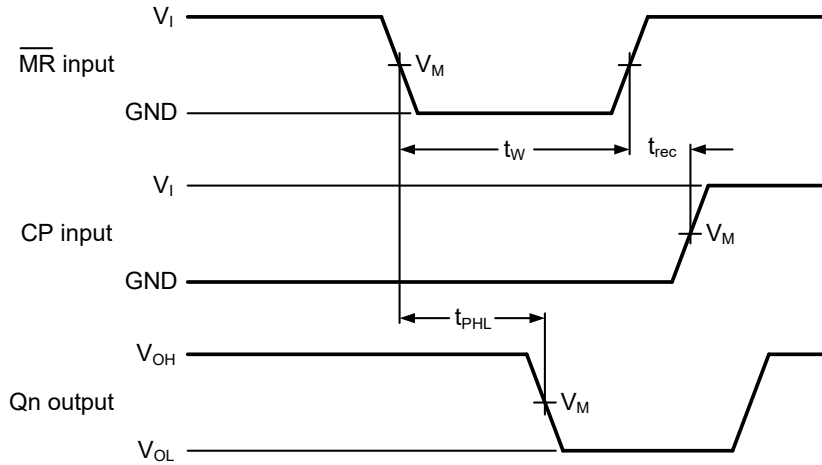
R<sub>T</sub>=Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

8.4.2 AC Testing Waveforms



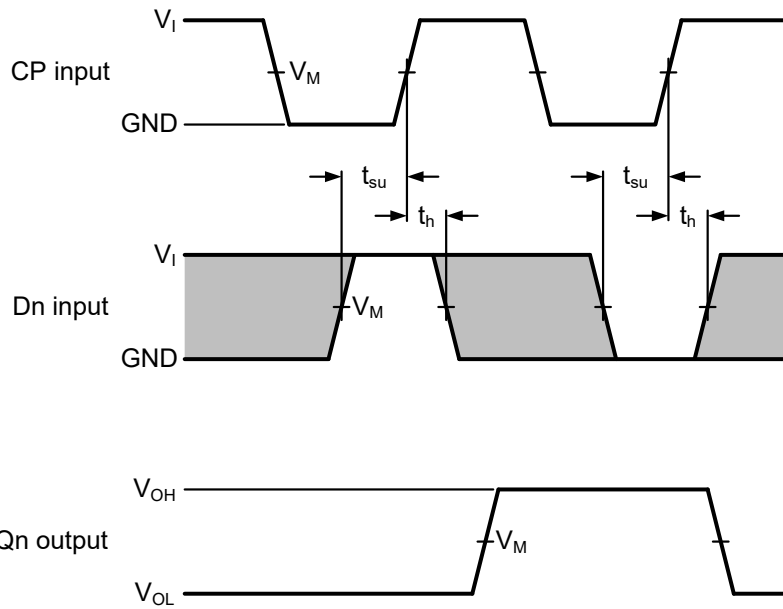
V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load

Figure 8-5 Propagation delay clock (CP) to output (Qn), clock pulse width and maximum clock frequency



$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load

**Figure 8-6 Pulse width master reset ( $\overline{\text{MR}}$ ), propagation delay master reset ( $\overline{\text{MR}}$ ) to output (Qn) and the master reset ( $\overline{\text{MR}}$ ) to clock (CP) recovery time**



$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load

The shaded areas indicate when the input is permitted to change for predictable output performance  
**Figure 8-7 Data set-up and hold times inputs (Dn) to clock (CP)**

**8.4.3 Measurement Points**

SUPPLY VOLTAGE	INPUT	OUTPUT
$V_{CC}$	$V_M$	$V_M$
1.2V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.0V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

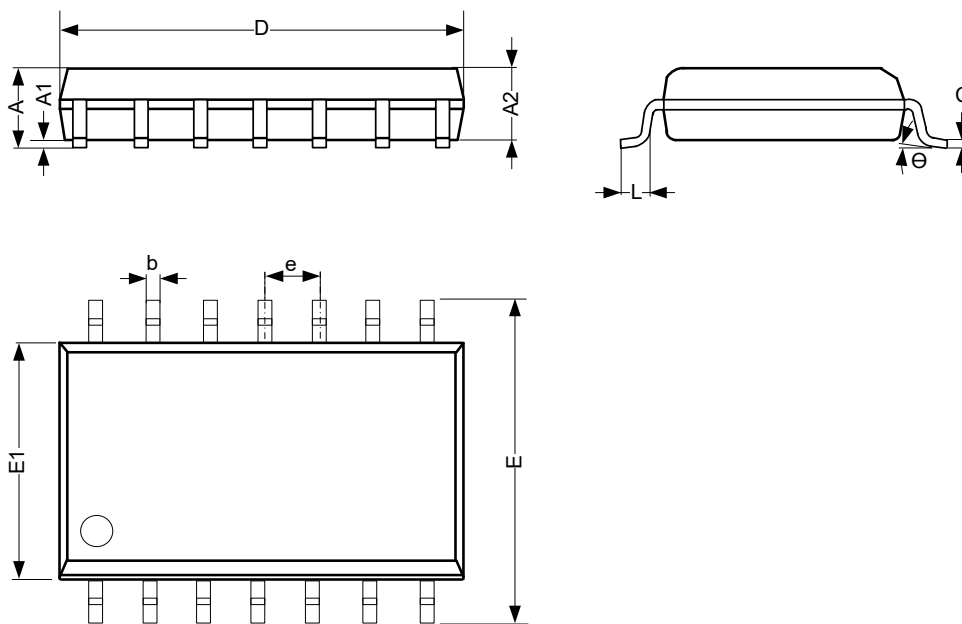
**8.4.4 Test Data**

SUPPLY VOLTAGE	INPUT		LOAD		TEST
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	
1.2V	$V_{CC}$	$\leq 2.5\text{ns}$	50pF	1k $\Omega$	$t_{PHL}, t_{PLH}$
2.0V	$V_{CC}$	$\leq 2.5\text{ns}$	50pF	1k $\Omega$	$t_{PHL}, t_{PLH}$
2.7V	2.7V	$\leq 2.5\text{ns}$	50pF	1k $\Omega$	$t_{PHL}, t_{PLH}$
3.0V to 3.6V	2.7V	$\leq 2.5\text{ns}$	50pF, 15pF	1k $\Omega$	$t_{PHL}, t_{PLH}$
4.5V to 5.5V	$V_{CC}$	$\leq 2.5\text{ns}$	50pF	1k $\Omega$	$t_{PHL}, t_{PLH}$

9 Mechanical Information

9.1 SOP14 Mechanical Information

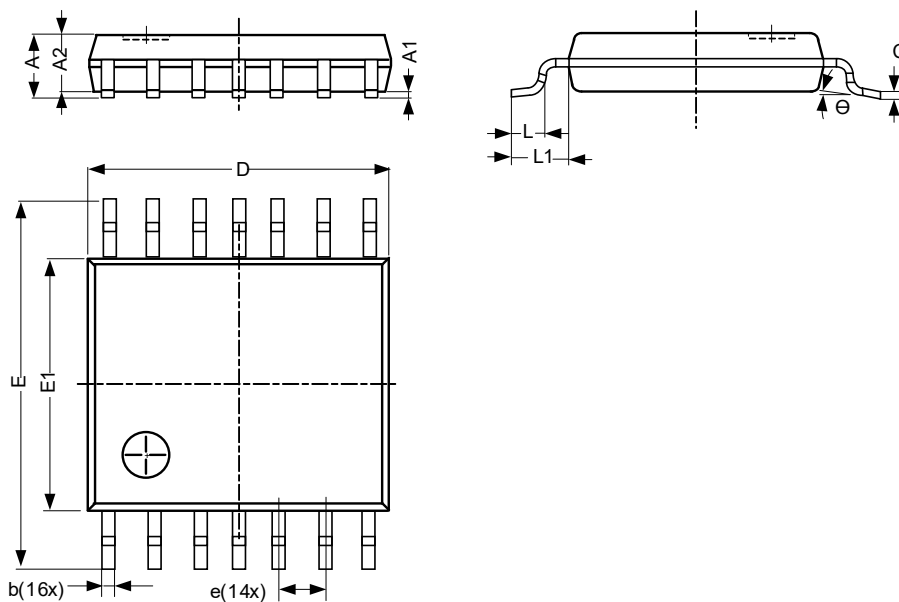
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
$\theta$	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

## 10 Notes and Revision History

### 10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

### 10.2 Notes

#### Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

# DISCLAIMER

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