8-bit Parallel-in/Serial-out Shift Register

CJ74LV165 Logic

1 Introduction

The CJ74LV165 is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q7 and /Q7) available from the last stage.

Schmitt-trigger action at all inputs, makes the circuit tolerant for slower input rise and fall times.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LV165	SOP16
	SSOP16
	TSSOP16
	QFN4x3.5-16L

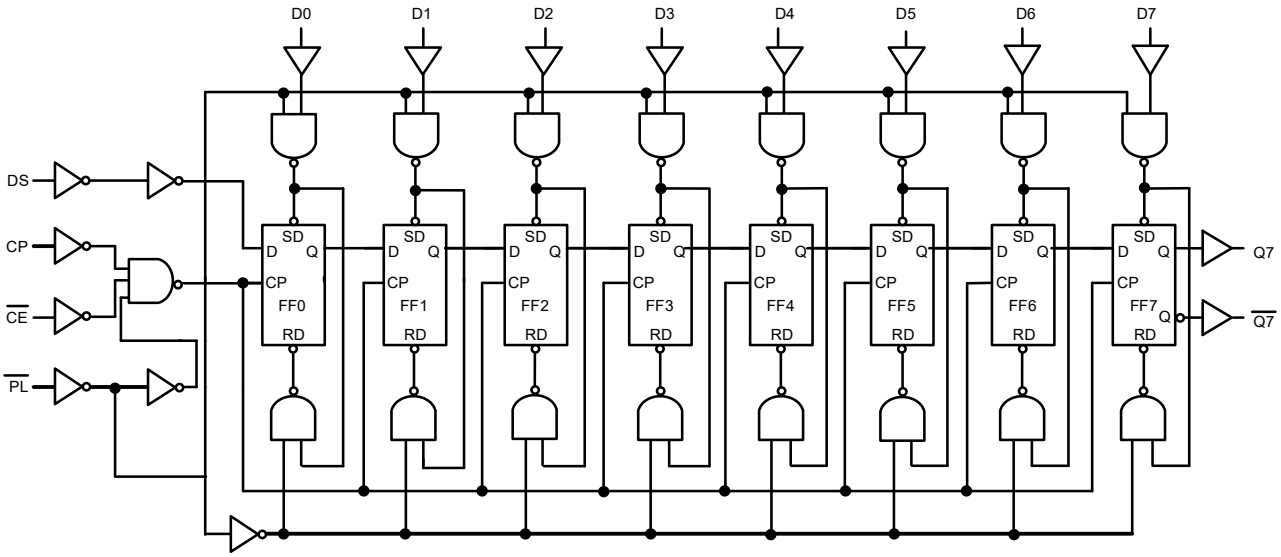
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide operating voltage: 1.0V to 5.5V
- 5.5 V tolerant inputs/outputs
- Power-down mode
- Specified from -40°C to +125°C

4 Applications

- Increase the Number of Inputs on a Microcontroller



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LV165AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CJ74LV165SEN	SSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2500 Units/Reel	Active
CJ74LV165BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active
CJ74LV165QGN	QFN4x3.5-16L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 1500 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

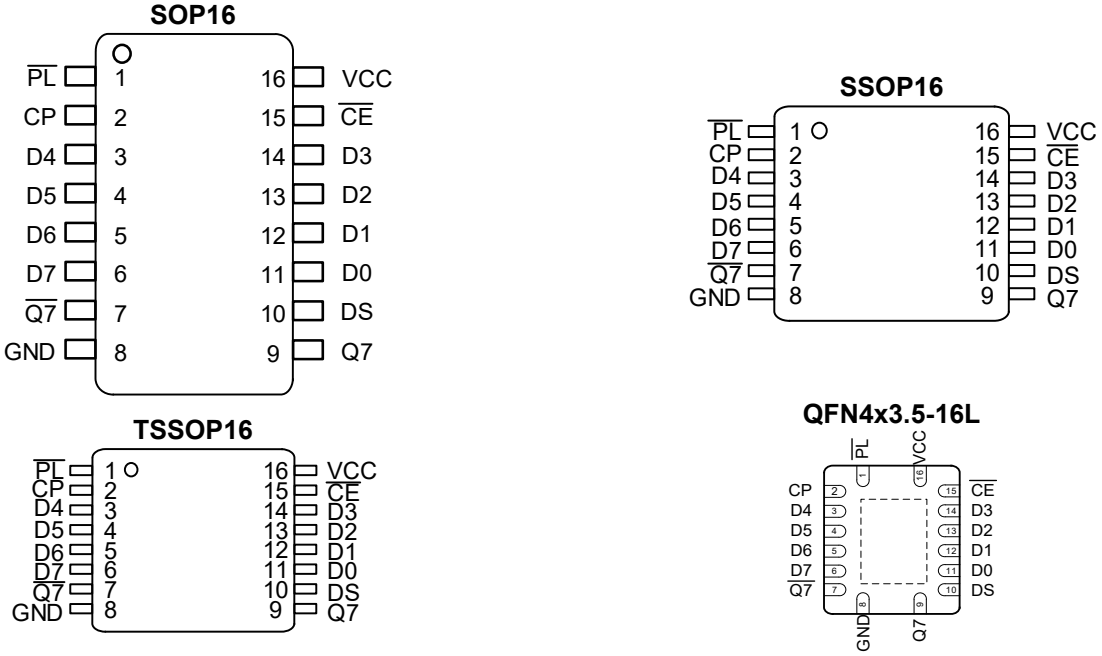


Figure 6-1 Pin configuration

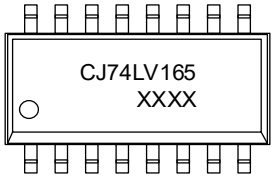
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	$\overline{PL}$	I	Parallel enable input (active LOW)
2	CP	I	Clock input (LOW-to-HIGH edge-triggered)
3	D4	I	Parallel data input
4	D5	I	Parallel data input
5	D6	I	Parallel data input
6	D7	I	Parallel data input
7	$\overline{Q7}$	O	Complementary serial output from the last stage
8	GND	G	Ground (0V)
9	Q7	O	Serial output from the last stage
10	DS	I	Serial data input
11	D0	I	Parallel data input
12	D1	I	Parallel data input
13	D2	I	Parallel data input
14	D3	I	Parallel data input
15	$\overline{CE}$	I	Clock enable input (active LOW)
16	VCC	P	Positive supply voltage

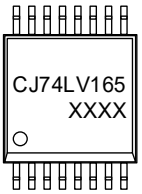
(1) I-Input, O-Output, P-Power, G-Ground.

6.3 Marking Information

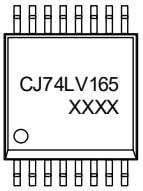
SOP16



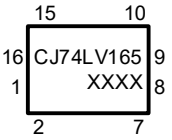
SSOP16



TSSOP16



QFN4x3.5-16L



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

T_{amb}=25°C, all voltage referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-	-0.5	+7.0	V
V_I	Input voltage	-	-0.5	+7.0	V
I_{IK}	Input clamping current	V_I<-0.5V or V_I>V_{CC}+0.5V	-	+20	mA
I_{OK}	Output clamping current	V_O>V_{CC} or V_O<0	-	±50	mA
I_O	Output current	V_O=-0.5V to (V_{CC}+0.5V)	-	±25	mA
I_{CC}	Supply current	-	-	+50	mA
I_{GND}	Ground current	-	-50	-	mA
T_{stg}	Storage temperature	-	-65	+150	°C
P_{tot}	Total power dissipation	-	-	500	mW
T_L	Soldering temperature	10s	260		°C

7.2 Recommended Operating Conditions

All voltage referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	-	1.0	3.3	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 Electrical Characteristics

7.3.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=1.2V		0.9	-	-	V
		V_{CC}=2.3V to 2.7V		1.4	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=1.2V		-	-	0.3	V
		V_{CC}=2.3V to 2.7V		-	-	0.6	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.2V	-	1.2	-	V
			I_O=-100uA; V_{CC}=2.0V	1.8	2.0	-	V
			I_O=-100uA; V_{CC}=2.7V	2.5	2.7	-	V
			I_O=-100uA; V_{CC}=3.0V	2.8	3.0	-	V
			I_O=-100uA; V_{CC}=4.5V	4.3	4.5	-	V
			I_O=-6mA; V_{CC}=3.0V	2.4	2.82	-	V
			I_O=-12mA; V_{CC}=4.5V	3.6	4.2	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.2V	-	0	-	V
			I_O=100uA; V_{CC}=2.0V	-	0	0.2	V
			I_O=100uA; V_{CC}=2.7V	-	0	0.2	V
			I_O=100uA; V_{CC}=3.0V	-	0	0.2	V
			I_O=100uA; V_{CC}=4.5V	-	0	0.2	V
			I_O=6mA; V_{CC}=3.0V	-	0.25	0.4	V
			I_O=12mA; V_{CC}=4.5V	-	0.35	0.55	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1	uA
I_{OFF}	Power-off leakage current	V_I or V_O=5.5V; V_{CC}=0V		-	-	±5	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	20	uA
ΔI_{CC}	Additional supply current	Per input; V_I=V_{CC}-0.6V; V_{CC}=2.7V to 3.6V		-	-	500	uA

7.3.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=1.2V		0.9	-	-	V
		V_{CC}=2.3V to 2.7V		1.4	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		$0.7V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=1.2V		-	-	0.3	V
		V_{CC}=2.3V to 2.7V		-	-	0.6	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	$0.3V_{CC}$	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=2.0V	1.8	-	-	V
			I_O=-100uA; V_{CC}=2.7V	2.5	-	-	V
			I_O=-100uA; V_{CC}=3.0V	2.8	-	-	V
			I_O=-100uA; V_{CC}=4.5V	4.3	-	-	V
			I_O=-6mA; V_{CC}=3.0V	2.2	-	-	V
			I_O=-12mA; V_{CC}=4.5V	3.5	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=100uA; V_{CC}=2.0V	1.8	-	0.2	V
			I_O=100uA; V_{CC}=2.7V	2.5	-	0.2	V
			I_O=100uA; V_{CC}=3.0V	2.8	-	0.2	V
			I_O=100uA; V_{CC}=4.5V	4.3	-	0.2	V
			I_O=6mA; V_{CC}=3.0V	-	-	0.5	V
			I_O=12mA; V_{CC}=4.5V	-	-	0.65	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1	uA
I_{OFF}	Power-off leakage current	V_I or V_O=5.5V; V_{CC}=0V		-	-	±10	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
ΔI_{CC}	Additional supply current	Per input; V_I=V_{CC}-0.6V; V_{CC}=2.7V to 3.6V		-	-	850	uA

7.3.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, GND=0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}/t_{PLH}	Propagation delay	$\overline{CE}$, CP to Q7,$\overline{Q7}$; See Figure 8-5 and Figure 8-6	V_{CC}=1.2V	-	115	-	ns
			V_{CC}=2.0V	-	38	61	ns
			V_{CC}=2.7V	-	27	43	ns
			V_{CC}=3.0V to 3.6V	-	22	36	ns
			V_{CC}=3.3V; C_L=15pF	-	18	-	ns
			V_{CC}=4.5V to 5.5V	-	15	24	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; See Figure 8-6	V_{CC}=1.2V	-	110	-	ns
			V_{CC}=2.0V	-	35	56	ns
			V_{CC}=2.7V	-	24	39	ns
			V_{CC}=3.0V to 3.6V	-	20	33	ns
			V_{CC}=3.3V; C_L=15pF	-	18	-	ns
			V_{CC}=4.5V to 5.5V	-	14	22	ns
		D7 to Q7, $\overline{Q7}$; See Figure 8-7	V_{CC}=1.2V	-	90	-	ns
			V_{CC}=2.0V	-	28	45	ns
			V_{CC}=2.7V	-	20	32	ns
			V_{CC}=3.0V to 3.6V	-	17	27	ns
			V_{CC}=3.3V; C_L=15pF	-	14	-	ns
			V_{CC}=4.5V to 5.5V	-	11	18	ns
t_W	Pulse width	CP input HIGH to LOW; See Figure 8-5	V_{CC}=2.0V	34	-	-	ns
			V_{CC}=2.7V	25	-	-	ns
			V_{CC}=3.0V to 3.6V	20	-	-	ns
			V_{CC}=4.5V to 5.5V	15	-	-	ns
		$\overline{PL}$ input LOW; See Figure 8-6	V_{CC}=2.0V	34	-	-	ns
			V_{CC}=2.7V	25	-	-	ns
			V_{CC}=3.0V to 3.6V	20	-	-	ns
			V_{CC}=4.5V to 5.5V	15	-	-	ns
t_{rec}	Recovery time	$\overline{PL}$ to CP, $\overline{CE}$; See Figure 8-6	V_{CC}=1.2V	-	-	-	ns
			V_{CC}=2.0V	24	-	-	ns
			V_{CC}=2.7V	18	-	-	ns
			V_{CC}=3.0V to 3.6V	17	-	-	ns
			V_{CC}=4.5V to 5.5V	12	-	-	ns
t_{su}	Set-up time	DS to CP, $\overline{CE}$; See Figure 8-8	V_{CC}=1.2V	-	-	-	ns
			V_{CC}=2.0V	22	-	-	ns
			V_{CC}=2.7V	16	-	-	ns
			V_{CC}=3.0V to 3.6V	13	-	-	ns

			V_{CC}=4.5V to 5.5V	9	-	-	ns
		$\overline{CE}$ to CP, CP to $\overline{CE}$; See Figure 8-8	V_{CC}=1.2V	-	-	-	ns
			V_{CC}=2.0V	22	-	-	ns
			V_{CC}=2.7V	16	-	-	ns
			V_{CC}=3.0V to 3.6V	13	-	-	ns
			V_{CC}=4.5V to 5.5V	9	-	-	ns
		Dn to $\overline{PL}$; See Figure 8-9	V_{CC}=1.2V	-	-	-	ns
			V_{CC}=2.0V	22	-	-	ns
			V_{CC}=2.7V	16	-	-	ns
			V_{CC}=3.0V to 3.6V	13	-	-	ns
			V_{CC}=4.5V to 5.5V	9	-	-	ns
t_h	Hold time	DS to CP, $\overline{CE}$; Dn to $\overline{PL}$; See Figure 8-8 and 8-9	V_{CC}=1.2V	-	-	-	ns
			V_{CC}=2.0V	22	-	-	ns
			V_{CC}=2.7V	16	-	-	ns
			V_{CC}=3.0V to 3.6V	13	-	-	ns
			V_{CC}=4.5V to 5.5V	9	-	-	ns
		$\overline{CE}$ to CP, CP to $\overline{CE}$; See Figure 8-8	V_{CC}=1.2V	-	-	-	ns
			V_{CC}=2.0V	5	-	-	ns
			V_{CC}=2.7V	5	-	-	ns
			V_{CC}=3.0V to 3.6V	5	-	-	ns
			V_{CC}=4.5V to 5.5V	5	-	-	ns
f_{max}	Maximum frequency	See Figure 8-5	V_{CC}=2.0V	14	-	-	MHz
			V_{CC}=2.7V	19	-	-	MHz
			V_{CC}=3.0V to 3.6V	24	-	-	MHz
			V_{CC}=3.3V; C_L=15pF	-	-	-	MHz
			V_{CC}=4.5V to 5.5V	36	-	-	MHz

7.3.4 AC Characteristics 2

T_{amb}=-40°C to +125°C, GND=0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}/t_{PLH}	Propagation delay	$\overline{CE}$, CP to Q7,$\overline{Q7}$; See Figure 8-5 and Figure 8-6	V_{CC}=2.0V	-	-	76	ns
			V_{CC}=2.7V	-	-	54	ns
			V_{CC}=3.0V to 3.6V	-	-	45	ns
			V_{CC}=4.5V to 5.5V	-	-	30	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; See Figure 8-6	V_{CC}=2.0V	-	-	70	ns
			V_{CC}=2.7V	-	-	49	ns
			V_{CC}=3.0V to 3.6V	-	-	41	ns
			V_{CC}=4.5V to 5.5V	-	-	27	ns
		D7 to Q7, $\overline{Q7}$; See Figure 8-7	V_{CC}=2.0V	-	-	56	ns
			V_{CC}=2.7V	-	-	40	ns
			V_{CC}=3.0V to 3.6V	-	-	33	ns
			V_{CC}=4.5V to 5.5V	-	-	22	ns
t_W	Pulse width	CP input HIGH to LOW; See Figure 8-5	V_{CC}=2.0V	41	-	-	ns
			V_{CC}=2.7V	30	-	-	ns
			V_{CC}=3.0V to 3.6V	24	-	-	ns
			V_{CC}=4.5V to 5.5V	18	-	-	ns
		$\overline{PL}$ input LOW; See Figure 8-6	V_{CC}=2.0V	41	-	-	ns
			V_{CC}=2.7V	30	-	-	ns
			V_{CC}=3.0V to 3.6V	24	-	-	ns
			V_{CC}=4.5V to 5.5V	18	-	-	ns
t_{rec}	Recovery time	$\overline{PL}$ to CP, $\overline{CE}$; See Figure 8-6	V_{CC}=2.0V	30	-	-	ns
			V_{CC}=2.7V	23	-	-	ns
			V_{CC}=3.0V to 3.6V	21	-	-	ns
			V_{CC}=4.5V to 5.5V	15	-	-	ns
t_{su}	Set-up time	DS to CP, $\overline{CE}$; See Figure 8-8	V_{CC}=2.0V	26	-	-	ns
			V_{CC}=2.7V	19	-	-	ns
			V_{CC}=3.0V to 3.6V	15	-	-	ns
			V_{CC}=4.5V to 5.5V	10	-	-	ns
		$\overline{CE}$ to CP, CP to $\overline{CE}$; See Figure 8-8	V_{CC}=2.0V	26	-	-	ns
			V_{CC}=2.7V	19	-	-	ns
			V_{CC}=3.0V to 3.6V	15	-	-	ns
			V_{CC}=4.5V to 5.5V	10	-	-	ns
		Dn to $\overline{PL}$; See Figure 8-9	V_{CC}=2.0V	26	-	-	ns
			V_{CC}=2.7V	19	-	-	ns
			V_{CC}=3.0V to 3.6V	15	-	-	ns

			V_{CC}=4.5V to 5.5V	10	-	-	ns
t_h	Hold time	DS to CP, $\overline{CE}$; Dn to $\overline{PL}$; See Figure 8-8 and 8-9	V_{CC}=2.0V	26	-	-	ns
			V_{CC}=2.7V	19	-	-	ns
			V_{CC}=3.0V to 3.6V	15	-	-	ns
			V_{CC}=4.5V to 5.5V	10	-	-	ns
		$\overline{CE}$ to CP, CP to $\overline{CE}$; See Figure 8-8	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=2.7V	5	-	-	ns
			V_{CC}=3.0V to 3.6V	5	-	-	ns
			V_{CC}=4.5V to 5.5V	5	-	-	ns
f_{max}	Maximum frequency	See Figure 8-5	V_{CC}=2.0V	12	-	-	MHz
			V_{CC}=2.7V	16	-	-	MHz
			V_{CC}=3.0V to 3.6V	20	-	-	MHz
			V_{CC}=4.5V to 5.5V	30	-	-	MHz

8 Detailed Description

8.1 Overview

The CJ74LV165 is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q7 and /Q7) available from the last stage.

Schmitt-trigger action at all inputs, makes the circuit tolerant for slower input rise and fall times.

8.2 Functional Block Diagram

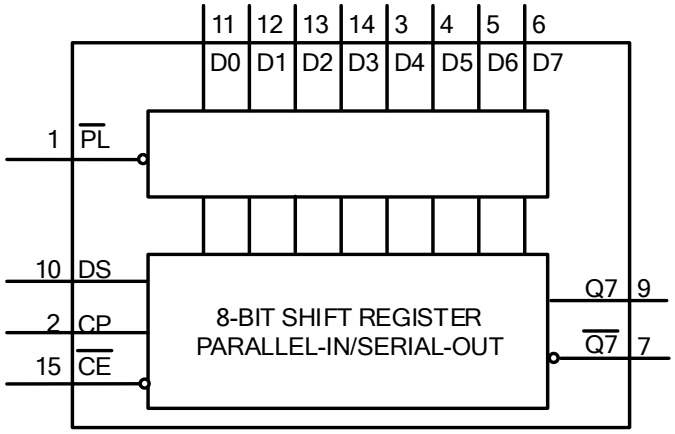


Figure 8-1 Functional diagram

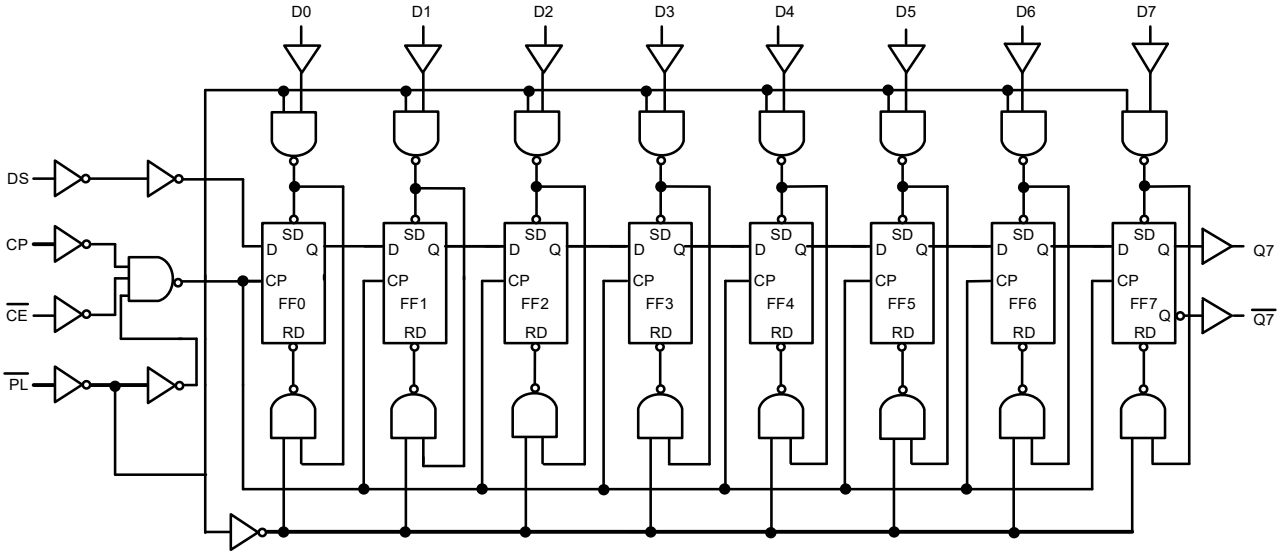


Figure 8-2 Logic diagram

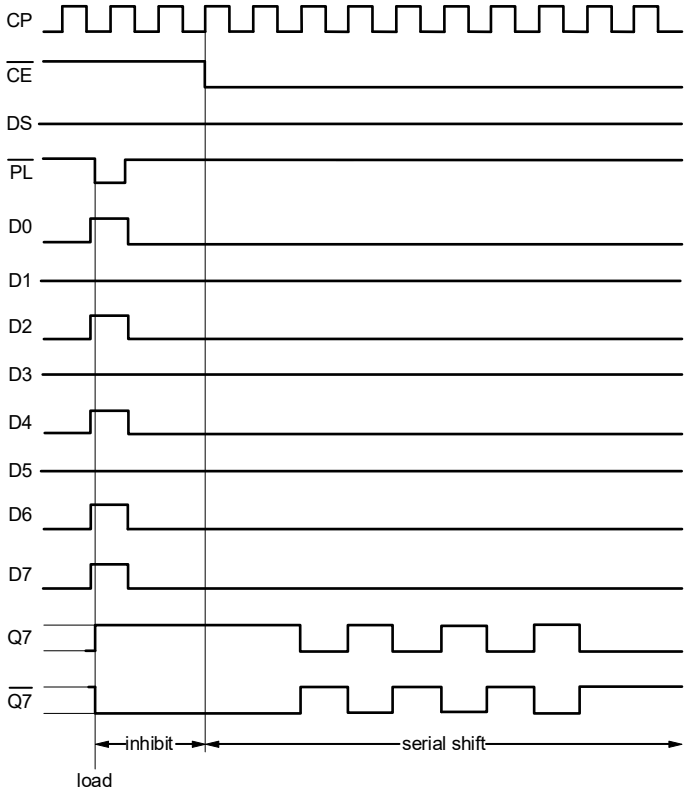


Figure 8-3 Timing diagram

8.3 Function Table

OPERATING MODE	INPUT					Qn REGISTERS		OUTPUT	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q0 to Q6	Q7	$\overline{Q7}$
Parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
Serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
Hold “do nothing”	H	H	X	X	X	q0	q1 to q6	q7	q7

Note:

H=HIGH voltage level; L=LOW voltage level; X=don’t care;

↑=LOW-to-HIGH clock transition;

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;

l=LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;

q=state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

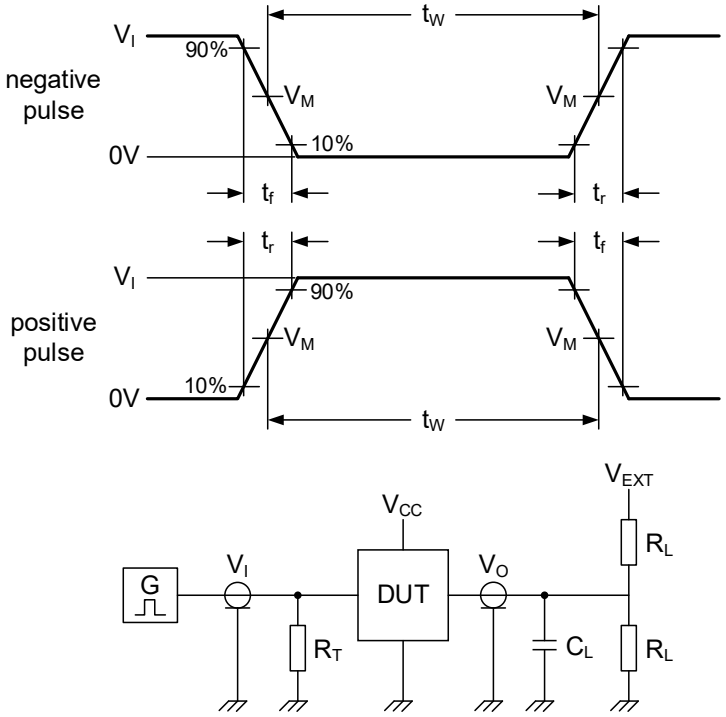


Figure 8-4 Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT}=External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

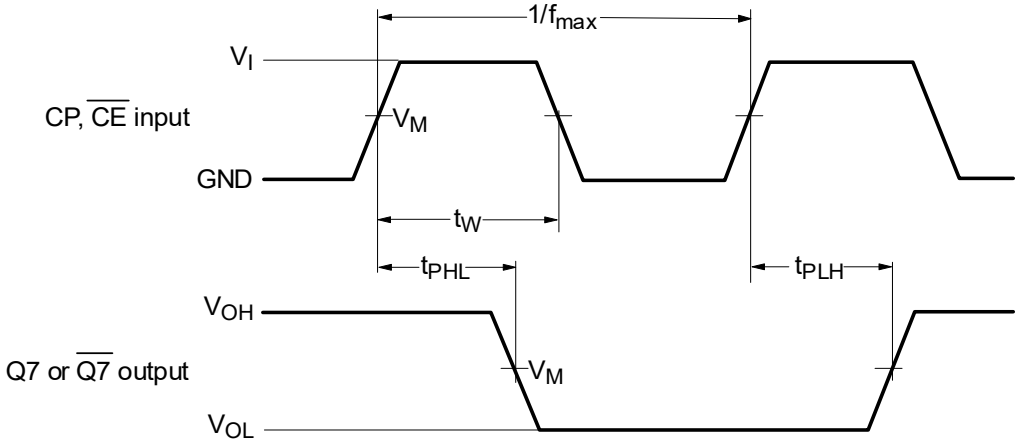


Figure 8-5 Clock pulse (CP) and clock enable ($\overline{CE}$) to output (Q7 or $\overline{Q7}$) propagation delays, clock pulse width and maximum clock frequency

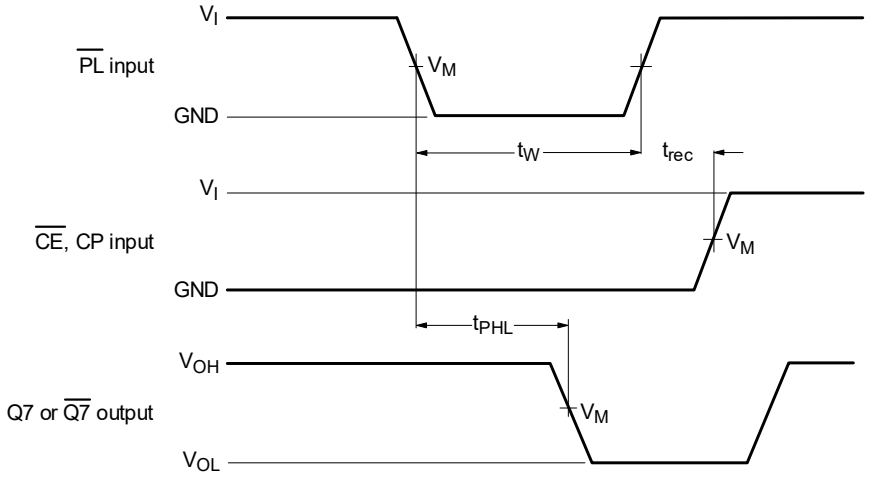


Figure 8-6 Parallel load ($\overline{PL}$) pulse width, parallel load to output (Q7 or $\overline{Q7}$) propagation delays, parallel load to clock (CP) and clock enable ($\overline{CE}$) recovery time

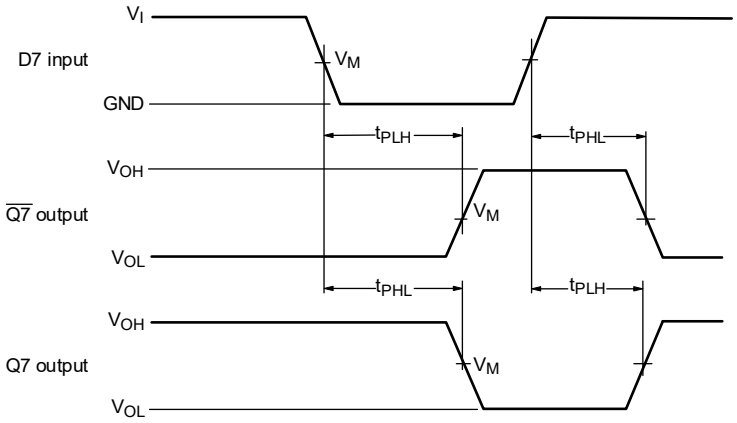
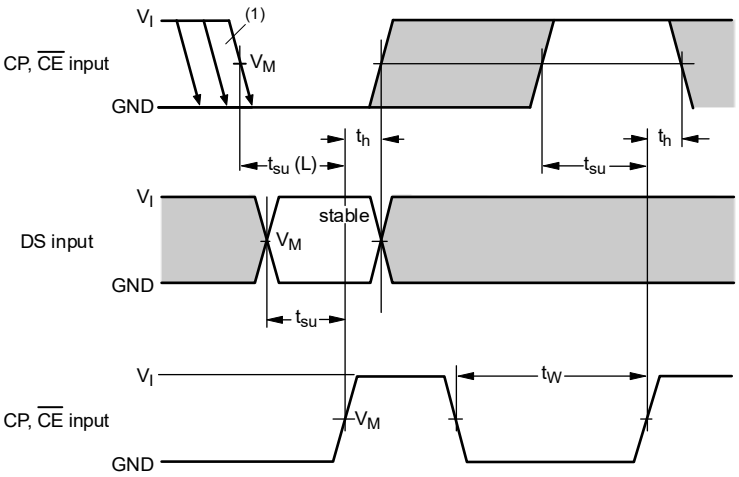


Figure 8-7 Data input (Dn) to output (Q7 or $\overline{Q7}$) propagation delays when PL is LOW



Note:

(1) CE may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 8-8. Set-up and hold times

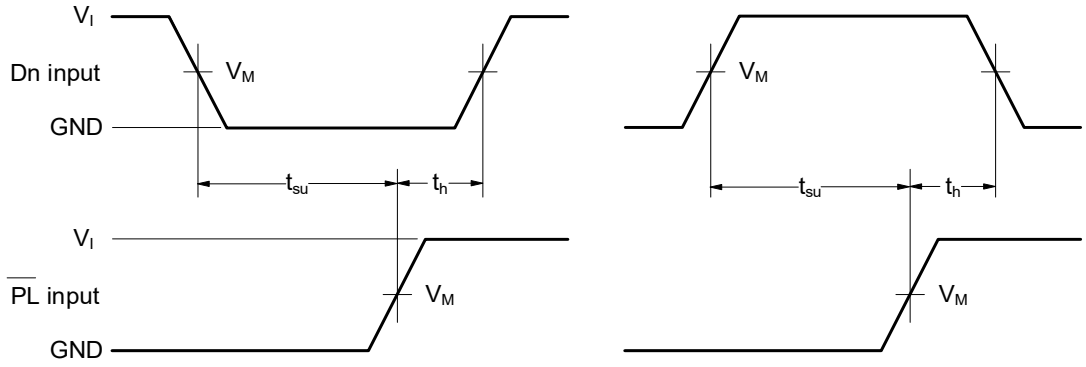


Figure 8-9. Set-up and hold times from the data inputs (Dn) to the parallel load input ($\overline{PL}$)

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{CC}	**V_M**	**V_M**
<2.7V	0.5xV_{CC}	0.5xV_{CC}
2.7V to 3.6V	1.5V	1.5V
≥4.5V	0.5xV_{CC}	0.5xV_{CC}

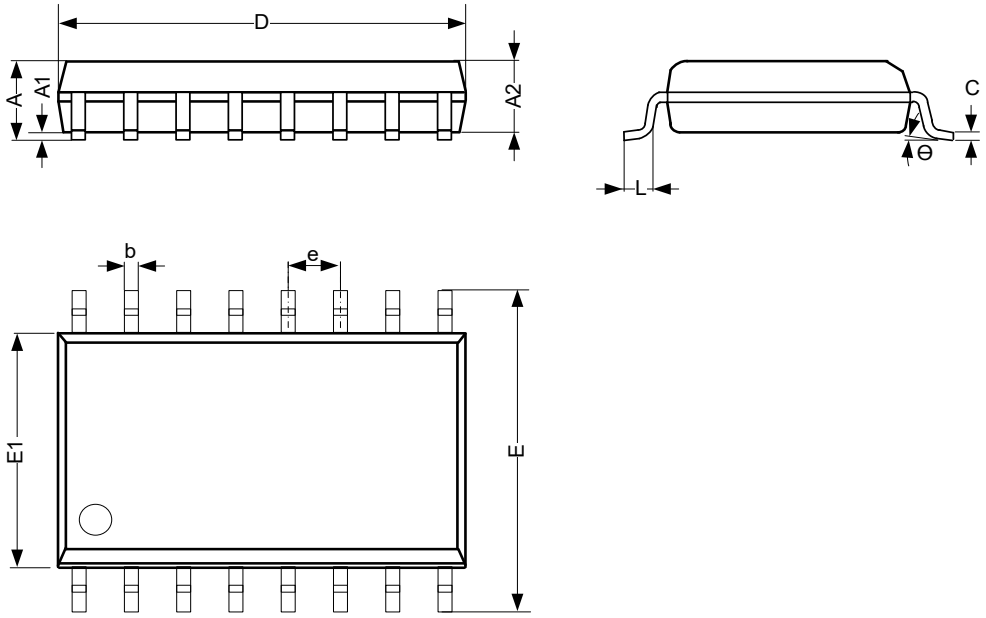
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD		TEST
V_{CC}	**V_I**	**t_r, t_f**	**C_L**	**R_L**	**t_{PHL}, t_{PLH}**
<2.7V	V_{CC}	≤3.0ns	50pF	1kΩ	Open
2.7V to 3.6V	2.7V	≤3.0ns	50pF, 15pF	1kΩ	Open
≥4.5V	V_{CC}	≤3.0ns	50pF	1kΩ	Open

9 Mechanical Information

9.1 SOP16 Mechanical Information

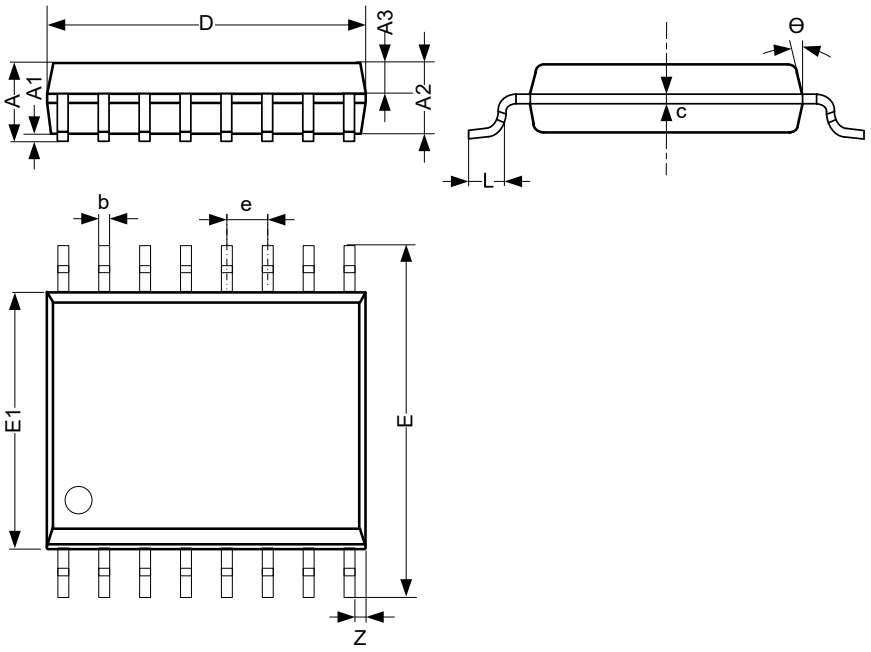
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 SSOP16 Mechanical Information

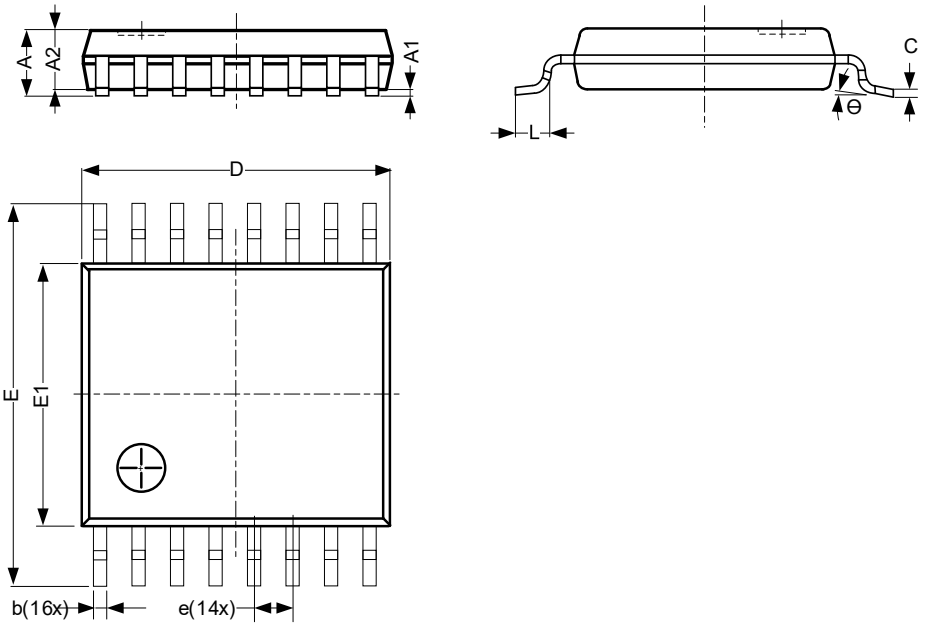
9.2.1 SSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.75	-	1.95
A1	0.05	-	0.15
A2	1.70	-	1.80
A3	-	0.80	-
b	-	0.30	-
c	-	0.15	-
D	6.15	-	6.25
E	7.65	-	7.95
E1	5.25	-	5.35
e	0.65 BSC		
L	0.60	-	0.80
Z	-	0.675	-
Θ	0°	-	8°
Unit: mm			

9.3 TSSOP16 Mechanical Information

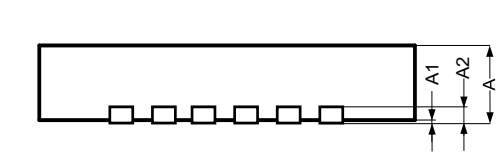
9.3.1 TSSOP16 Outline Dimensions



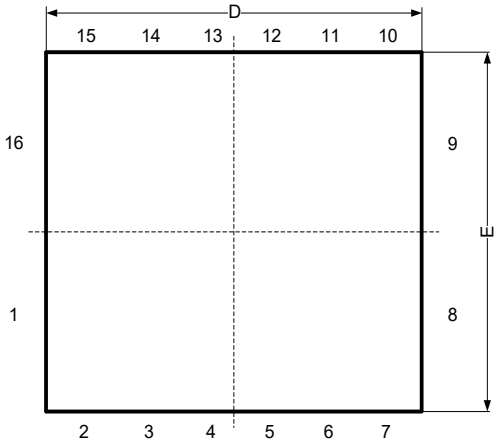
SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

9.4 QFN4x3.5-16L Mechanical Information

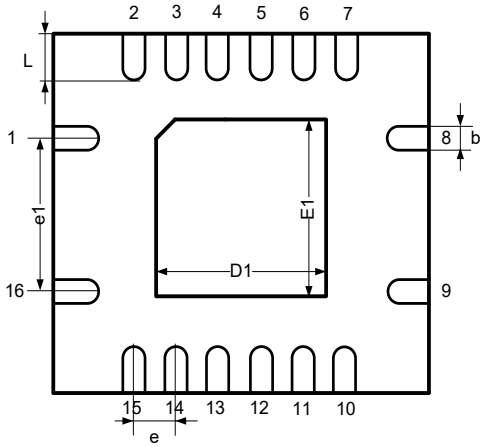
9.4.1 QFN4x3.5-16L Outline Dimensions



SIDE VIEW



TOP VIEW



BOTTOM VIEW

SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	0.75	-
A1	-	0.05	-
A2	-	0.203	-
b	0.215	-	0.265
D	-	4.00	-
D1	2.525	-	2.575
E	-	3.50	-
E1	2.025	-	2.075
e	0.475	-	0.525
e1	1.475	-	1.525
L	-	0.40	-
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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