16-bit Dual Supply Translating Transceiver; 3-state

CJ74LVC/LVCH16T245 Logic

1 Introduction

The CJ74LVC/LVCH16T245 are 16-bit dual supply translating transceivers with 3-state outputs that enable bidirectional level translation.The device can be used as two 8-bit transceivers or as a 16-bit transceiver.It has dual supplies ($V_{CC(A)}$ and $V_{CC(B)}$) for voltage translation and four 8-bit input-output ports (nAn and nBn) each with its own output enable (/nOE) and send/receive (nDIR) input for direction control.Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2V and 5.5V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V). Pins nAn, /nOE and nDIR are referenced to $V_{CC(A)}$ and pins nBn are referenced to $V_{CC(B)}$. A HIGH on nDIR allows transmission from nAn to nBn and a LOW on nDIR allows transmission from nBn to nAn. The output enable input (/nOE) can be used to disable the outputs so the buses are effectively isolated.

The devices are fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both nAn port and nBn port are in the high-impedance OFF-state.

Active bus hold circuitry in the CJ74LVCH16T245 holds unused or floating data inputs at a valid logic level.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LVC16T245	SSOP48
	TSSOP48
CJ74LVCH16T245	SSOP48
	TSSOP48

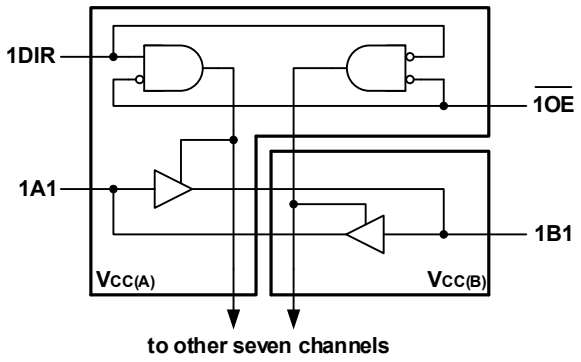
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range:
  $V_{CC(A)}$: 1.2V to 5.5V
  $V_{CC(B)}$: 1.2V to 5.5V
- Suspend mode
- ±24mA output drive (V_{CC}=3.0V)
- Inputs accept voltages up to 5.5V
- Low power consumption: 30uA maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from -40°C to +125°C

4 Applications

- Personal electronic
- Industrial
- Enterprise
- Telecom



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LVC16T245SNN	SSOP48	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 1000 Units/Reel	Active
CJ74LVCH16T245SNN	SSOP48	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 1000 Units/Reel	Active
CJ74LVC16T245BNN	TSSOP48	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units/Reel	Active
CJ74LVCH16T245BNN	TSSOP48	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

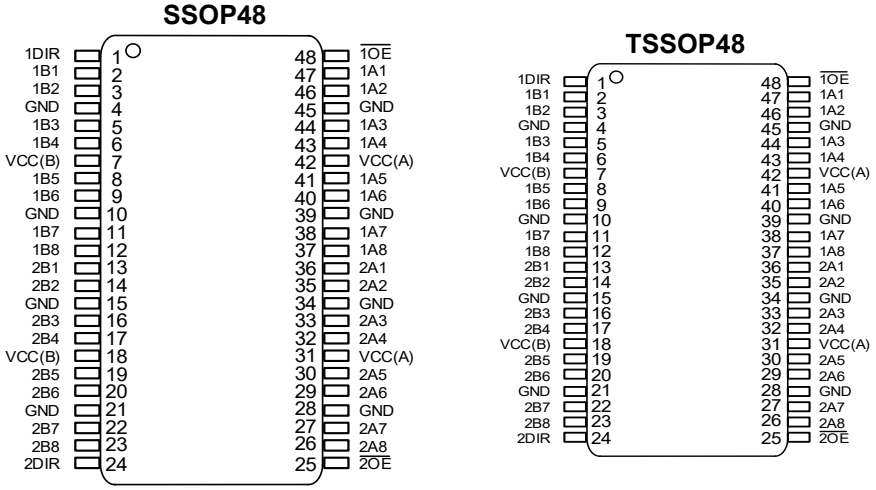


Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1,24	1DIR, 2DIR	-	Direction control
2,3,5,6,8,9,11,12	1B1,1B2,1B3,1B4,1B5,1B6,1B7,1B8	I/O	Data input or output
13,14,16,17,19,20,22, 23	2B1,2B2,2B3,2B4,2B5,2B6,2B7,2B8	I/O	Data input or output
4,10,15,21,28,34,39,45	GND(2)	G	Ground (0V)
7,18	VCC(B)	P	Supply voltage B (nBn inputs/outputs are referenced to VCC(B))
48,25	$\overline{1OE}$,$\overline{2OE}$	I	Output enable input (active LOW)
47,46,44,43,41,40,38,37	1A1,1A2,1A3,1A4,1A5,1A6,1A7,1A8	I/O	Data input or output
36,35,33,32,30,29,27,26	2A1,2A2,2A3,2A4,2A5,2A6,2A7,2A8	I/O	Data input or output
31,42	VCC(A)	P	Supply voltage A (nAn inputs/outputs, $\overline{nOE}$ and nDIR inputs are referenced to VCC(A))

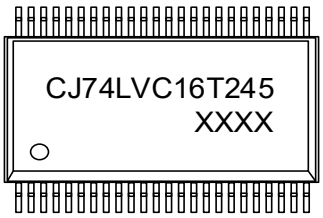
(1) I-Input, O-Output, P-Power, G-Ground.

(2) All GND pins must be connected to ground (0V).

6.3 Marking Information

6.3.1 CJ74LVC16T245

SSOP48



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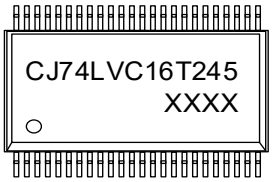

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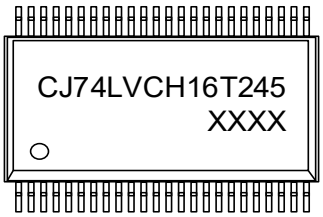
6.3.2 CJ74LVCH16T245

SSOP48



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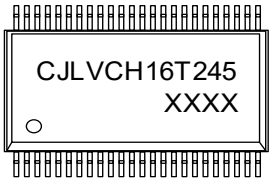

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7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND(ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-	-0.5	+6.5	V
$V_{CC(B)}$	Supply voltage B	-	-0.5	+6.5	V
I_{IK}	Input clamping current	V_I<0V	-50	-	mA
V_I	Input voltage	-(1)	-0.5	+6.5	V
I_{OK}	Output clamping current	V_O<0V	-50	-	mA
V_O	Output voltage	Active mode(1)(2)(3)	-0.5	V_{CCO}+0.5	V
		Suspend or 3-state mode(1)	-0.5	+6.5	V
I_O	Output current	V_O=0V to V_{CCO}(2)	-	±50	mA
I_{CC}	Supply current	$I_{CC(A)}$ or $I_{CC(B)}$; Per V_{CC} pin	-	100	mA
I_{GND}	Ground current	Per GND pin	-100	-	mA
T_{stg}	Storage temperature	-	-65	+150	°C
P_{tot}	Total power dissipation	-	-	500	mW
T_L	Soldering temperature	10s	-	260	°C

(1) The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

(2) V_{CCO} is the supply voltage associated with the output port.

(3) V_{CCO}+0.5V should not exceed 6.5V.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-	1.2	-	5.5	V
$V_{CC(B)}$	Supply voltage B	-	1.2	-	5.5	V
V_I	Input voltage	-	0	-	5.5	V
V_O	Output voltage	Active mode(1)	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	5.5	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
Δt/ΔV	Input transition rise and fall rate	V_{CCI}=1.2V(2)	-	-	20	ns/V
		V_{CCI}=1.4V to 1.95V	-	-	20	ns/V
		V_{CCI}=2.3V to 2.7V	-	-	20	ns/V
		V_{CCI}=3.0V to 3.6V	-	-	10	ns/V
		V_{CCI}=4.5V to 5.5V	-	-	5	ns/V

(1) V_{CCO} is the supply voltage associated with the output port.

(2) V_{CCI} is the supply voltage associated with the input port.

7.3 Electrical Characteristics

7.3.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}(1)	I_O=-3mA; V_{CCO}=1.2V	-	1.09	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=3mA; V_{CCO}=1.2V(1)	-	0.07	-	V
I_I	Input leakage current	nDIR, $\overline{nOE}$ input; V_I=0V to 5.5V; V_{CCI}=1.2V to 5.5V(2)		-	-	±1	uA
I_{BHL}	Bus hold LOW current	A or B port; V_I=0.42V; V_{CCI}=1.2V(2)		-	19	-	uA
I_{BHH}	Bus hold HIGH current	A or B port; V_I=0.78V; V_{CCI}=1.2V(2)		-	-19	-	uA
I_{BHLO}	Bus hold LOW overdrive current	A or B port; V_{CCI}=1.2V(2)(3)		-	19	-	uA
I_{BHHO}	Bus hold HIGH overdrive current	A or B port; V_{CCI}=1.2V(2)(3)		-	-19	-	uA
I_{OZ}	OFF-state output current	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V(1)		-	-	±1	uA
		Suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V(1)		-	-	±1	uA
		Suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V(1)		-	-	±1	uA
I_{OFF}	Power-off leakage current	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±1	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±1	uA
C_I	Input capacitance	nDIR, $\overline{nOE}$ input; V_I=0V or 3.3V; $V_{CC(A)}$=3.3V		-	3	-	pF
$C_{I/O}$	Input/output capacitance	A and B port; V_O=3.3V or 0V; $V_{CC(A)}$ =$V_{CC(B)}$=3.3V		-	6.5	-	pF

(1) V_{CCO} is the supply voltage associated with the output port.

(2) V_{CCI} is the supply voltage associated with the data input port.

(3) To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

7.3.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	Data input(1)	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		nDIR, $\overline{nOE}$ input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IL}	LOW-level input voltage	Data input(1)	V_{CCI}=1.2V	-	-	$0.2V_{CCI}$	V
			V_{CCI}=1.4V to 1.95V	-	-	$0.35V_{CCI}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	$0.3V_{CCI}$	V
		nDIR, $\overline{nOE}$ input	V_{CCI}=1.2V	-	-	$0.2V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	$0.35V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	$0.3V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH}	I_O=-100uA; V_{CCO}=1.2V to 4.5V(2)	V_{CCO}-0.1	-	-	V
			I_O=-6mA; V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA; V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA; V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA; V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA; V_{CCO}=4.5V	3.8	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IL}(2)	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V
			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
I_I	Input leakage current	nDIR, $\overline{nOE}$ input;V_I=0V or 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±2	uA
I_{BHL}	Bus hold LOW current	A or B port(1)	V_I=0.49V; V_{CCI}=1.4V	15	-	-	uA
			V_I=0.58V; V_{CCI}=1.65V	25	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	100	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
I_{BHH}	Bus hold HIGH current	A or B port(1)	V_I=0.91V; V_{CCI}=1.4V	-15	-	-	uA
			V_I=1.07V; V_{CCI}=1.65V	-25	-	-	uA
			V_I=1.70V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-100	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{BHLO}	Bus hold LOW overdrive current	A or B port(1)(3)	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
I_{BHHO}	Bus hold HIGH overdrive current	A or B port(1)(3)	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
I_{OZ}	OFF-state output current	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V(2)		-	-	±2	uA
		Suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V(2)		-	-	±2	uA
		Suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V(2)		-	-	±2	uA
I_{OFF}	Power-off leakage current	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±2	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±2	uA
I_{CC}	Supply current	A port; V_I=0V or V_{CCI}; I_O=0A(1)	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	15	uA
			$V_{CC(A)}$=5.5V;$V_{CC(B)}$=0V	-	-	15	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=5.5V	-2	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	15	uA
			$V_{CC(B)}$=0V;$V_{CC(A)}$=5.5V	-2	-	-	uA
			$V_{CC(B)}$=5.5V;$V_{CC(A)}$=0V	-	-	15	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A; V_I=0V or V_{CCI}	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	25	uA
ΔI_{CC}	Additional supply current	Per input; $V_{CC(A)}$,$V_{CC(B)}$ = 3.0V to 5.5V	nDIR and $\overline{nOE}$ input; nDIR or $\overline{nOE}$ Input at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	50	uA
			A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open(4)	-	-	50	uA
			B port; B port at $V_{CC(B)}$-0.6V; nDIR at GND; A port=open(4)	-	-	50	uA

(1) V_{CCI} is the supply voltage associated with the data input port.

(2) V_{CCO} is the supply voltage associated with the output port.

(3) To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

(4) For non bus hold parts only (CJ74LVC16T245).

7.3.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	Data input(1)	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		nDIR, $\overline{nOE}$ input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
V_{IL}	LOW-level input voltage	Data input(1)	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		nDIR, $\overline{nOE}$ input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3$V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH}	I_O=-100uA; V_{CCO}=1.2V to 4.5V(2)	V_{CCO}-0.1	-	-	V
			I_O=-6mA; V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA; V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA; V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA; V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA; V_{CCO}=4.5V	3.8	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IL}(2)	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V
			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
I_I	Input leakage current	nDIR, $\overline{nOE}$ input;V_I=0V or 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±10	uA

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{BHL}	Bus hold LOW current	A or B port(1)	V_I=0.49V; V_{CCI}=1.4V	10	-	-	uA
			V_I=0.58V; V_{CCI}=1.65V	20	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	80	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
I_{BHH}	Bus hold HIGH current	A or B port(1)	V_I=0.91V; V_{CCI}=1.4V	-10	-	-	uA
			V_I=1.07V; V_{CCI}=1.65V	-20	-	-	uA
			V_I=1.70V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-80	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA
I_{BHLO}	Bus hold LOW overdrive current	A or B port(1)(3)	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
I_{BHHO}	Bus hold HIGH overdrive current	A or B port(1)(3)	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
I_{OZ}	OFF-state output current	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V(2)		-	-	±10	uA
		Suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V(2)		-	-	±10	uA
		Suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V(2)		-	-	±10	uA
I_{OFF}	Power-off leakage current	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±10	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±10	uA
I_{CC}	Supply current	A port; V_I=0V or V_{CCI}; I_O=0A(1)	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	20	uA
			$V_{CC(A)}$=5.5V;$V_{CC(B)}$=0V	-	-	20	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=5.5V	-4	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	20	uA
			$V_{CC(B)}$=0V;$V_{CC(A)}$=5.5V	-4	-	-	uA
			$V_{CC(B)}$=5.5V;$V_{CC(A)}$=0V	-	-	20	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A; V_I=0V or V_{CCI}	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	30	uA

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
ΔI_{CC}	Additional supply current	Per input; $V_{CC(A)}$,$V_{CC(B)}$ = 3.0V to 5.5V	nDIR and $\overline{nOE}$ input; nDIR or $\overline{nOE}$ Input at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	75	uA
			A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open(4)	-	-	75	uA
			B port; B port at $V_{CC(B)}$-0.6V; nDIR at GND; A port=open(4)	-	-	75	uA

(1) V_{CCI} is the supply voltage associated with the data input port.

(2) V_{CCO} is the supply voltage associated with the output port.

(3) To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

(4) For non bus hold parts only (CJ74LVC16T245).

7.3.4 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$										UNIT
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$V_{CC(A)}$=1.5V±0.1V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	17.6	-	15.3	-	13.1	-	12.5	-	12.5	ns
		nBn to nAn	-	17.5	-	16.3	-	15.2	-	14.4	-	13.8	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	29.1	-	29.1	-	29.1	-	29.1	-	29.1	ns
		$\overline{nOE}$ to nBn	-	36.4	-	34.5	-	17.3	-	15.5	-	13.6	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	33.6	-	33.6	-	33.6	-	33.6	-	33.6	ns
		$\overline{nOE}$ to nBn	-	37.3	-	35.5	-	18.2	-	15.5	-	14.5	ns
$V_{CC(A)}$=1.8V±0.15V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	16.4	-	13.1	-	11.1	-	10.1	-	10.0	ns
		nBn to nAn	-	15.2	-	12.7	-	11.4	-	10.6	-	10.1	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	29.1	-	28.9	-	28.7	-	28.5	-	28.4	ns
		$\overline{nOE}$ to nBn	-	36.4	-	32.9	-	15.5	-	14.5	-	13.0	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	24.5	-	24.5	-	24.4	-	24.3	-	24.3	ns
		$\overline{nOE}$ to nBn	-	35.5	-	34.5	-	18.2	-	14.2	-	13.5	ns

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$										UNIT
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$V_{CC(A)}$=2.5V±0.2V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	15.3	-	11.9	-	9.2	-	8.2	-	7.6	ns
		nBn to nAn	-	13.0	-	10.6	-	8.9	-	7.9	-	7.1	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	10.9	-	10.9	-	10.9	-	10.9	-	10.9	ns
		$\overline{nOE}$ to nBn	-	33.6	-	30.5	-	13.6	-	13.0	-	9.9	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	15.5	-	15.5	-	15.5	-	15.5	-	15.5	ns
		$\overline{nOE}$ to nBn	-	33.6	-	29.5	-	15.9	-	12.3	-	10.0	ns
$V_{CC(A)}$=3.3V±0.3V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	14.6	-	11.2	-	8.1	-	7.0	-	6.5	ns
		nBn to nAn	-	12.3	-	9.8	-	7.9	-	6.8	-	6.0	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	10.9	-	10.9	-	10.9	-	10.9	-	10.9	ns
		$\overline{nOE}$ to nBn	-	30.9	-	28.2	-	13.2	-	11.4	-	9.5	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	12.3	-	12.3	-	12.1	-	12.0	-	12.0	ns
		$\overline{nOE}$ to nBn	-	33.5	-	28.5	-	16.5	-	11.3	-	9.5	ns
$V_{CC(A)}$=5.0V±0.5V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	14.1	-	10.6	-	7.3	-	6.3	-	5.6	ns
		nBn to nAn	-	12.3	-	9.5	-	7.4	-	6.3	-	5.5	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	8.4	-	8.4	-	8.4	-	8.4	-	8.4	ns
		$\overline{nOE}$ to nBn	-	32.5	-	29.5	-	12.3	-	10.9	-	8.9	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	9.7	-	9.7	-	9.7	-	9.7	-	9.7	ns
		$\overline{nOE}$ to nBn	-	33.5	-	28.5	-	16.7	-	12.3	-	9.7	ns

7.3.5 AC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$										UNIT
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$V_{CC(A)}$=1.5V±0.1V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	19.4	-	16.8	-	14.4	-	13.8	-	13.8	ns
		nBn to nAn	-	19.2	-	17.9	-	16.7	-	15.8	-	15.2	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	32	-	32	-	32	-	32	-	32	ns
		$\overline{nOE}$ to nBn	-	40	-	38	-	19	-	17	-	15	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	37	-	37	-	37	-	37	-	37	ns
		$\overline{nOE}$ to nBn	-	41	-	39	-	20	-	17	-	16	ns

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$										UNIT
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$V_{CC(A)}$=1.8V±0.15V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	18	-	14.4	-	12.2	-	11.1	-	11	ns
		nBn to nAn	-	16.7	-	14	-	12.5	-	11.7	-	11.1	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	32	-	31.8	-	31.6	-	31.3	-	31.2	ns
		$\overline{nOE}$ to nBn	-	40	-	36.2	-	17.1	-	16.0	-	14.3	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	27	-	27	-	26.8	-	26.7	-	26.7	ns
		$\overline{nOE}$ to nBn	-	39	-	38	-	20	-	15.6	-	14.8	ns
$V_{CC(A)}$=2.5V±0.2V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	16.8	-	13.1	-	10.1	-	9	-	8.4	ns
		nBn to nAn	-	14.3	-	11.7	-	9.8	-	8.7	-	7.8	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	12	-	12	-	12	-	12	-	12	ns
		$\overline{nOE}$ to nBn	-	37	-	33.6	-	15	-	14.3	-	10.9	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	17	-	17	-	17	-	17	-	17	ns
		$\overline{nOE}$ to nBn	-	37	-	32.5	-	17.5	-	13.5	-	11	ns
$V_{CC(A)}$=3.3V±0.3V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	16.1	-	12.3	-	8.9	-	7.7	-	7.2	ns
		nBn to nAn	-	13.5	-	10.8	-	8.7	-	7.5	-	6.6	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	12	-	12	-	12	-	12	-	12	ns
		$\overline{nOE}$ to nBn	-	34	-	31	-	14.5	-	12.5	-	10.4	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	13.5	-	13.5	-	13.3	-	13.2	-	13.2	ns
		$\overline{nOE}$ to nBn	-	36.8	-	31.4	-	18.1	-	12.4	-	10.5	ns
$V_{CC(A)}$=5.0V±0.5V													
t_{PLH}, t_{PHL}	Propagation Delay	nAn to nBn	-	15.5	-	11.7	-	8	-	6.9	-	6.2	ns
		nBn to nAn	-	13.5	-	10.5	-	8.1	-	6.9	-	6	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{nOE}$ to nAn	-	9.2	-	9.2	-	9.2	-	9.2	-	9.2	ns
		$\overline{nOE}$ to nBn	-	35.8	-	32.5	-	13.5	-	12	-	9.8	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{nOE}$ to nAn	-	10.7	-	10.7	-	10.7	-	10.7	-	10.7	ns
		$\overline{nOE}$ to nBn	-	36.8	-	31.4	-	18.4	-	13.5	-	10.7	ns

8 Detailed Description

8.1 Overview

The CJ74LVC/LVCH16T245 are 16-bit dual supply translating transceivers with 3-state outputs that enable bidirectional level translation.The device can be used as two 8-bit transceivers or as a 16-bit transceiver.It has dual supplies ($V_{CC(A)}$ and $V_{CC(B)}$) for voltage translation and four 8-bit input-output ports (nAn and nBn) each with its own output enable (/nOE) and send/receive (nDIR) input for direction control.Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2V and 5.5V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V). Pins nAn, /nOE and nDIR are referenced to $V_{CC(A)}$ and pins nBn are referenced to $V_{CC(B)}$. A HIGH on nDIR allows transmission from nAn to nBn and a LOW on nDIR allows transmission from nBn to nAn. The output enable input (/nOE) can be used to disable the outputs so the buses are effectively isolated.

The devices are fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both nAn port and nBn port are in the high-impedance OFF-state.

Active bus hold circuitry in the CJ74LVCH16T245 holds unused or floating data inputs at a valid logic level.

8.2 Functional Block Diagram

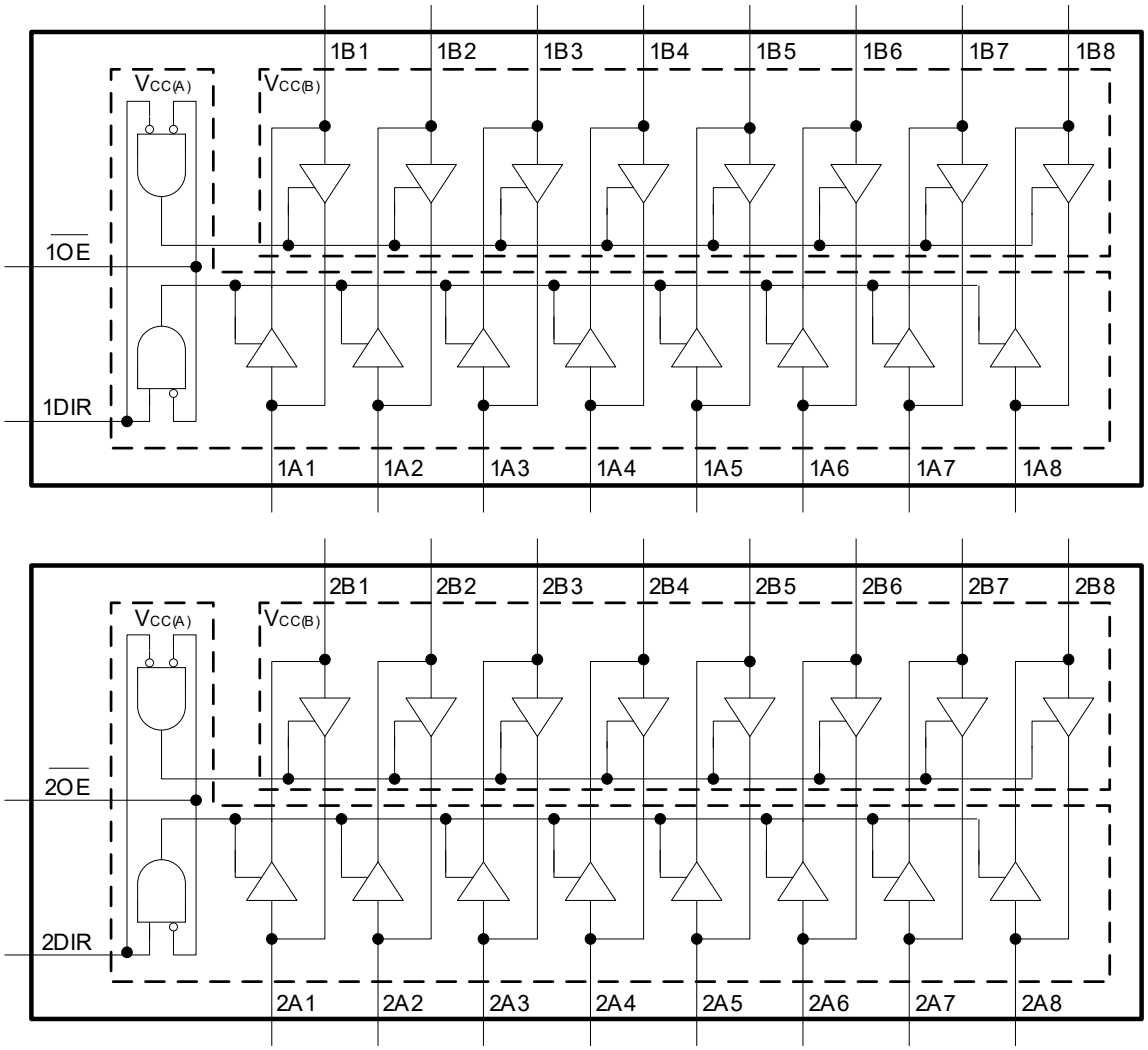


Figure 8-1 Logic symbol

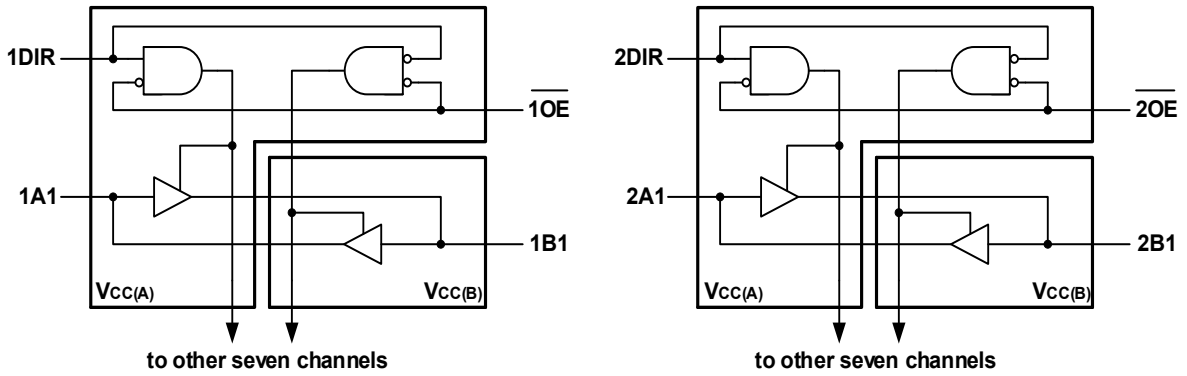


Figure 8-2 Logic diagram

8.3 Function Table

SUPPLY VOLTAGE	INPUT		INPUT/OUTPUT	
$V_{CC(A)}$, $V_{CC(B)}$	$\overline{nOE}$	nDIR	nAn	nBn
1.2V to 5.5V	L	L	nAn=nBn	input
1.2V to 5.5V	L	H	input	nBn=nAn
1.2V to 5.5V	H	X	Z	Z
GND	X	X	Z	Z

Note:

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

(2) The nAn inputs/outputs, nDIR and $\overline{nOE}$ input circuit is referenced to $V_{CC(A)}$; The nBn inputs/outputs circuit is referenced to $V_{CC(B)}$.

(3) If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

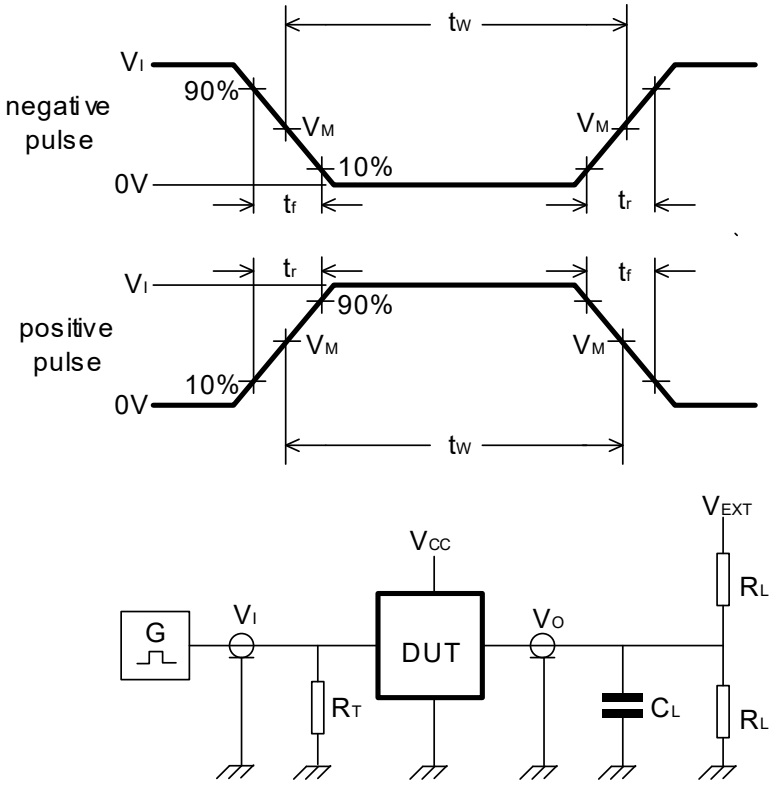


Figure 8-3 Load circuitry for switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance.

V_{EXT}=External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

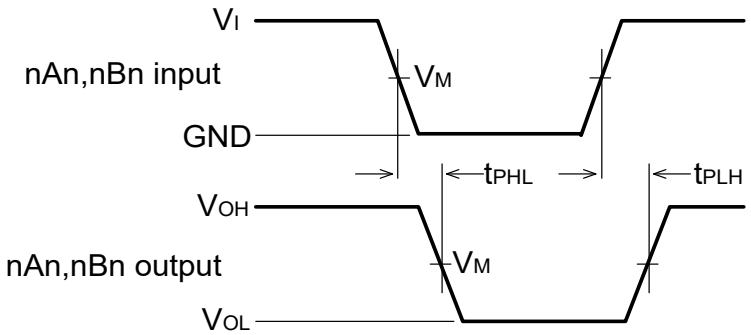


Figure 8-4 The data input (nAn, nBn) to output (nBn, nAn) propagation delay times (V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.)

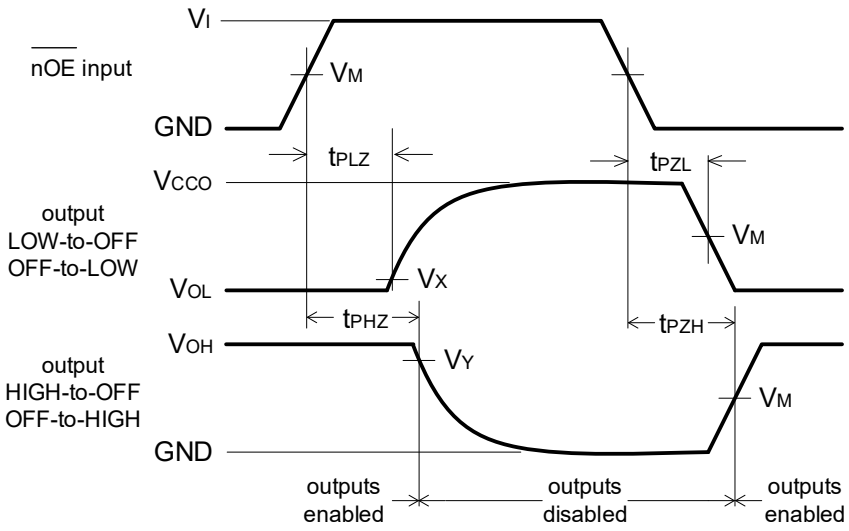


Figure 8-5 Enable and disable times
(V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.)

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT(1)	OUTPUT(2)		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.1V	V_{OH}-0.1V
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
3.0V to 5.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V

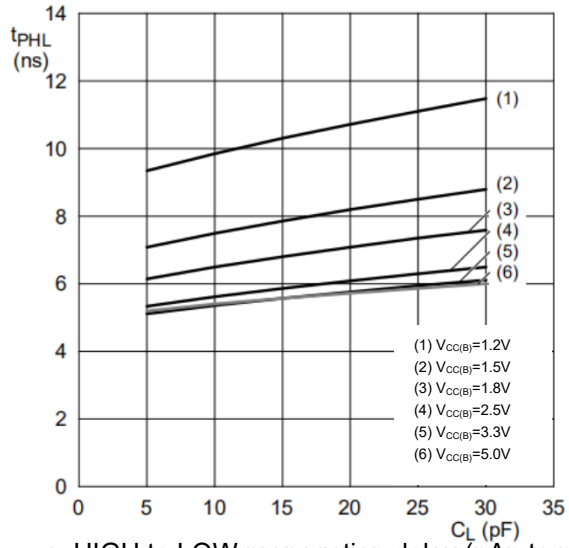
(1) V_{CCI} is the supply voltage associated with the data input port.
(2) V_{CCO} is the supply voltage associated with the output port.

8.4.4 Test Data

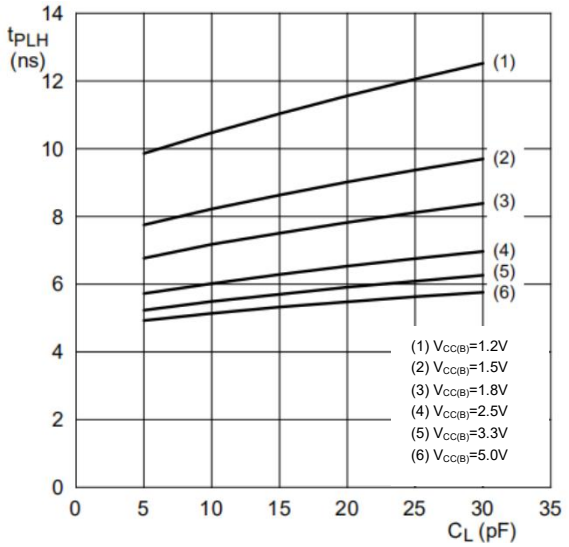
SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I(1)	$\Delta t/\Delta V$(2)	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}(3)
1.2V to 5.5V	V_{CCI}	≤1.0ns/V	15pF	2kΩ	Open	GND	$2V_{CCO}$

(1) V_{CCI} is the supply voltage associated with the data input port.
(2) dV/dt≥1.0V/ns.
(3) V_{CCO} is the supply voltage associated with the output port.

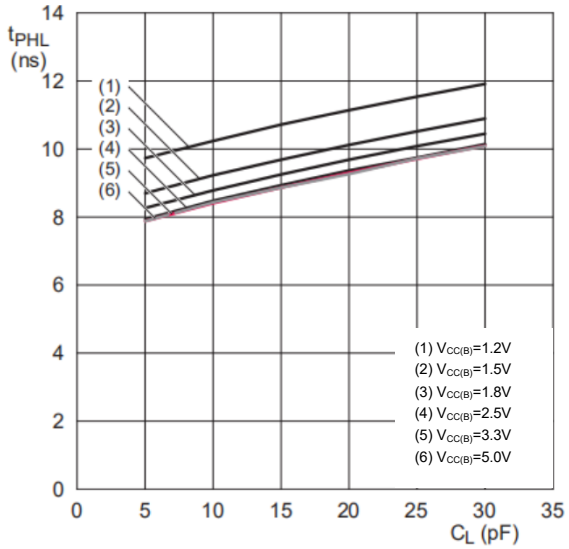
9 Characteristic Curve



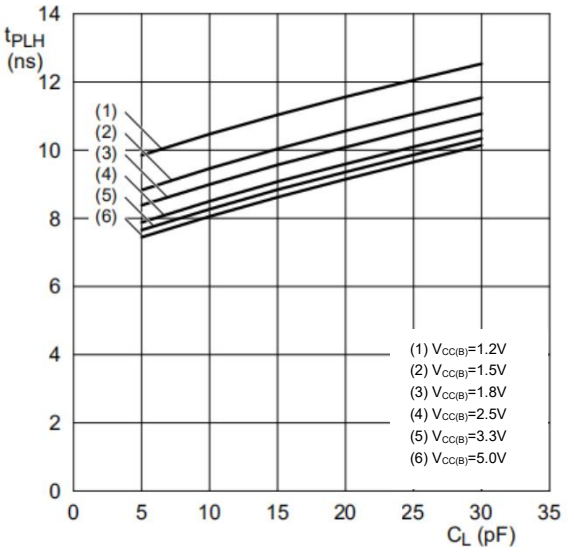
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)

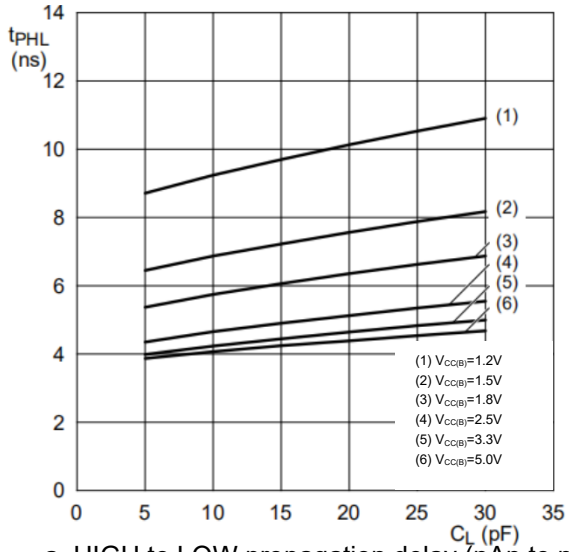


c. HIGH to LOW propagation delay (nBn to nAn)

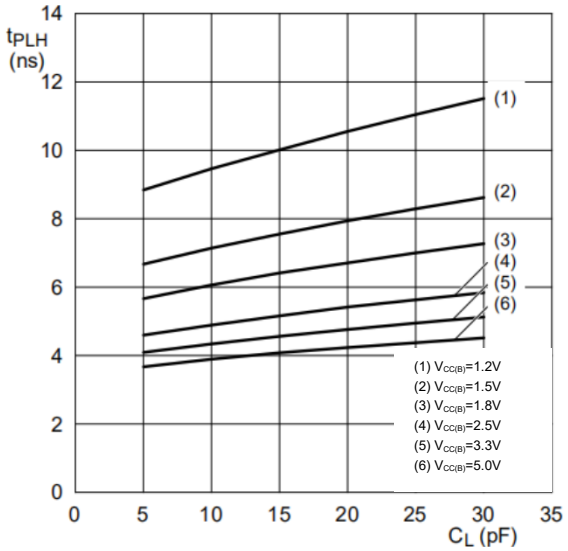


d. LOW to HIGH propagation delay (nBn to nAn)

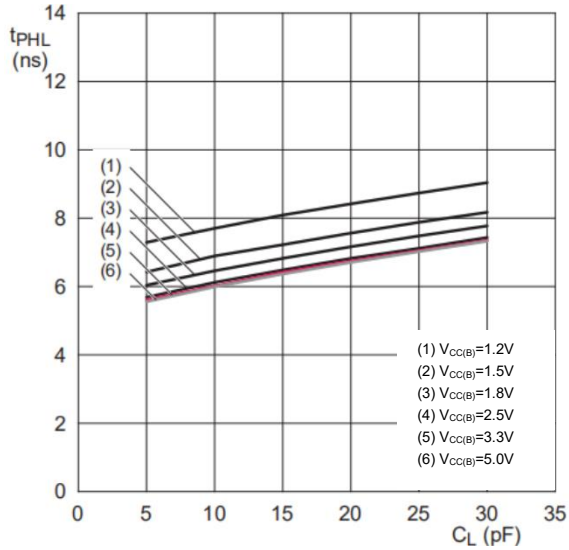
Figure 9-1 Typical propagation delay versus load capacitance; T_{amb}=25°C; $V_{CC(A)}$=1.2V



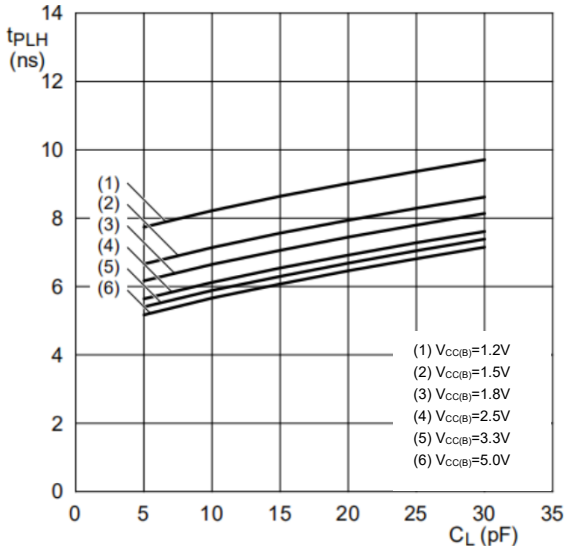
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)

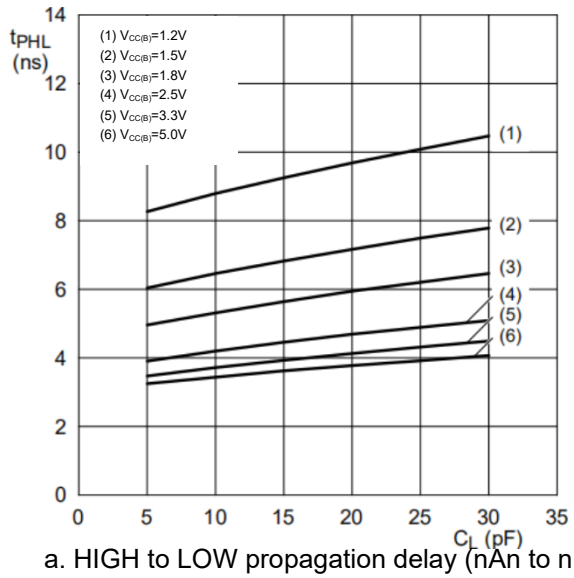


c. HIGH to LOW propagation delay (nBn to nAn)

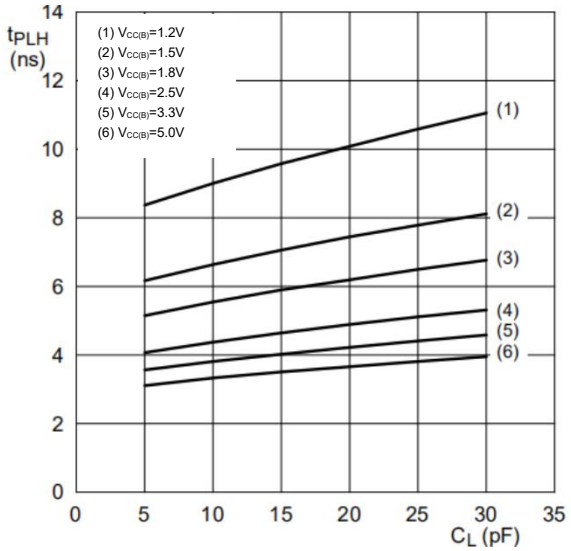


d. LOW to HIGH propagation delay (nBn to nAn)

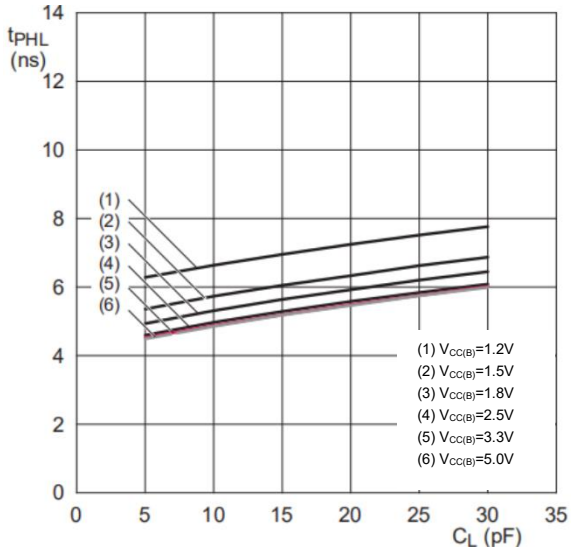
Figure 9-2 Typical propagation delay versus load capacitance; T_{amb}=25°C; $V_{CC(A)}$=1.5V



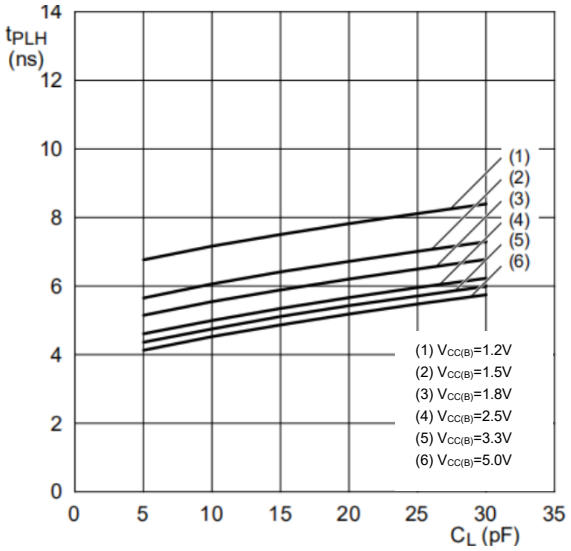
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)

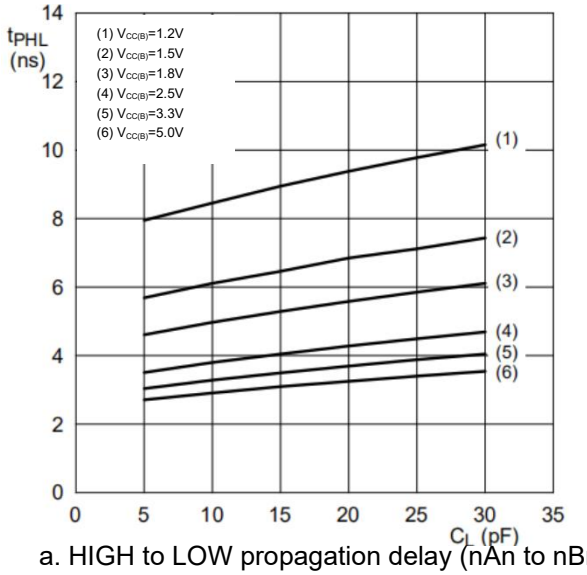


c. HIGH to LOW propagation delay (nBn to nAn)

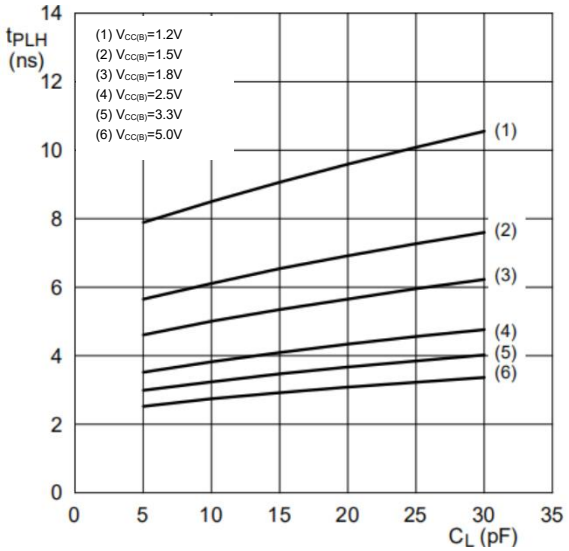


d. LOW to HIGH propagation delay (nBn to nAn)

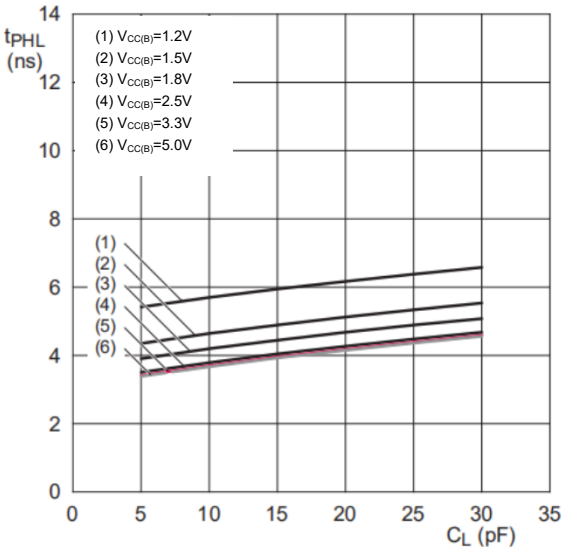
Figure 9-3 Typical propagation delay versus load capacitance; T_{amb}=25°C; $V_{CC(A)}$=1.8V



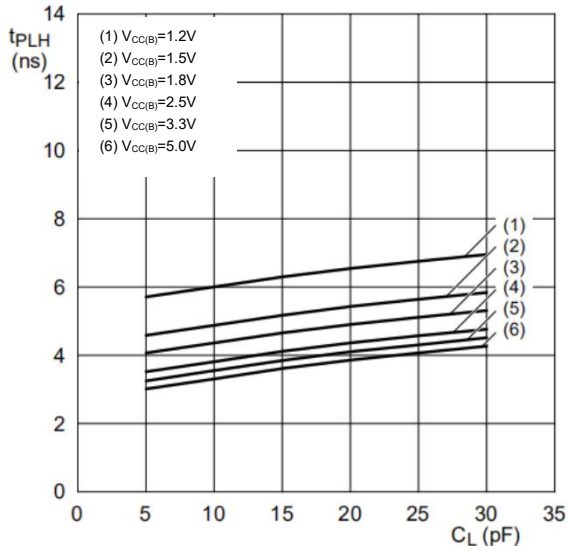
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)

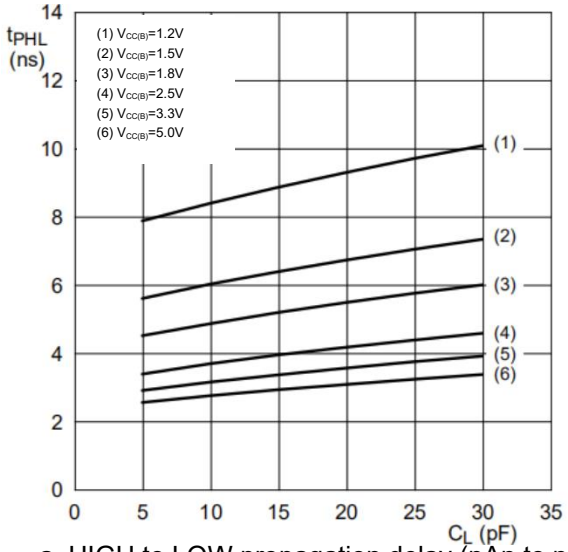


c. HIGH to LOW propagation delay (nBn to nAn)

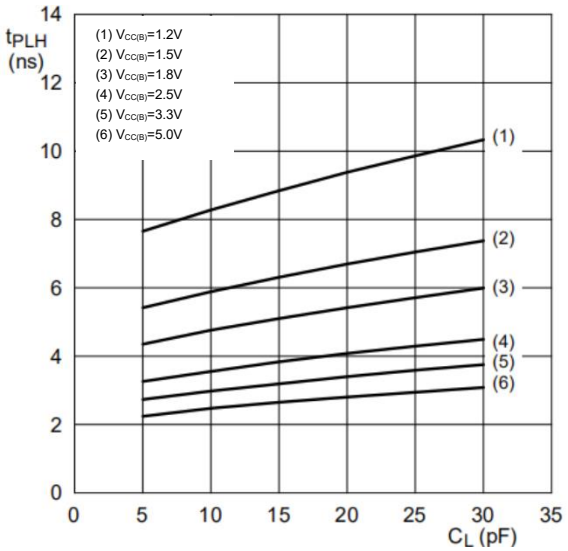


d. LOW to HIGH propagation delay (nBn to nAn)

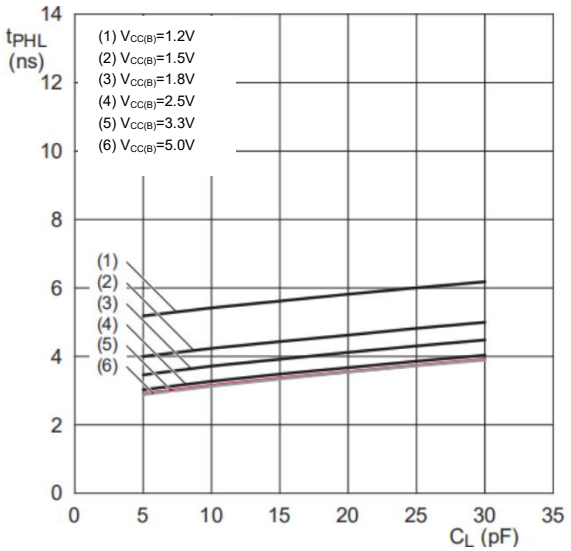
Figure 9-4 Typical propagation delay versus load capacitance; T_{amb}=25°C; $V_{CC(A)}$=2.5V



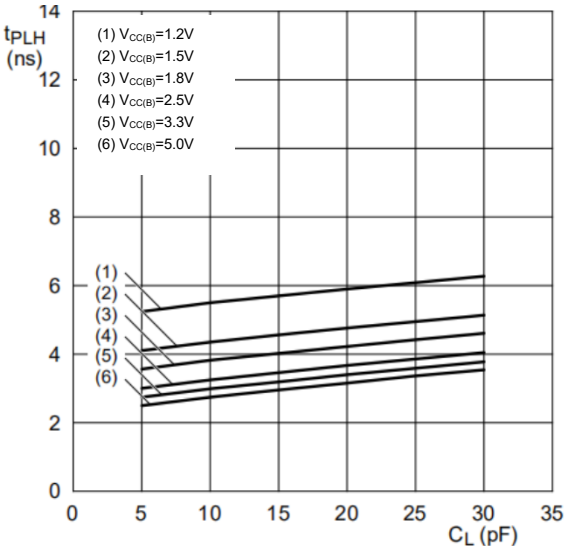
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)

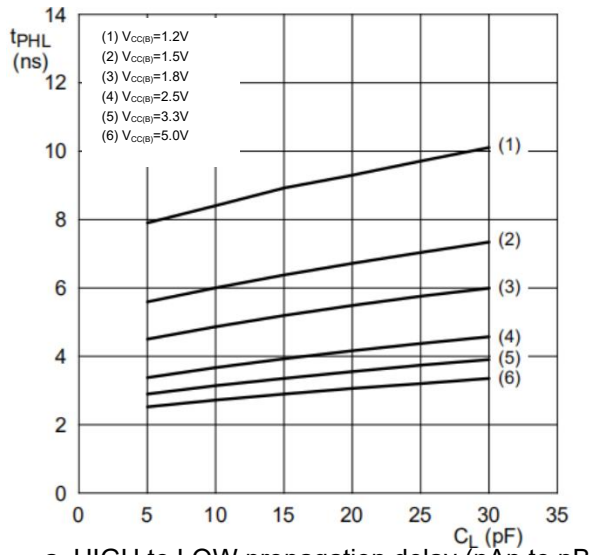


c. HIGH to LOW propagation delay (nBn to nAn)

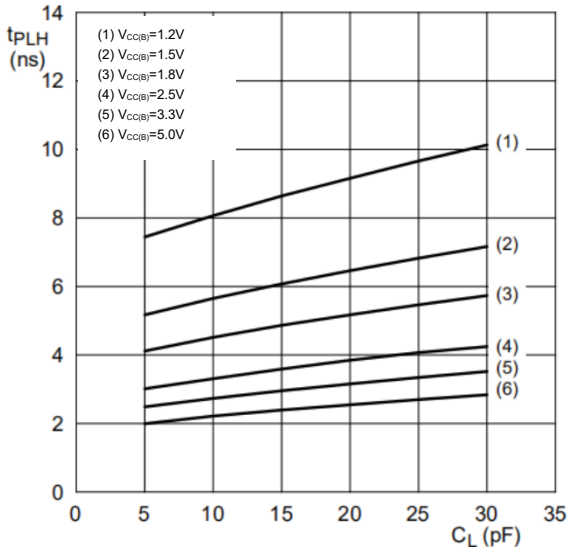


d. LOW to HIGH propagation delay (nBn to nAn)

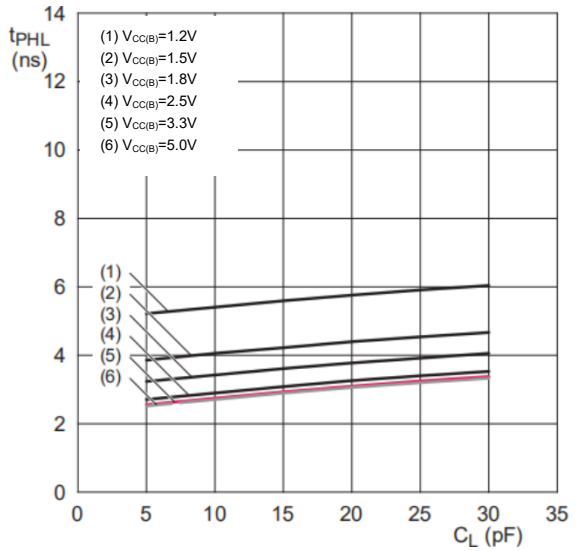
Figure 9-5 Typical propagation delay versus load capacitance; T_{amb}=25°C; $V_{CC(A)}$=3.3V



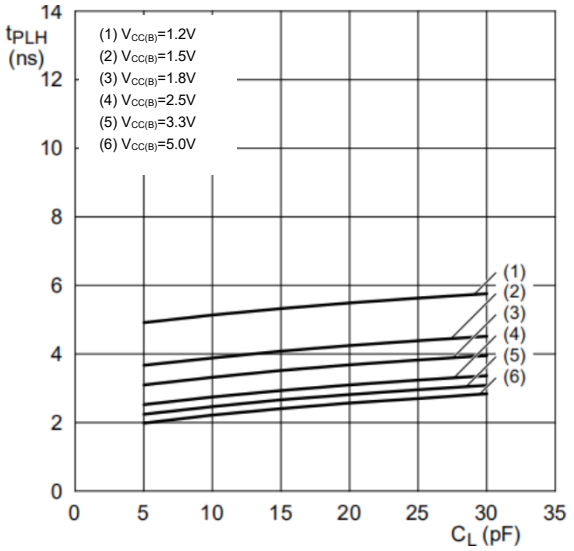
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



c. HIGH to LOW propagation delay (nBn to nAn)



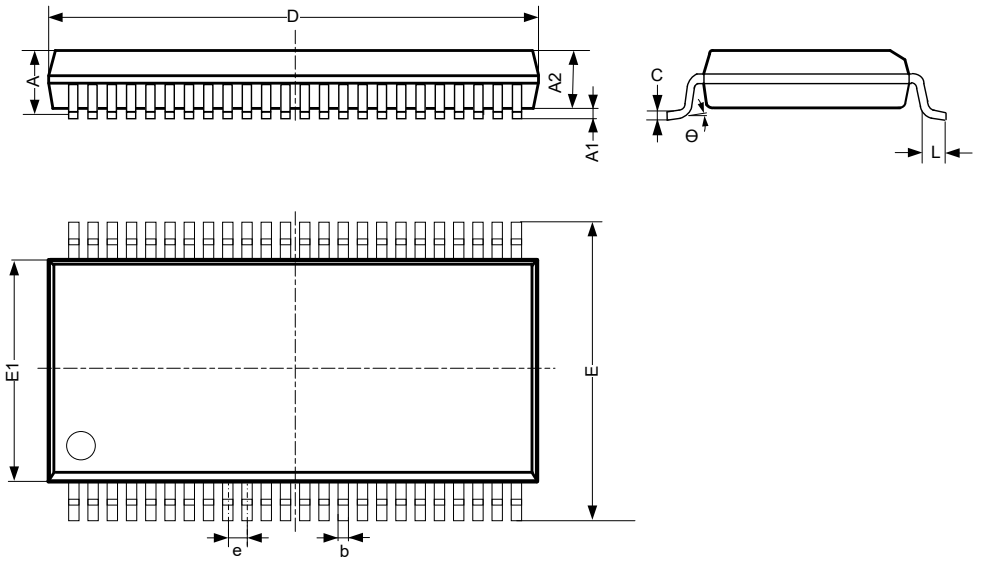
d. LOW to HIGH propagation delay (nBn to nAn)

Figure 9-6 Typical propagation delay versus load capacitance; T_{amb}=25°C; $V_{CC(A)}$=5.0V

10 Mechanical Information

10.1 SSOP48 Mechanical Information

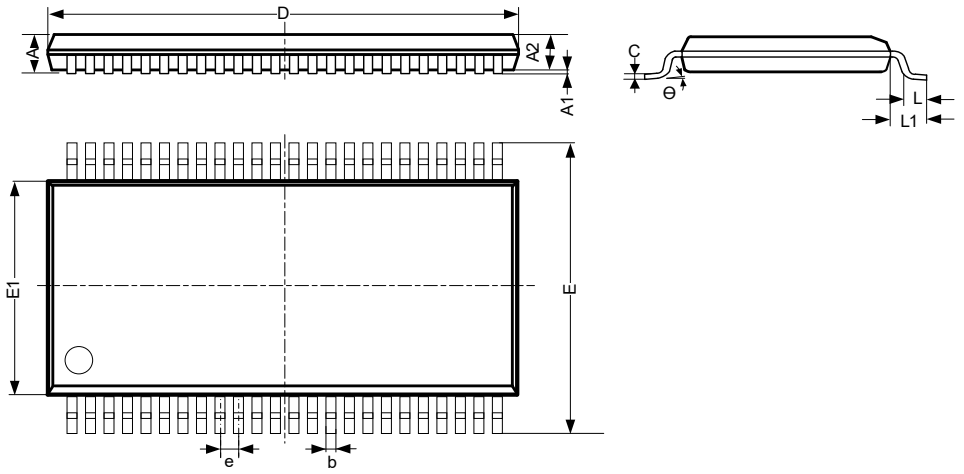
10.1.1 SSOP48 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	2.85
A1	0.15	-	0.45
A2	2.10	-	2.45
b	0.20	-	0.35
c	0.12	-	0.25
D	15.60	-	16.05
E	9.80	-	10.80
E1	7.35	-	7.65
e	0.635 BSC		
L	0.56	-	0.95
Θ	0°	-	8°
Unit: mm			

10.2 TSSOP48 Mechanical Information

10.2.1 TSSOP48 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.03	-	0.15
A2	0.82	-	1.05
b	0.17	-	0.27
c	0.12	-	0.22
D	12.40	-	12.60
E	7.90	-	8.30
E1	6.00	-	6.20
e	0.50 BSC		
L	0.35	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

11 Notes and Revision History

11.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

11.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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