Triple 2-channel Analog Multiplexer/Demultiplexer

CJ74LVC1G175 Logic

1 Introduction

The CJ74LVC1G175 is a low-power, low-voltage single positive edge triggered D-type flip-flop with individual data (D) input, clock (CP) input, master reset (/MR) input, and Q output.

The input can be driven from either 3.3V or 5V devices. This feature allows the use of this device in a mixed 3.3V and 5V environment.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LVC1G175	SOT-23-6L
	SOT-363

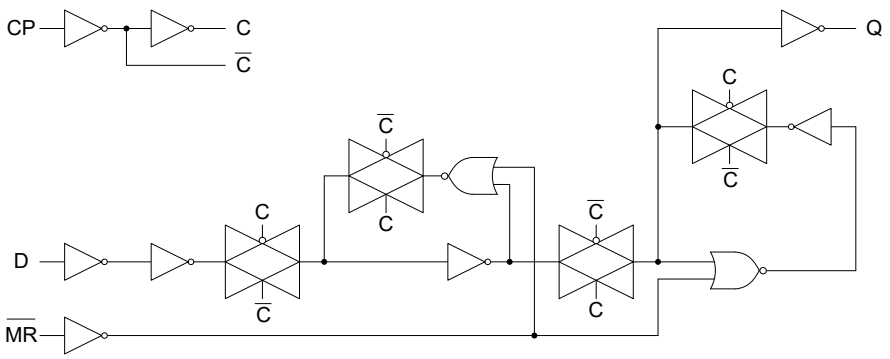
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 1.65V to 5.5V
- Inputs accept voltages to 5.5 V
- ±24mA output drive at 3.0V
- High-impedance when V_{CC}=0V
- Temperature range: -40°C to +125°C

4 Applications

- TV/Set Top Box/Audio
- EPOS(Electronic Point-of-Sale)
- Motor Drives
- PC/Notebook
- Servers
- Factory Automation and Control
- Tablets
- Medical Healthcare and Fitness
- Smart Grid
- Telecom Infrastructure
- Enterprise Switching
- Projectors
- Storage



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LVC1G175M6N	SOT-23-6L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active
CJ74LVC1G175R6N	SOT-363	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

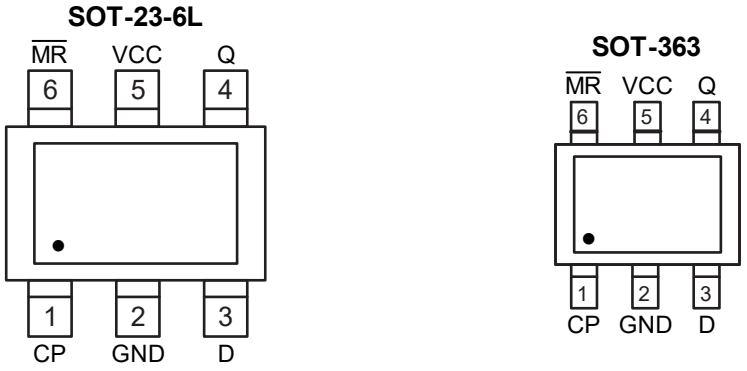


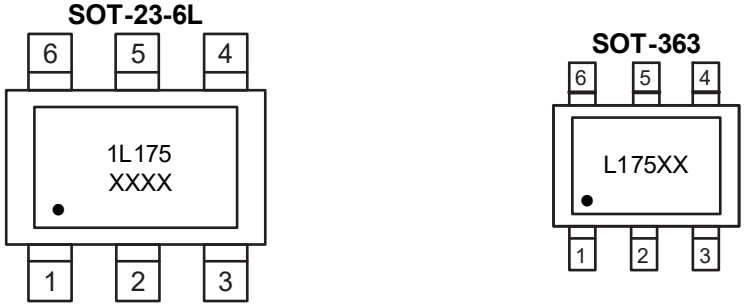
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	CP	I	Clock input (LOW-to-HIGH, edge-triggered)
2	GND	G	Ground (0V)
3	D	I	Data input
4	Q	O	Data output
5	VCC	P	Supply voltage
6	$\overline{MR}$	I	Master reset input (active LOW)

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX or XX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-	-0.5	+6.5	V
V_I	Input voltage	-	-0.5	+6.5	V
V_O	Output voltage	Active mode	-0.5	V_{CC}+0.5	V
		Power-down mode; V_{CC}=0V	-0.5	+6.5	V
I_{CC}	Supply current	-	-	100	mA
I_{GND}	Ground current	-	-100	-	mA
I_{IK}	Input clamping current	V_I < 0V	-50	-	mA
I_O	Output current	V_O=0V to V_{CC}	-	±50	mA
I_{OK}	Output clamping current	V_O > V_{CC} or V_O < 0V	-	±50	mA
T_{stg}	Storage temperature	-	-65	+150	°C
T_L	Soldering temperature	10s	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	-	1.65	-	5.5	V
V_I	Input voltage	-	0	-	5.5	V
V_O	Output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC}=0V	0	-	5.5	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 Electrical Characteristics

7.3.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground = 0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=1.65V to 1.95V		0.65xV_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7xV_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=1.65V to 1.95V		-	-	0.35xV_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3xV_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	V_{CC}-0.1	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.2	1.54	-	V
			I_O=-8mA; V_{CC}=2.3V	1.9	2.15	-	V
			I_O=-12mA; V_{CC}=2.7V	2.2	2.50	-	V
			I_O=-24mA; V_{CC}=3.0V	2.3	2.62	-	V
			I_O=-32mA; V_{CC}=4.5V	3.8	4.11	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 5.5V	-	-	0.10	V
			I_O=4mA; V_{CC}=1.65V	-	0.07	0.45	V
			I_O=8mA; V_{CC}=2.3V	-	0.12	0.30	V
			I_O=12mA; V_{CC}=2.7V	-	0.17	0.40	V
			I_O=24mA; V_{CC}=3.0V	-	0.33	0.55	V
			I_O=32mA; V_{CC}=4.5V	-	0.39	0.55	V
I_I	Input leakage current	V_I=5.5V or GND;V_{CC}=0V to 5.5V		-	-	±1	uA
I_{OFF}	Power-off leakage current	V_I or V_O=5.5V; V_{CC}=0V		-	-	±2	uA
I_{CC}	Supply current	V_I=5.5V or GND; I_O=0A;V_{CC}=1.65V to 5.5V		-	-	4	uA
ΔI_{CC}	Additional supply current	V_I=V_{CC}-0.6V; I_O=0A;V_{CC}=2.3V to 5.5V		-	-	500	uA

Note: Typical values are measured at T_{amb}=25°C.

7.3.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=1.65V to 1.95V		0.65xV_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7xV_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=1.65V to 1.95V		-	-	0.35xV_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3xV_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	V_{CC}-0.1	-	-	V
			I_O=-4mA; V_{CC}=1.65V	0.95	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.7	-	-	V
			I_O=-12mA; V_{CC}=2.7V	1.9	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.0	-	-	V
			I_O=-32mA; V_{CC}=4.5V	3.4	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 5.5V	-	-	0.10	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.70	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.45	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.60	V
			I_O=24mA; V_{CC}=3.0V	-	-	0.80	V
			I_O=32mA; V_{CC}=4.5V	-	-	0.80	V
I_I	Input leakage current	V_I=5.5V or GND; V_{CC}=0V to 5.5V		-	-	±1	uA
I_{OFF}	Power-off leakage current	V_I or V_O=5.5V; V_{CC}=0V		-	-	±2	uA
I_{CC}	Supply current	V_I=5.5V or GND; I_O=0A;V_{CC}=1.65V to 5.5V		-	-	4	uA
ΔI_{CC}	Additional supply current	V_I=V_{CC}-0.6V; I_O=0A;V_{CC}=2.3V to 5.5V		-	-	500	uA

7.3.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground = 0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PLH}, t_{PHL}	A to Y propagation delay	See Figure 8-4	V_{CC}=1.65V to 1.95V	-	4.9	13.4	ns
			V_{CC}=2.3V to 2.7V	-	3.1	7.1	ns
			V_{CC}=2.7V	-	3.2	7.1	ns
			V_{CC}=3.0V to 3.6V	-	3.1	5.7	ns
			V_{CC}=4.5V to 5.5V	-	2.2	4.0	ns
t_{PHL}	$\overline{MR}$ to Q High to Low propagation delay	See Figure 8-5	V_{CC}=1.65V to 1.95V	-	4.3	12.9	ns
			V_{CC}=2.3V to 2.7V	-	2.8	7.0	ns
			V_{CC}=2.7V	-	3.0	7.0	ns
			V_{CC}=3.0V to 3.6V	-	2.5	5.8	ns
			V_{CC}=4.5V to 5.5V	-	2.0	4.1	ns
t_W	CP HIGH or LOW pulse width	See Figure 8-4	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	-	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
	$\overline{MR}$ LOW pulse width	See Figure 8-5	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	-	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-5	V_{CC}=1.65V to 1.95V	1.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.4	-	-	ns
			V_{CC}=2.7V	1.3		-	ns
			V_{CC}=3.0V to 3.6V	1.2	-	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
t_{su}	D to CP Set-up time	See Figure 8-4	V_{CC}=1.65V to 1.95V	2.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.7	-	-	ns
			V_{CC}=2.7V	1.7	-	-	ns
			V_{CC}=3.0V to 3.6V	1.3	-	-	ns
			V_{CC}=4.5V to 5.5V	1.1	-	-	ns
t_h	D to CP hold time	See Figure 8-4	V_{CC}=1.65V to 1.95V	0.0	-	-	ns
			V_{CC}=2.3V to 2.7V	0.3	-	-	ns
			V_{CC}=2.7V	0.5	-	-	ns
			V_{CC}=3.0V to 3.6V	1.2	-	-	ns
			V_{CC}=4.5V to 5.5V	0.5	-	-	ns

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
f_{max}	Maximum frequency	See Figure 8-4	V_{CC}=1.65V to 1.95V	80	-	-	MHz
			V_{CC}=2.3V to 2.7V	175	-	-	MHz
			V_{CC}=2.7V	175	-	-	MHz
			V_{CC}=3.0V to 3.6V	175	-	-	MHz
			V_{CC}=4.5V to 5.5V	200	-	-	MHz

Note: Typical values are measured at T_{amb}=25°C and V_{CC}=1.8V, 2.5V, 2.7V, 3.3V and 5.0V respectively.

7.3.4 AC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground = 0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PLH}, t_{PHL}	A to Y propagation delay	See Figure 8-4	V_{CC}=1.65V to 1.95V	-	-	17	ns
			V_{CC}=2.3V to 2.7V	-	-	9.0	ns
			V_{CC}=2.7V	-	-	9.0	ns
			V_{CC}=3.0V to 3.6V	-	-	7.5	ns
			V_{CC}=4.5V to 5.5V	-	-	5.5	ns
t_{PHL}	$\overline{MR}$ to Q propagation delay	See Figure 8-5	V_{CC}=1.65V to 1.95V	-	-	17	ns
			V_{CC}=2.3V to 2.7V	-	-	9.0	ns
			V_{CC}=2.7V	-	-	9.0	ns
			V_{CC}=3.0V to 3.6V	-	-	7.5	ns
			V_{CC}=4.5V to 5.5V	-	-	5.5	ns
t_W	CP HIGH or LOW pulse width	See Figure 8-4	V_{CC}=1.65V to 1.95V	6.8	-	-	ns
			V_{CC}=2.3V to 2.7V	2.9	-	-	ns
			V_{CC}=2.7V	2.9	-	-	ns
			V_{CC}=3.0V to 3.6V	2.9	-	-	ns
			V_{CC}=4.5V to 5.5V	2.2	-	-	ns
	$\overline{MR}$ LOW pulse width	See Figure 8-5	V_{CC}=1.65V to 1.95V	6.8	-	-	ns
			V_{CC}=2.3V to 2.7V	2.9	-	-	ns
			V_{CC}=2.7V	2.9	-	-	ns
			V_{CC}=3.0V to 3.6V	2.9	-	-	ns
			V_{CC}=4.5V to 5.5V	2.2	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-5	V_{CC}=1.65V to 1.95V	2.1	-	-	ns
			V_{CC}=2.3V to 2.7V	1.5	-	-	ns
			V_{CC}=2.7V	1.4	-	-	ns
			V_{CC}=3.0V to 3.6V	1.3	-	-	ns
			V_{CC}=4.5V to 5.5V	1.1	-	-	ns

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{su}	D to CP Set-up time	See Figure 8-4	V_{CC}=1.65V to 1.95V	3.2	-	-	ns
			V_{CC}=2.3V to 2.7V	1.8	-	-	ns
			V_{CC}=2.7V	1.8	-	-	ns
			V_{CC}=3.0V to 3.6V	1.4	-	-	ns
			V_{CC}=4.5V to 5.5V	1.2	-	-	ns
t_h	D to CP hold time	See Figure 8-4	V_{CC}=1.65V to 1.95V	0.0	-	-	ns
			V_{CC}=2.3V to 2.7V	0.3	-	-	ns
			V_{CC}=2.7V	0.6	-	-	ns
			V_{CC}=3.0V to 3.6V	1.3	-	-	ns
			V_{CC}=4.5V to 5.5V	0.6	-	-	ns
f_{max}	Maximum frequency	See Figure 8-4	V_{CC}=1.65V to 1.95V	72	-	-	MHz
			V_{CC}=2.3V to 2.7V	159	-	-	MHz
			V_{CC}=2.7V	159	-	-	MHz
			V_{CC}=3.0V to 3.6V	159	-	-	MHz
			V_{CC}=4.5V to 5.5V	182	-	-	MHz

8 Detailed Description

8.1 Overview

The CJ74LVC1G175 is a low-power, low-voltage single positive edge triggered D-type flip-flop with individual data (D) input, clock (CP) input, master reset (/MR) input, and Q output.

The input can be driven from either 3.3V or 5V devices. This feature allows the use of this device in a mixed 3.3V and 5V environment.

8.2 Functional Block Diagram

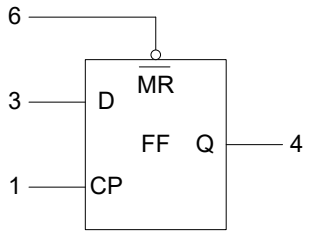


Figure 8-1 Logic symbol

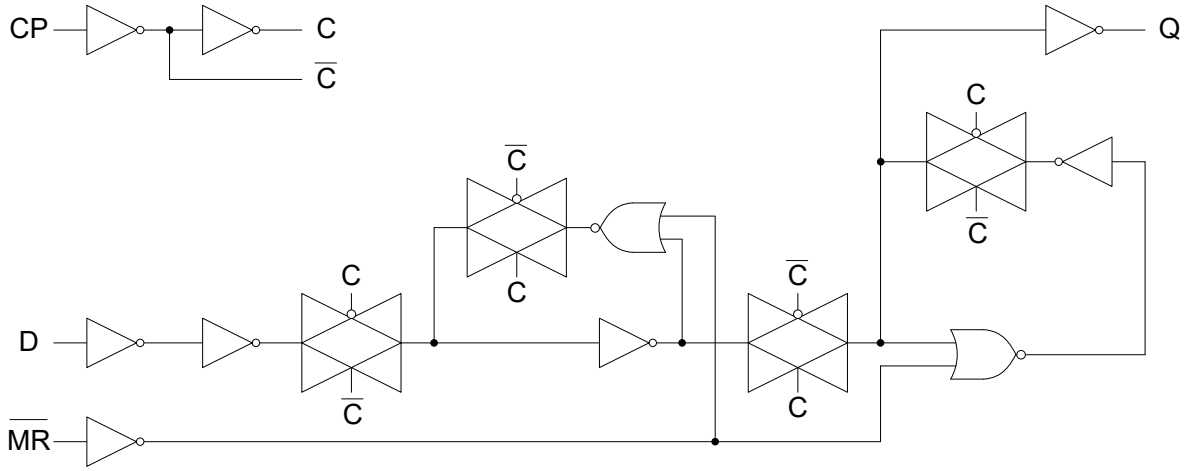


Figure 8-2 Logic diagram

8.3 Function Table

OPERATING MODE	INPUT			OUTPUT
	$\overline{MR}$	CP	D	Q
Reset(clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

Note:

(1) H = HIGH voltage level; L = LOW voltage level.

(2) h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;

(3) l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;

(4) ↑ = LOW-to-HIGH CP transition

(5) X = don't care

8.4 Testing Circuit

8.4.1 AC Testing Circuit

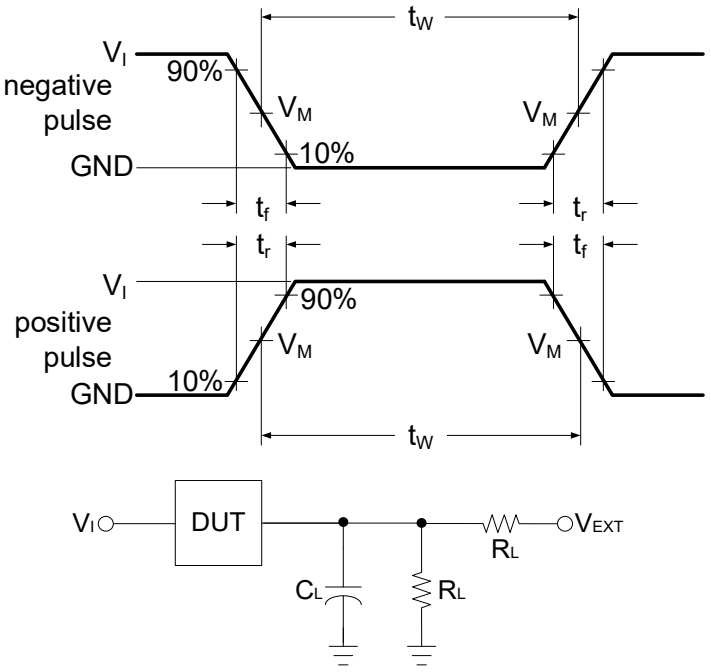


Figure 8-3 Load circuit

Definitions for test circuit:

C_L includes probe and jig capacitance.

R_L=Load resistance.

8.4.2 AC Testing Waveforms

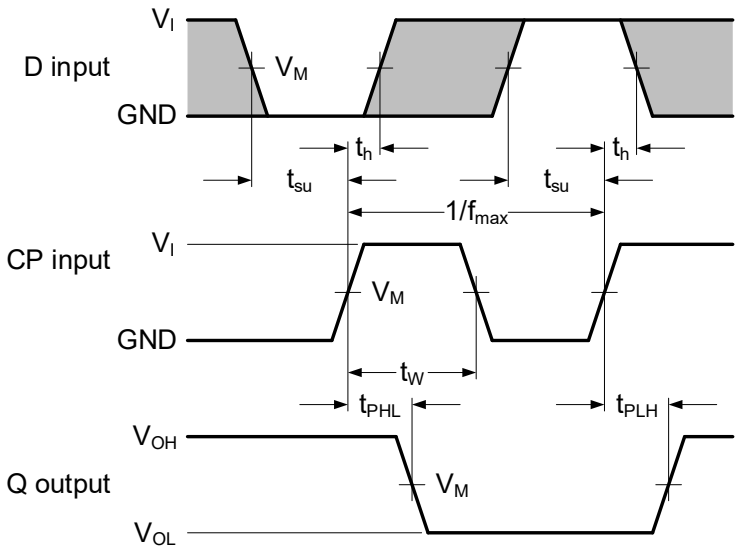


Figure 8-4 The clock input (CP) to output (Q) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times, and the maximum clock pulse frequency

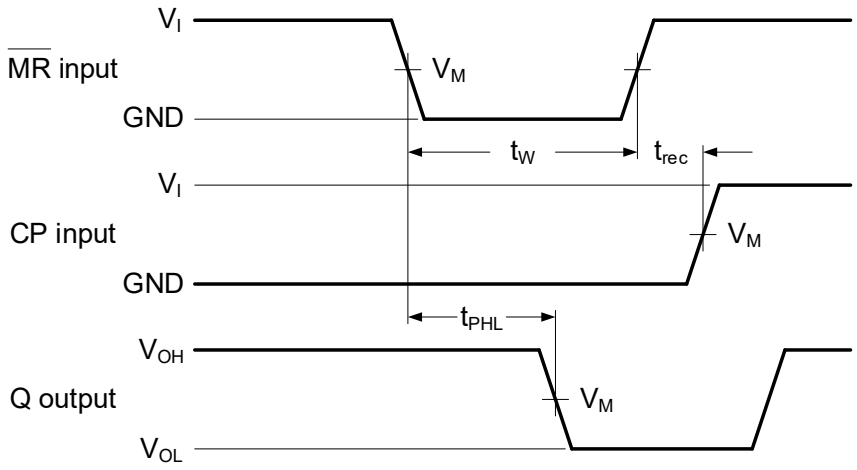


Figure 8-5 The master reset ($\overline{MR}$) input to output (Q) propagation delays, the master reset pulse width, and the $\overline{MR}$ to CP recovery time

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{CC}	V_M	V_M
1.65V to 1.95V	0.5xV_{CC}	0.5xV_{CC}
2.3V to 2.7V	0.5xV_{CC}	0.5xV_{CC}
2.7V	0.5xV_{CC}	0.5xV_{CC}
3.0V to 3.6V	0.5xV_{CC}	0.5xV_{CC}
4.5V to 5.5V	0.5xV_{CC}	0.5xV_{CC}

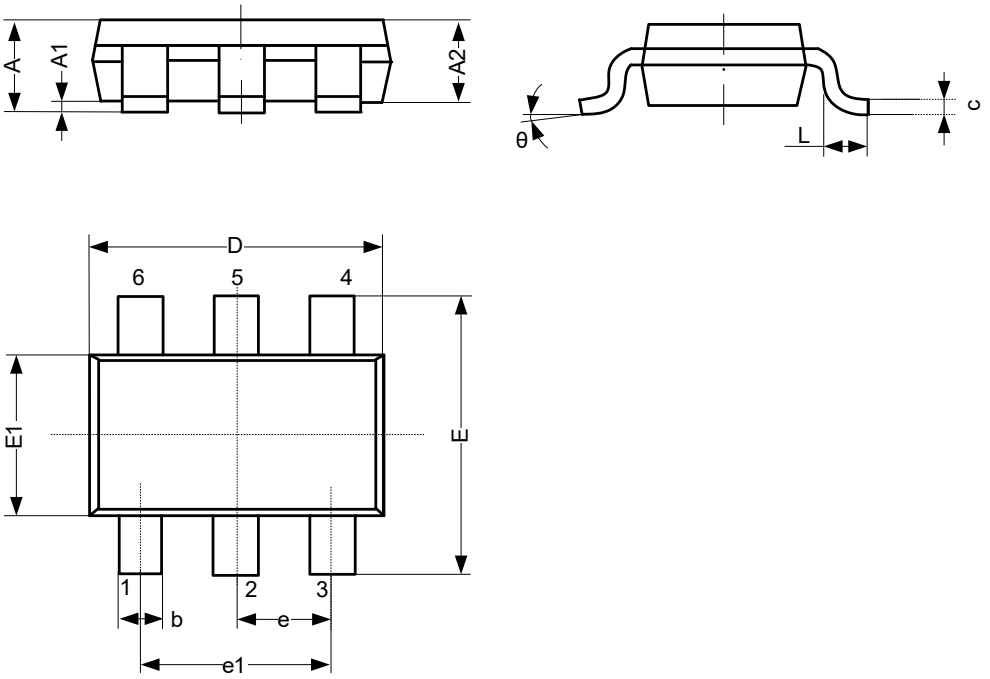
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
1.65V to 1.95V	V_{CC}	≤ 3ns	30pF	1kΩ	Open	2xV_{CC}	GND
2.3V to 2.7V	V_{CC}	≤ 3ns	30pF	500Ω	Open	2xV_{CC}	GND
2.7V	V_{CC}	≤ 3ns	50pF	500Ω	Open	2xV_{CC}	GND
3.0V to 3.6V	V_{CC}	≤ 3ns	50pF	500Ω	Open	2xV_{CC}	GND
4.5V to 5.5V	V_{CC}	≤ 3ns	50pF	500Ω	Open	2xV_{CC}	GND

9 Mechanical Information

9.1 SOT-23-6L Mechanical Information

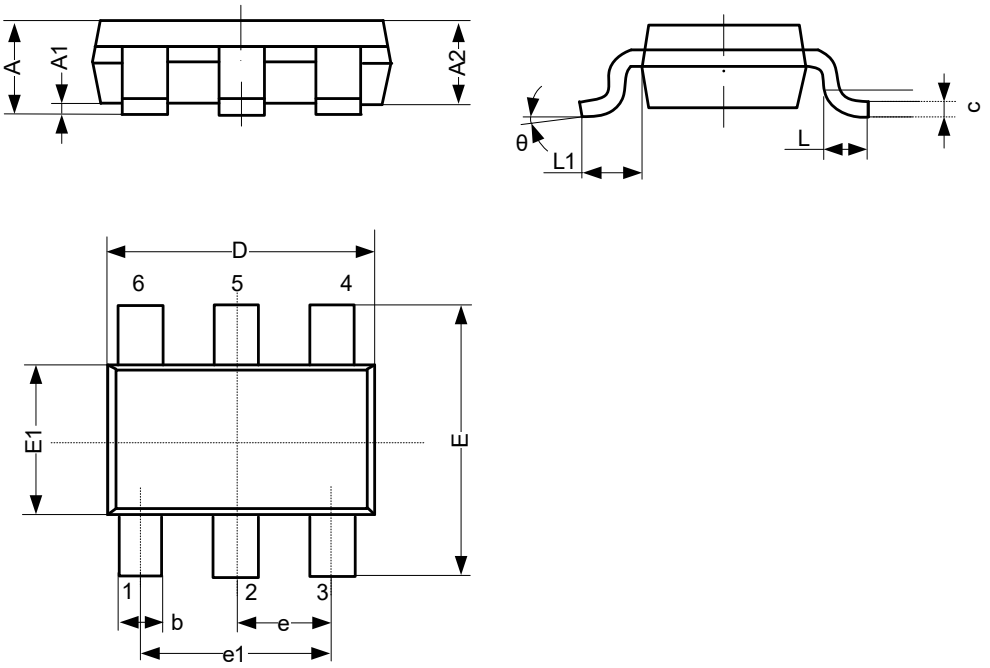
9.1.1 SOT-23-6L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.25
A1	0.00	-	0.12
A2	1.00	-	1.20
b	0.30	-	0.50
c	0.10	-	0.20
D	2.82	-	3.02
E	2.60	-	3.00
E1	1.50	-	1.70
e	0.95 BSC		
e1	1.80	-	2.00
L	0.30	-	0.60
Θ	0°	-	8°
Unit: mm			

9.2 SOT-363 Mechanical Information

9.2.1 SOT-363 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.90	-	1.10
A1	0.00	-	0.10
A2	0.90	-	1.00
b	0.15	-	0.35
c	0.11	-	0.175
D	2.00	-	2.20
E	2.15	-	2.45
E1	1.15	-	1.35
e	0.65 BSC		
e1	1.20	-	1.40
L	0.26	-	0.46
L1	-	0.525	-
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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