Single D-type Flip-flop with Set and Reset；Positive Edge Trigger

CJ74LVC2G74 Logic

1 Introduction

The CJ74LVC2G74 is a single positive-edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set (/SD) and reset (/RD) inputs, and complementary Q and /Q outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable, one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LVC2G74	TSSOP8(3x3)
	VSSOP8

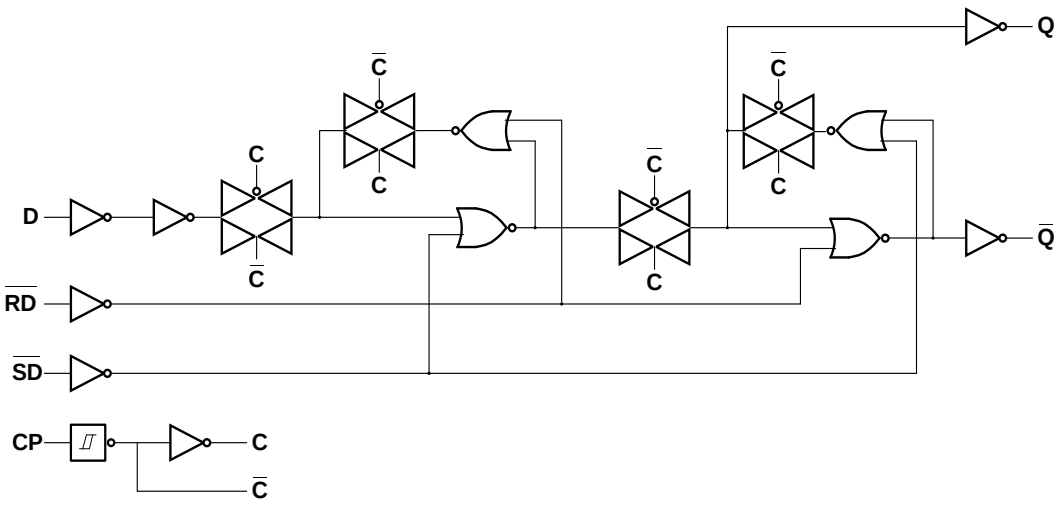
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 1.65V to 5.5V
- 5 V tolerant outputs for interfacing with 5 V logic
- ±24mA output drive (V_{CC}=3.0V)
- CMOS low power consumption
- Latch-up performance exceeds 250mA
- Specified from -40°C to +125°C

4 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LVC2G74BAN	TSSOP8(3x3)	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active
CJ74LVC2G74VAN	VSSOP8	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

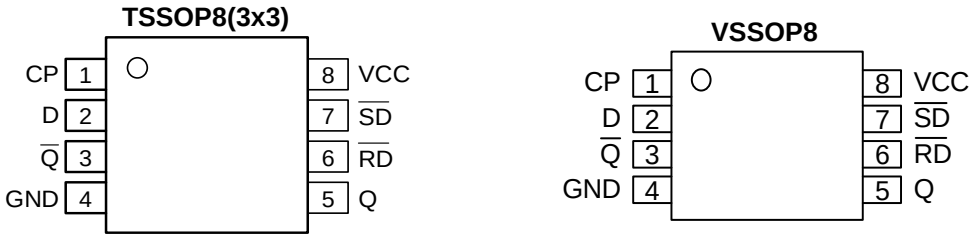


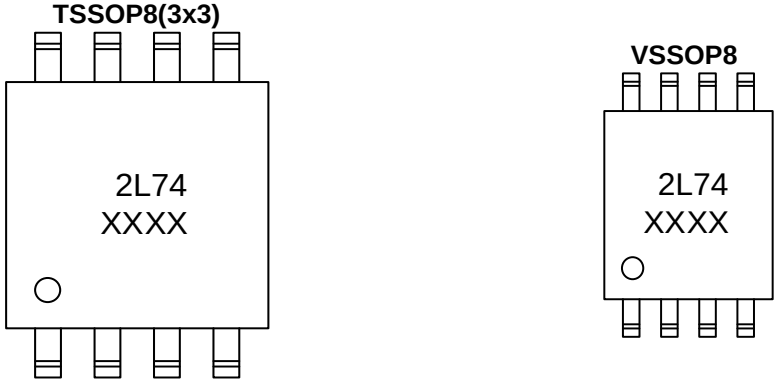
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	CP	I	Clock input (LOW-to-HIGH, edge-triggered)
2	D	I	Data input
3	$\overline{Q}$	O	Complement output
4	GND	G	Ground (0V)
5	Q	O	True output
6	$\overline{RD}$	I	Asynchronous reset-direct input (active LOW)
7	$\overline{SD}$	I	Asynchronous set-direct input (active LOW)
8	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-	-0.5	+6.5	V
I_{IK}	Input clamping current	V_I < 0V	-50	-	mA
V_I	Input voltage	-	-0.5	+6.5	V
I_{OK}	Output clamping current	V_O > V_{CC} or V_O < 0V	-	±50	mA
V_O	Output voltage	Active mode	-0.5	V_{CC}+0.5	V
		Power-down mode; V_{CC}=0V	-0.5	+6.5	V
I_O	Output current	V_O=0V to V_{CC}	-	±50	mA
I_{CC}	Supply current	-	-	100	mA
I_{GND}	Ground current	-	-100	-	mA
P_{tot}	Total power dissipation	-	-	300	mW
T_{stg}	Storage temperature	-	-65	+150	°C
T_L	Soldering temperature	10s	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	-	1.65	-	5.5	V
V_I	Input voltage	-	0	-	5.5	V
V_O	Output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC}=0V	0	-	5.5	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 Electrical Characteristics

7.3.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=1.65V to 1.95V		0.65×V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7×V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=1.65V to 1.95V		-	-	0.35xV_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3xV_{CC}	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	V_{CC}-0.1	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.2	1.54	-	V
			I_O=-8mA; V_{CC}=2.3V	1.9	2.15	-	V
			I_O=-12mA; V_{CC}=2.7V	2.2	2.50	-	V
			I_O=-24mA; V_{CC}=3.0V	2.3	2.62	-	V
			I_O=-32mA; V_{CC}=4.5V	3.8	4.11	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 5.5V	-	-	0.10	V
			I_O=4mA; V_{CC}=1.65V	-	0.07	0.45	V
			I_O=8mA; V_{CC}=2.3V	-	0.12	0.30	V
			I_O=12mA; V_{CC}=2.7V	-	0.17	0.40	V
			I_O=24mA; V_{CC}=3.0V	-	0.33	0.55	V
			I_O=32mA; V_{CC}=4.5V	-	0.39	0.55	V
I_I	Input leakage current	V_I=5.5V or GND; V_{CC}=0V to 5.5V		-	-	±1	uA
I_{OFF}	Power-off leakage current	V_I or V_O=5.5V; V_{CC}=0V		-	-	±2	uA
I_{CC}	Supply current	V_I =5.5V or GND; I_O=0A; V_{CC} =1.65V to 5.5V		-	-	4	uA
ΔI_{CC}	Additional supply current	Per pin; V_I = V_{CC} -0.6V; I_O =0A; V_{CC} =2.3V to 5.5V		-	-	500	uA
C_I	Input capacitance	-		-	4.0	-	pF

Note: All typical values are measured at T_{amb}=25°C.

7.3.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=1.65V to 1.95V		0.65xV_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7xV_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=1.65V to 1.95V		-	-	0.35xV_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3xV_{CC}	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	V_{CC}-0.1	-	-	V
			I_O=-4mA; V_{CC}=1.65V	0.95	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.7	-	-	V
			I_O=-12mA; V_{CC}=2.7V	1.9	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.0	-	-	V
			I_O=-32mA; V_{CC}=4.5V	3.4	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	-	-	0.10	V
			I_O=-4mA; V_{CC}=1.65V	-	-	0.70	V
			I_O=-8mA; V_{CC}=2.3V	-	-	0.45	V
			I_O=-12mA; V_{CC}=2.7V	-	-	0.60	V
			I_O=-24mA; V_{CC}=3.0V	-	-	0.80	V
			I_O=-32mA; V_{CC}=4.5V	-	-	0.80	V
I_I	Input leakage current	V_I=5.5V or GND; V_{CC}=0V to 5.5V		-	-	±1	uA
I_{OFF}	Power-off leakage current	V_I or V_O=5.5V; V_{CC} =0V		-	-	±2	uA
I_{CC}	Supply current	V_I =5.5V or GND; I_O=0A; V_{CC} =1.65V to 5.5V		-	-	4	uA
ΔI_{CC}	Additional supply current	Per pin; V_I =V_{CC}-0.6V; I_O=0A; V_{CC}=2.3V to 5.5V		-	-	500	uA

7.3.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
t_{PHL}	Propagation delay	CP to Q, $\overline{Q}$; See Figure 8-5	V_{CC}=1.65V to 1.95V	-	12.5	18.8	ns
			V_{CC}=2.3V to 2.7V	-	10.5	15.8	ns
			V_{CC}=2.7V	-	10	15	ns
			V_{CC}=3.0V to 3.6V	-	9.5	14.3	ns
			V_{CC}=4.5V to 5.5V	-	9	13.5	ns
		$\overline{SD}$ to Q, $\overline{Q}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	-	12.5	18.8	ns
			V_{CC}=2.3V to 2.7V	-	10.5	15.8	ns
			V_{CC}=2.7V	-	10	15	ns
			V_{CC}=3.0V to 3.6V	-	9.5	14.3	ns
			V_{CC}=4.5V to 5.5V	-	9	13.5	ns
		$\overline{RD}$ to Q, $\overline{Q}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	-	12.5	18.8	ns
			V_{CC}=2.3V to 2.7V	-	10.5	15.8	ns
			V_{CC}=2.7V	-	10	15	ns
			V_{CC}=3.0V to 3.6V	-	9.5	14.3	ns
			V_{CC}=4.5V to 5.5V	-	9	13.5	ns
t_{PLH}	Propagation delay	CP to Q, $\overline{Q}$; See Figure 8-5	V_{CC}=1.65V to 1.95V	-	14	21	ns
			V_{CC}=2.3V to 2.7V	-	10	15	ns
			V_{CC}=2.7V	-	9.5	14.3	ns
			V_{CC}=3.0V to 3.6V	-	8.5	12.8	ns
			V_{CC}=4.5V to 5.5V	-	7.5	11.3	ns
		$\overline{SD}$ to Q, $\overline{Q}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	-	14	21	ns
			V_{CC}=2.3V to 2.7V	-	10	15	ns
			V_{CC}=2.7V	-	9.5	14.3	ns
			V_{CC}=3.0V to 3.6V	-	8.5	12.8	ns
			V_{CC}=4.5V to 5.5V	-	7.5	11.3	ns
		$\overline{RD}$ to Q, $\overline{Q}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	-	14	21	ns
			V_{CC}=2.3V to 2.7V	-	10	15	ns
			V_{CC}=2.7V	-	9.5	14.3	ns
			V_{CC}=3.0V to 3.6V	-	8.5	12.8	ns
			V_{CC}=4.5V to 5.5V	-	7.5	11.3	ns

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_W	Pulse width	CP HIGH or LOW; See Figure 8-5	V_{CC} =1.65V to 1.95V	6.2	-	-	ns
			V_{CC} =2.3V to 2.7V	2.7	-	-	ns
			V_{CC} =2.7V	2.7	-	-	ns
			V_{CC} =3.0V to 3.6V	2.7	-	-	ns
			V_{CC} =4.5V to 5.5V	2.0	-	-	ns
		$\overline{SD}$ and $\overline{RD}$ LOW; See Figure 8-6	V_{CC} =1.65V to 1.95V	6.2	-	-	ns
			V_{CC} =2.3V to 2.7V	2.7	-	-	ns
			V_{CC} =2.7V	2.7	-	-	ns
			V_{CC} =3.0V to 3.6V	2.7	-	-	ns
			V_{CC} =4.5V to 5.5V	2.0	-	-	ns
t_{rec}	Recovery time	$\overline{SD}$ or $\overline{RD}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	1.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.4	-	-	ns
			V_{CC}=2.7V	1.3	-	-	ns
			V_{CC}=3.0V to 3.6V	1.2	-	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
t_{su}	Set-up time	D to CP; See Figure 8-5	V_{CC}=1.65V to 1.95V	2.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.7	-	-	ns
			V_{CC}=2.7V	1.7	-	-	ns
			V_{CC}=3.0V to 3.6V	1.3	-	-	ns
			V_{CC}=4.5V to 5.5V	1.1	-	-	ns
t_h	Hold time	D to CP; See Figure 8-5	V_{CC}=1.65V to 1.95V	1.5	-	-	ns
			V_{CC}=2.3V to 2.7V	1.0	-	-	ns
			V_{CC}=2.7V	1.0	-	-	ns
			V_{CC}=3.0V to 3.6V	1.0	-	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
f_{max}	Maximum frequency	CP; See Figure 8-5	V_{CC} =1.65V to 1.95V	80	-	-	MHz
			V_{CC} =2.3V to 2.7V	175	-	-	MHz
			V_{CC} =2.7V	175	-	-	MHz
			V_{CC} =3.0V to 3.6V	175	280	-	MHz
			V_{CC} =4.5V to 5.5V	200	-	-	MHz
C_{PD}	Power dissipation capacitance	V_{CC}=3.3V; V_I=GND to V_{CC}		-	15	-	pF

(1) Typical values are measured at T_{amb}=25°C and V_{CC}=1.8V, 2.5V, 2.7V, 3.3V and 5.0V respectively.

7.3.4 AC Characteristics 2

T_{amb}=-40°C to +125°C,voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}	Propagation delay	CP to Q, $\overline{Q}$; See Figure 8-5	V_{CC}=1.65V to 1.95V	-	-	20.8	ns
			V_{CC}=2.3V to 2.7V	-	-	17.8	ns
			V_{CC}=2.7V	-	-	17	ns
			V_{CC}=3.0V to 3.6V	-	-	16.3	ns
			V_{CC}=4.5V to 5.5V	-	-	15.5	ns
		$\overline{SD}$ to Q, $\overline{Q}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	-	-	20.8	ns
			V_{CC}=2.3V to 2.7V	-	-	17.8	ns
			V_{CC}=2.7V	-	-	17	ns
			V_{CC}=3.0V to 3.6V	-	-	16.3	ns
			V_{CC}=4.5V to 5.5V	-	-	15.5	ns
		$\overline{RD}$ to Q, $\overline{Q}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	-	-	20.8	ns
			V_{CC}=2.3V to 2.7V	-	-	17.8	ns
			V_{CC}=2.7V	-	-	17	ns
			V_{CC}=3.0V to 3.6V	-	-	16.3	ns
			V_{CC}=4.5V to 5.5V	-	-	15.5	ns
t_{PLH}	Propagation delay	CP to Q, $\overline{Q}$; See Figure 8-5	V_{CC}=1.65V to 1.95V	-	-	23	ns
			V_{CC}=2.3V to 2.7V	-	-	17	ns
			V_{CC}=2.7V	-	-	16.3	ns
			V_{CC}=3.0V to 3.6V	-	-	14.8	ns
			V_{CC}=4.5V to 5.5V	-	-	13.3	ns
		$\overline{SD}$ to Q, $\overline{Q}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	-	-	23	ns
			V_{CC}=2.3V to 2.7V	-	-	17	ns
			V_{CC}=2.7V	-	-	16.3	ns
			V_{CC}=3.0V to 3.6V	-	-	14.8	ns
			V_{CC}=4.5V to 5.5V	-	-	13.3	ns
		$\overline{RD}$ to Q, $\overline{Q}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	-	-	23	ns
			V_{CC}=2.3V to 2.7V	-	-	17	ns
			V_{CC}=2.7V	-	-	16.3	ns
			V_{CC}=3.0V to 3.6V	-	-	14.8	ns
			V_{CC}=4.5V to 5.5V	-	-	13.3	ns

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_W	Pluse width	CP HIGH or LOW; See Figure 8-5	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	-	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
		$\overline{SD}$ and $\overline{RD}$ LOW; See Figure 8-6	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	-	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
t_{rec}	Recovery time	$\overline{SD}$ or $\overline{RD}$; See Figure 8-6	V_{CC}=1.65V to 1.95V	1.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.4	-	-	ns
			V_{CC}=2.7V	1.3	-	-	ns
			V_{CC}=3.0V to 3.6V	1.2	-	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
t_{su}	Set-up time	D to CP; See Figure 8-5	V_{CC}=1.65V to 1.95V	2.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.7	-	-	ns
			V_{CC}=2.7V	1.7	-	-	ns
			V_{CC}=3.0V to 3.6V	1.3	-	-	ns
			V_{CC}=4.5V to 5.5V	1.1	-	-	ns
t_h	Hold time	D to CP; See Figure 8-5	V_{CC}=1.65V to 1.95V	1.5	-	-	ns
			V_{CC}=2.3V to 2.7V	1.0	-	-	ns
			V_{CC}=2.7V	1.0	-	-	ns
			V_{CC}=3.0V to 3.6V	1.0	-	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
f_{max}	Maximum frequency	CP; See Figure 8-5	V_{CC}=1.65V to 1.95V	80	-	-	MHz
			V_{CC}=2.3V to 2.7V	175	-	-	MHz
			V_{CC}=2.7V	175	-	-	MHz
			V_{CC}=3.0V to 3.6V	175	-	-	MHz
			V_{CC}=4.5V to 5.5V	200	-	-	MHz

8 Detailed Description

8.1 Overview

The CJ74LVC2G74 is a single positive-edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set (/SD) and reset (/RD) inputs, and complementary Q and /Q outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable, one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

8.2 Functional Block Diagram

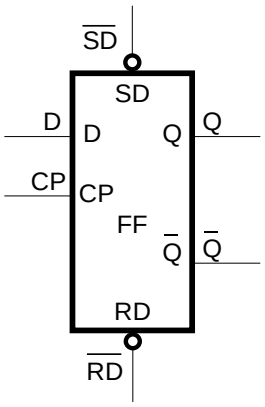


Figure 8-1 Logic symbol

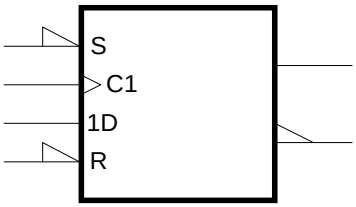


Figure 8-2 IEC logic symbol

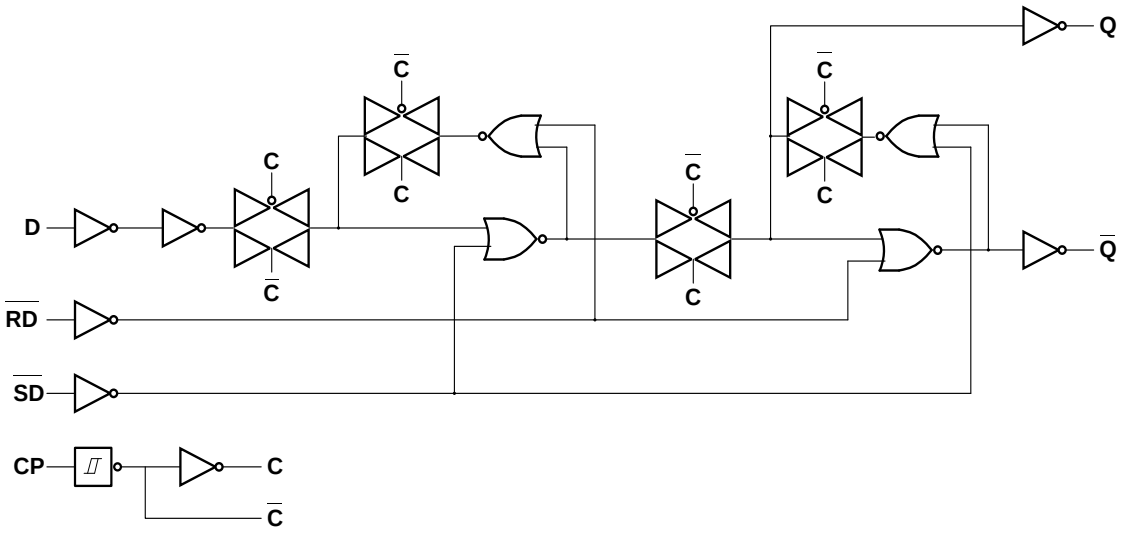


Figure 8-3 Logic diagram

8.3 Function Table

Function table for asynchronous operation

INPUT				OUTPUT	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

Function table for asynchronous operation

INPUT				OUTPUT	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

Note: H=HIGH voltage level; L=LOW voltage level; ↑=LOW-to-HIGH CP transition; Qn+1=state after the next LOW-to-HIGH CP transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

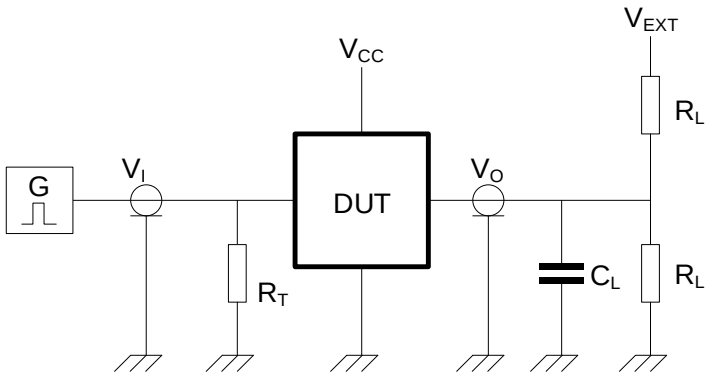


Figure 8-4 Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance; should be equal to the output impedance Z_o of the pulse generator.

V_{EXT}=External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

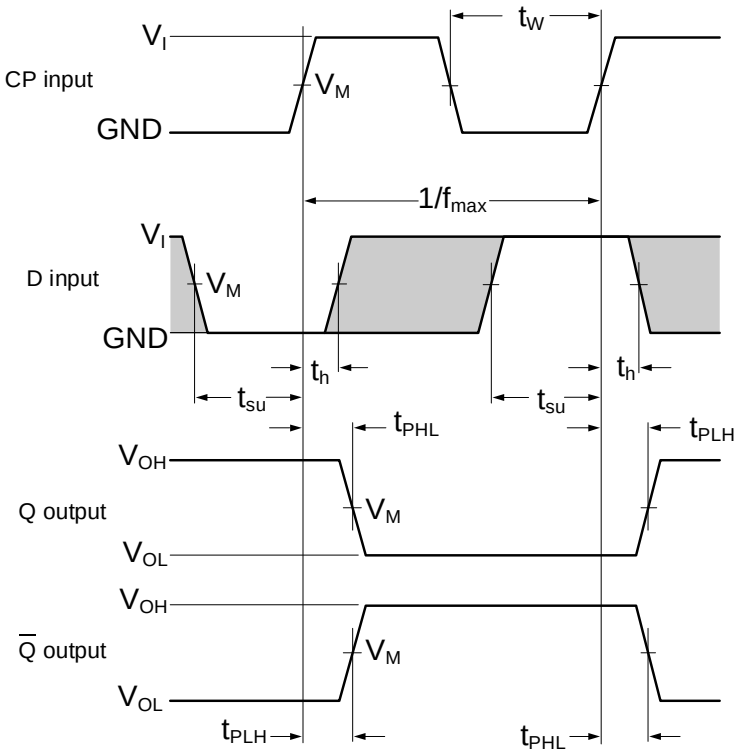


Figure 8-5 The clock input (CP) to output (Q,$\overline{Q}$) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times and the maximum frequency

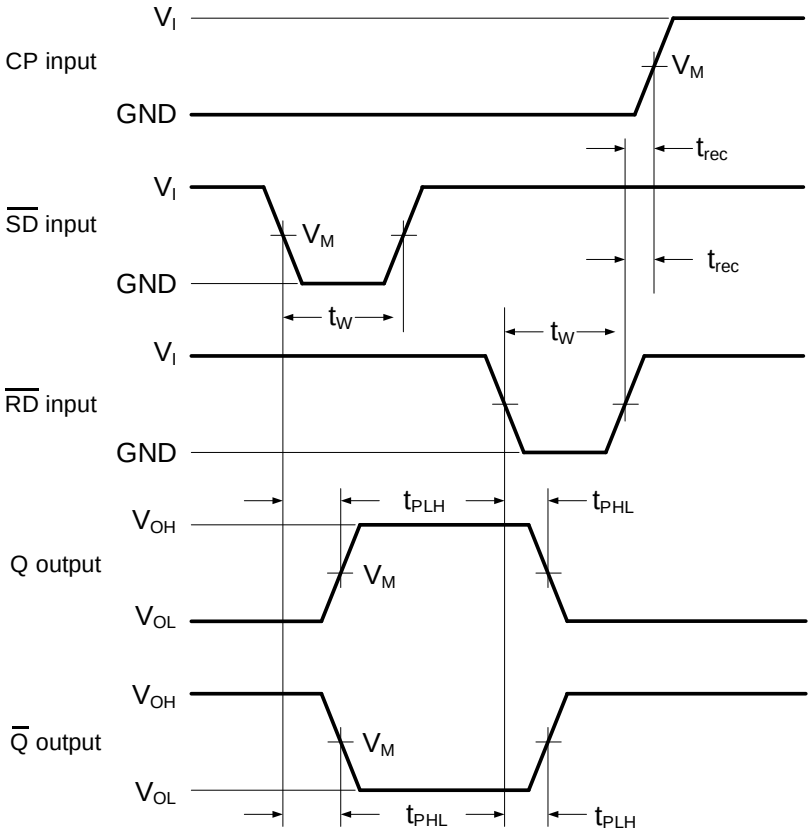


Figure 8-6 The set ($\overline{SD}$) and reset ($\overline{RD}$) to output (Q, $\overline{Q}$) propagation delays, the set and reset pulse widths and the $\overline{RD}$ to CP recovery time

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{CC}	V_M	V_M
1.65V to 1.95V	0.5xV_{CC}	0.5xV_{CC}
2.3V to 2.7V	0.5xV_{CC}	0.5xV_{CC}
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	0.5xV_{CC}	0.5xV_{CC}

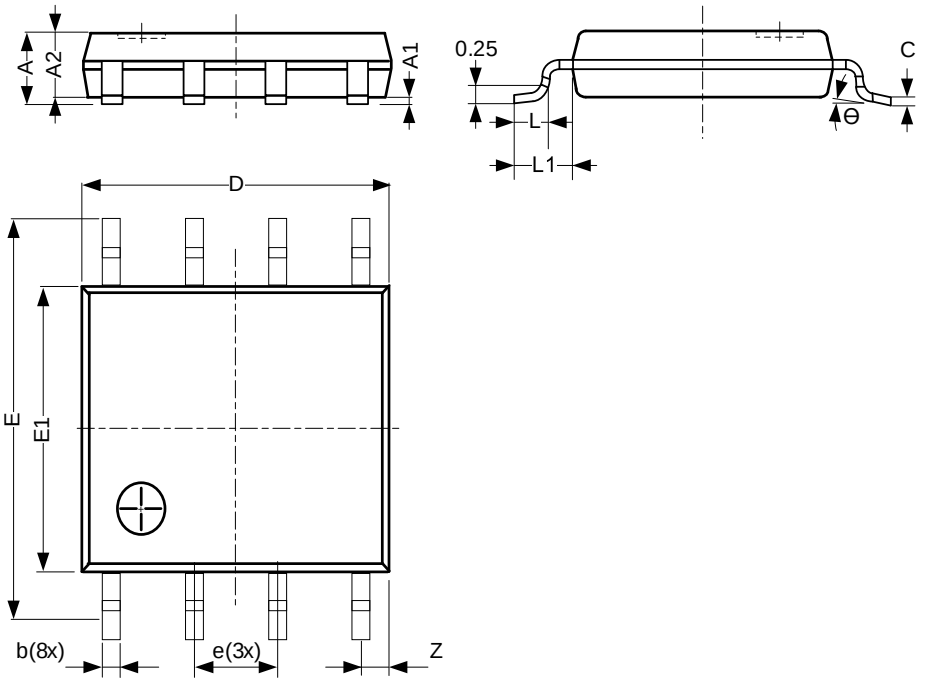
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65V to 1.95V	V_{CC}	≤ 3ns	30pF	1kΩ	Open	GND	2xV_{CC}
2.3V to 2.7V	V_{CC}	≤ 3ns	30pF	500Ω	Open	GND	2xV_{CC}
2.7V	2.7V	≤ 3ns	50pF	500Ω	Open	GND	6V
3.0V to 3.6V	2.7V	≤ 3ns	50pF	500Ω	Open	GND	6V
4.5V to 5.5V	V_{CC}	≤ 3ns	50pF	500Ω	Open	GND	2xV_{CC}

9 Mechanical Information

9.1 TSSOP8(3x3) Mechanical Information

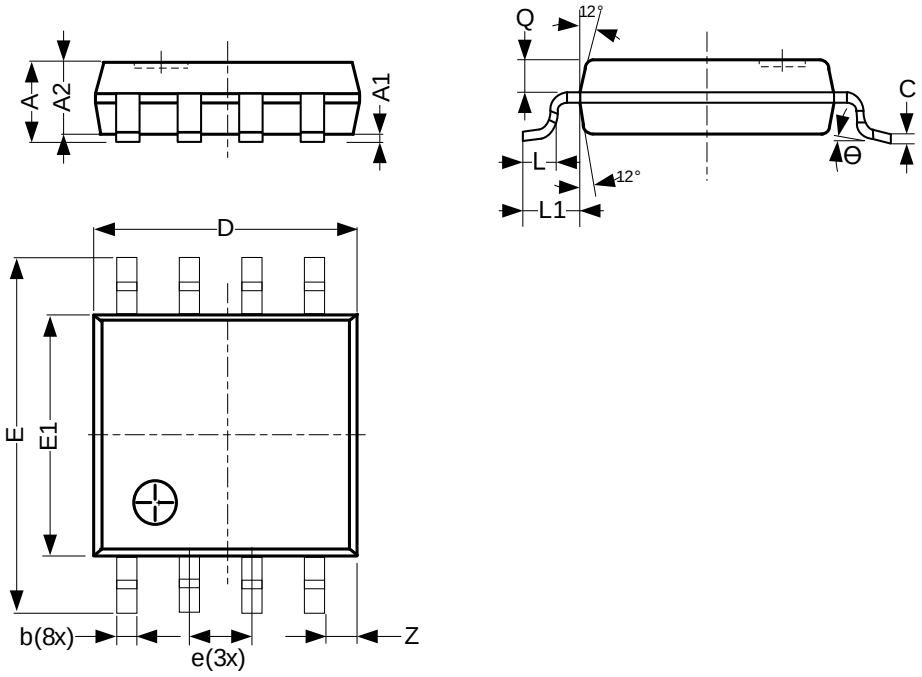
9.1.1 TSSOP8(3x3) Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.10
A1	0	-	0.15
A2	0.75	-	0.95
b	0.22	-	0.38
c	0.08	-	0.18
D	2.90	-	3.10
E	3.90	-	4.10
E1	2.90	-	3.10
e	0.65 BSC		
L	0.33	-	0.47
L1	-	0.50	-
Z	0.35	-	0.70
Θ	0°	-	8°
Unit: mm			

9.2 VSSOP8 Mechanical Information

9.2.1 VSSOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.00
A1	0	-	0.15
A2	0.60	-	0.85
Q	0.19	-	0.21
b	0.17	-	0.27
c	0.08	-	0.23
D	1.90	-	2.10
E	3.00	-	3.20
E1	2.20	-	2.40
e	0.50 BSC		
L	0.15	-	0.40
L1	-	0.40	-
Z	0.10	-	0.40
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

January, 2026: rev -1.1A, Change TSSOP8 marking information.

April, 2026: rev -1.2A, Update package from TSSOP8 to TSSOP8(3x3).

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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