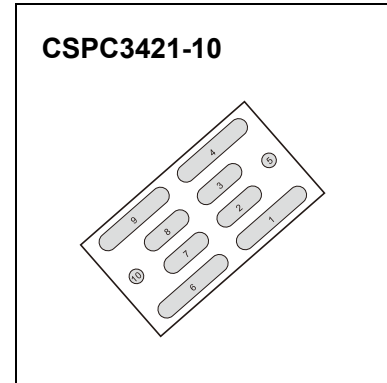




CSP Enhancement Mode Power MOSFET

CJ8508SP Dual N-Channel MOSFET

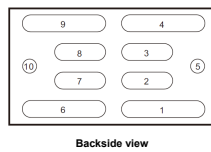
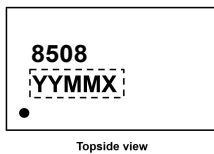
V _{SSS}	R _{SS(on)} TYP	I _S
23V	2.45mΩ@4.5V	13A
	2.50mΩ@3.8V	
	2.85mΩ@3.1V	
	3.40mΩ@2.5V	



DESCRIPTION

The CJ8508SP uses advanced trench technology to provide excellent R_{SS(ON)}, low gate charge and operation with gate voltages as low as 2.5V while retaining a 12V V_{GS(MAX)} rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

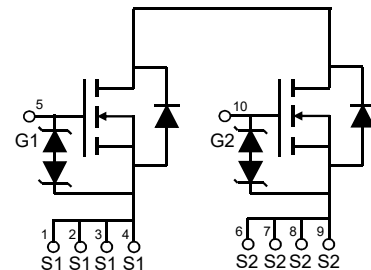
Marking and pin assignment



Marking:

- | | |
|-----------------------|--------------------|
| 1. 8508: Product Code | 1, 2, 3, 4 Source1 |
| 2. YYMMX: Date Code | 6, 7, 8, 9 Source2 |
| 3. Solid dot: Pin 1 | 5 Gate1 |
| | 10 Gate2 |

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V _{SSS}	23	V
Gate-Source Voltage	V _{GSS}	±12	V
Source Current(DC)	I _S ^①	13	A
Source Current (Pulsed)	I _{SP} ^①	130	A
Total Power Dissipation	P _T ^①	3.1	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature Range	T _{STG}	-55 To 150	°C

MOSFET ELECTRICAL CHARACTERISTICS

$T_A=25\text{ }^\circ\text{C}$ unless otherwise specified

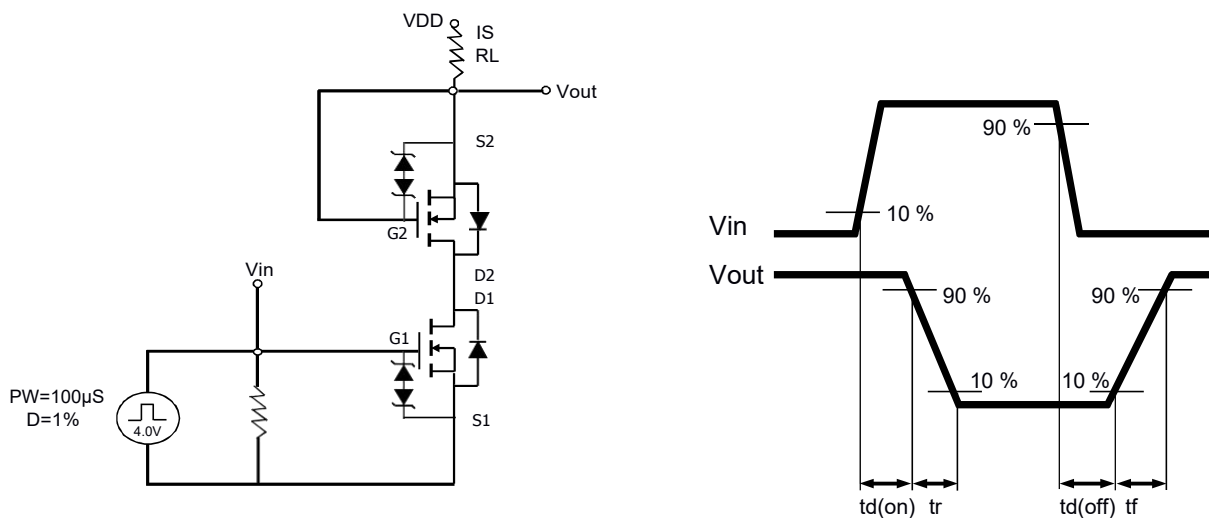
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	$I_S=1\text{mA}, V_{GS}=0\text{V}$	23			V
Zero-Gate Voltage Source Current	I_{SSS}	$V_{SS}=23\text{V}, V_{GS}=0\text{V}$			1.0	μA
Gate to Source Leakage Current	I_{GSS}	$V_{SS}=0\text{V}, V_{GS}=\pm 12\text{V}$			± 10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{SS}=10\text{V}, I_S=1.33\text{ mA}$	0.35	0.90	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=4.5\text{V}, I_S=2.0\text{A}$	1.8	2.45	3.2	$\text{m}\Omega$
		$V_{GS}=3.8\text{V}, I_S=2.0\text{A}$	1.9	2.50	3.45	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=2.0\text{A}$	2.05	2.85	4.5	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=2.0\text{A}$	2.3	3.40	7.6	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}, V_{SS}=10\text{V}, f=1\text{kHz}$		4522		pF
Output Capacitance	C_{oss}			502		pF
Reverse Transfer Capacitance	C_{rss}			451		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10\text{V}, R_L=1.5\Omega, V_{GS}=4.5\text{V}$		1.38		μs
Turn-on Rise Time	t_r			3.52		μs
Turn-off Delay Time	$t_{d(off)}$			8.64		μs
Turn-off Fall Time	t_f			7.40		μs
Total Gate Charge	Q_g	$V_{DD}=10\text{V}, V_{GS}=6\text{V}, I_D=7\text{A}$		63		nC
Gate1-source1 charge	Q_{g1s1}			8.2		nC
Gate1-source2 charge	Q_{g1s2}			15.3		nC
Diode Forward Voltage	$V_{F(S-S)}^{(4)}$	$V_{GS}=0\text{V}, I_S=2\text{A}$			1.0	V

Notes: 1. Mounted on FR4 board (25.4mm×25.4mm×1.0mm) using minimum recommended pad size (36um Copper).

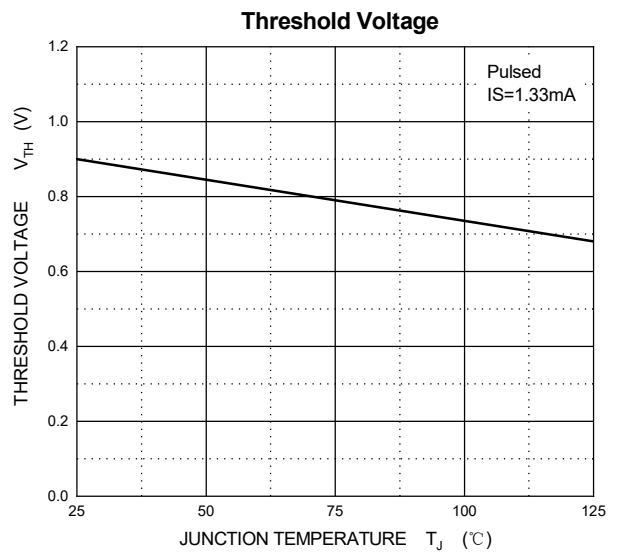
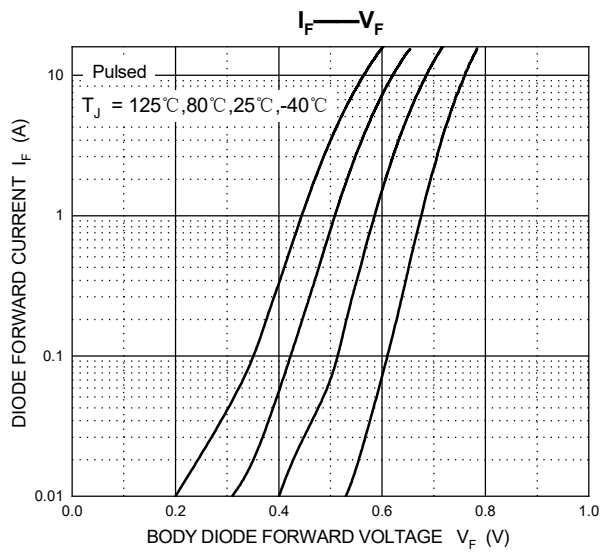
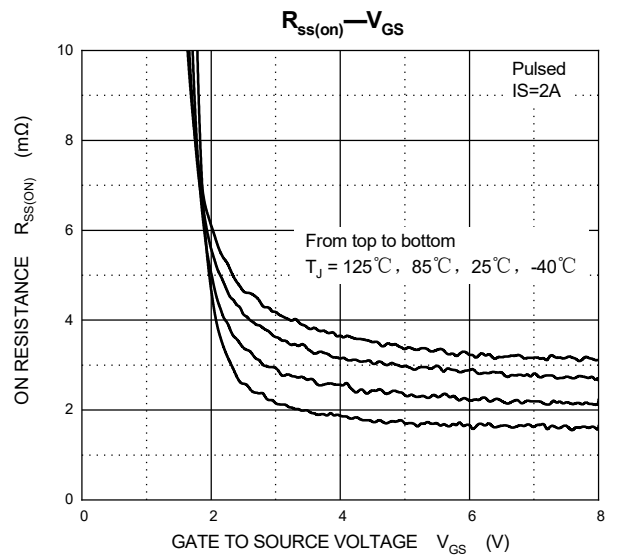
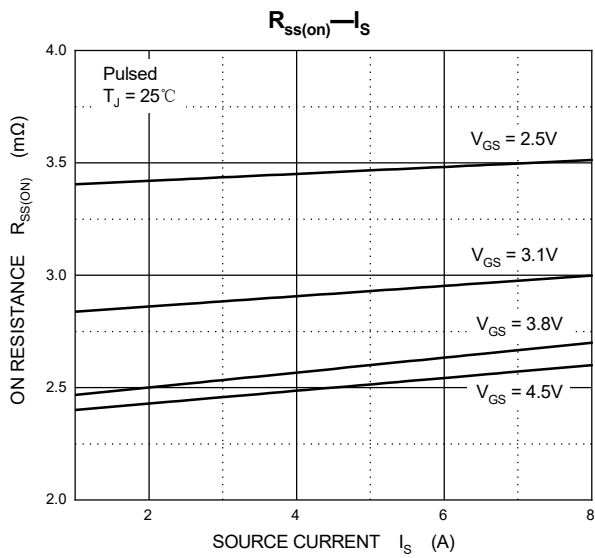
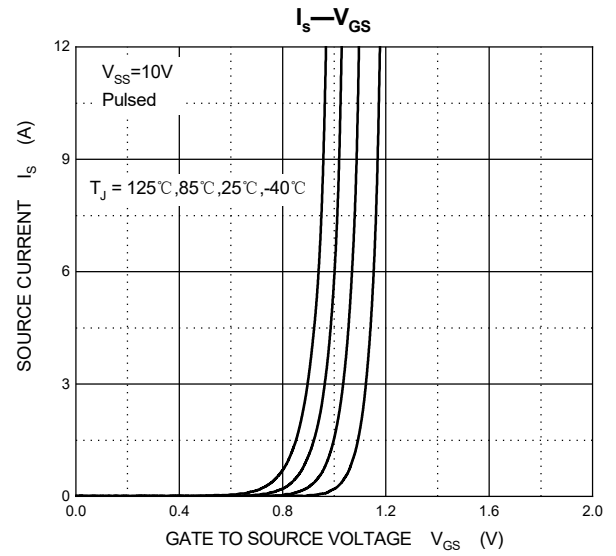
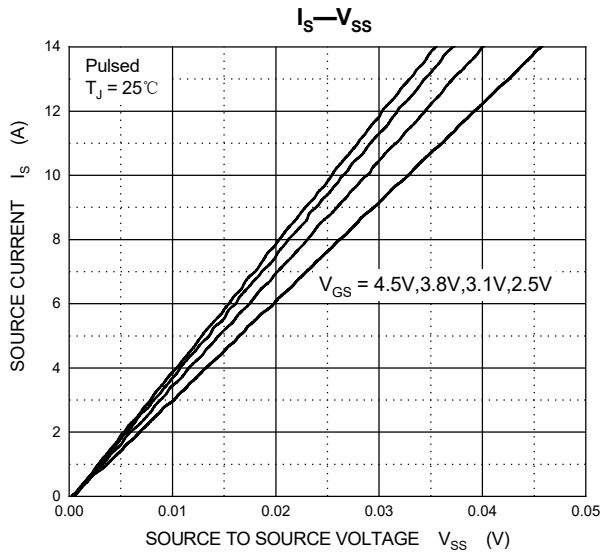
2. $t = 10\text{ }\mu\text{s}$, Duty Cycle = 1 %.

3. When FET1 is measured, G2 and S2 are short-circuited.

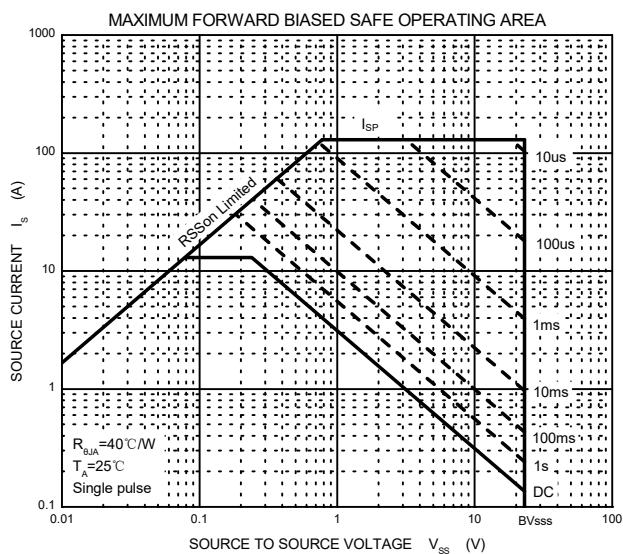
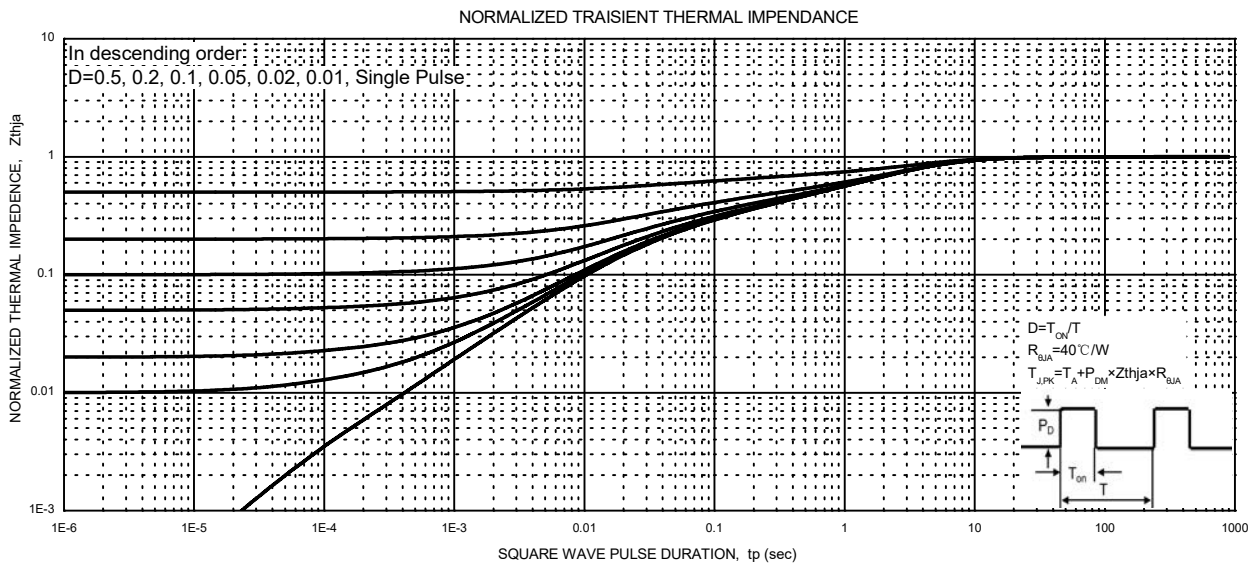
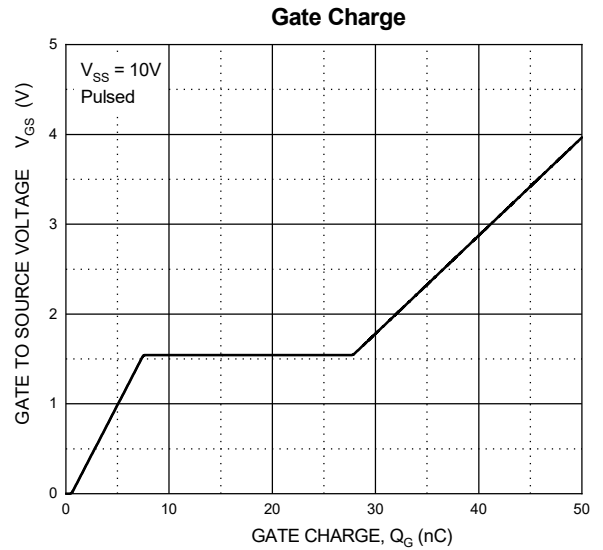
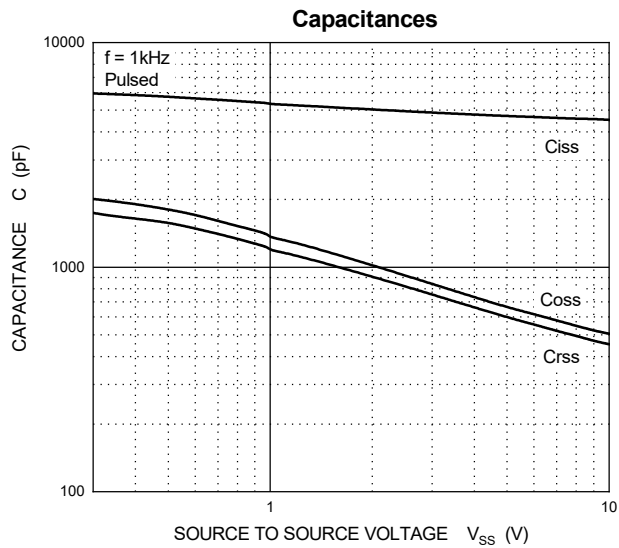
4. When FET1 is measured, G2 and S2 are biased with $V_{G2S2}=4.5\text{V}$.



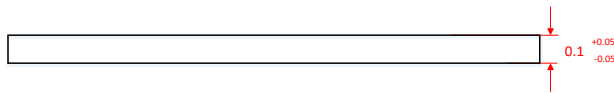
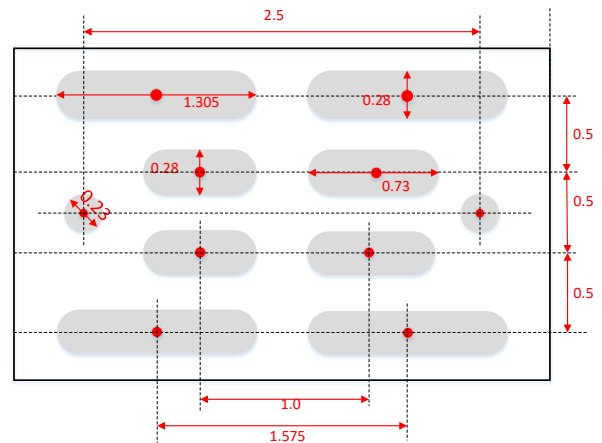
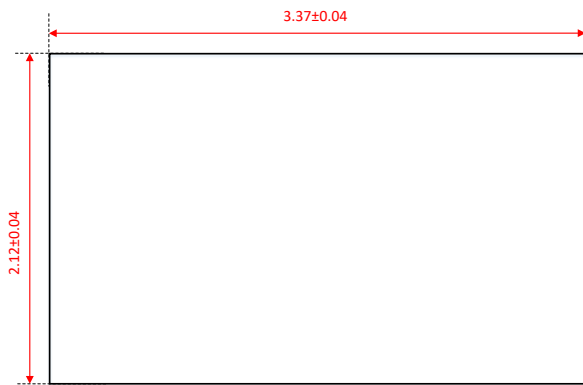
Typical Characteristics



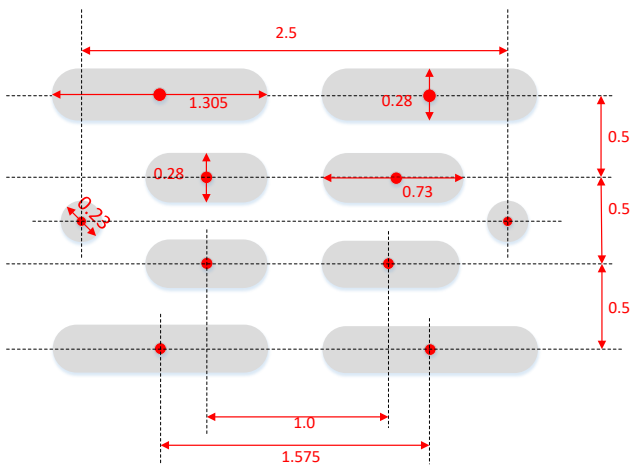
Typical Characteristics



CSPC3421-10 Package Outline Dimensions(Unit:mm)



CSPC3421-10 Suggested Pad Layout (Unit:mm)

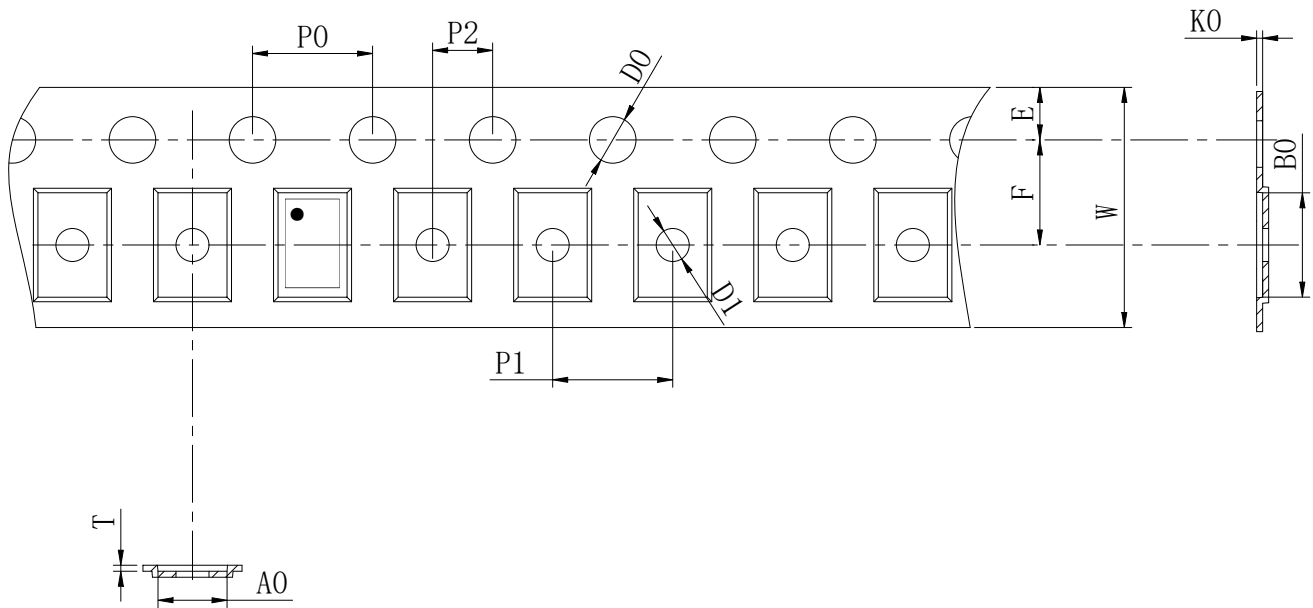


- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.050 mm.
 3. The pad layout is for reference purposes only.

NOTICE

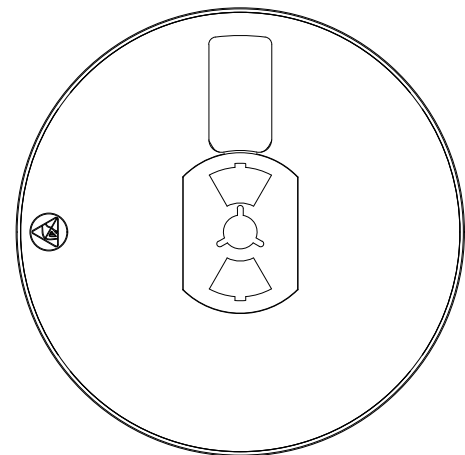
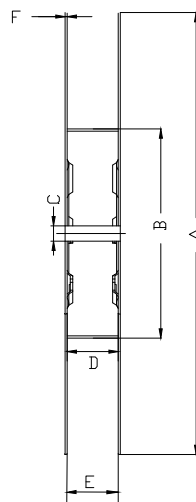
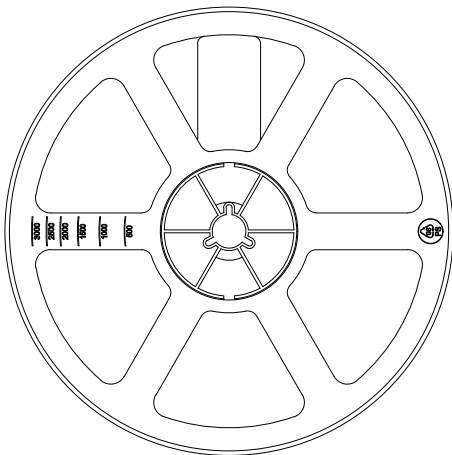
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Tape and Reel



产品尺寸规格(UNT:mm)

规格	W	P1	E	F	D0	D1
尺寸	8.00±0.15	4.00±0.10	1.75±0.10	3.50±0.05	1.55±0.10	1.10±0.10
规格	A0	B0	K0	T	P0	P2
尺寸	2.30±0.05	3.48±0.05	0.20±0.05	0.20±0.02	4.00±0.10	2.00±0.05



SIZE	8MM
A	178±2.0
B	55±1.0
C	13.0 ^{+0.35} _{-0.15}
D	8.4 ^{+2.5} _{-0.4}
E	8.65 ^{+4.7} _{-0.65}
F	1.5±0.5

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