10V, 1.2A Ultra Low IQ Synchronous Step-Down Converter

CJ92110 DCDC

1 Introduction

The CJ92110 is a 450nA Ultra Low quiescent current step-down converter with fully integrated low on resistance high-side and low-side power MOSFETs. The CJ92110 can deliver 1.2A of output current efficiently with constant on time (COT) control for fast loop response.

The CJ92110 achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

The CJ92110 has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, output over/under voltage protection and thermal shutdown in case of excessive power dissipation. The CJ92110 is available in a space-saving DFNWB2x3-8L package.

2 Available Packages

PART NUMBER	PACKAGE
CJ92110	DFNWB2x3-8L

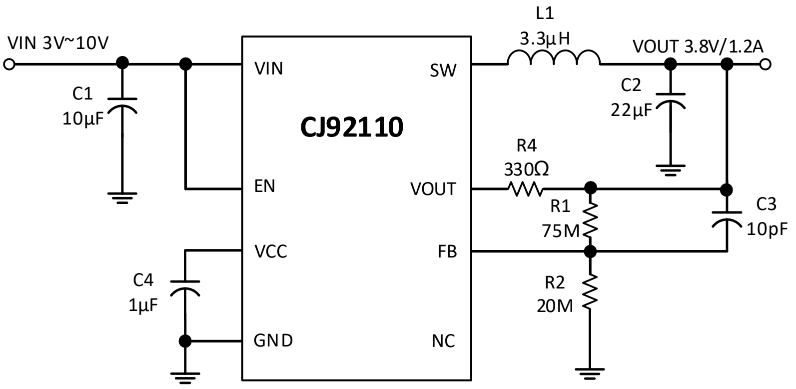
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide 3V to 10V Input Range
- 290mΩ/115mΩ Power MOSFET
- 450nA Ultra Low Quiescent Current at 5V Input
- Constant On Time Control for Fast Loop Response
- 0.85MHz Switching Frequency
- Support 100% Duty Cycle for Low Dropout Mode with 3.2μA Quiescent current at 3.8VIN
- Internal 2ms Soft Start
- Output Voltage Adjustable from 0.8V to 5V
- MSL 1 Moisture Sensitivity Level
- EN Shutdown Output Discharge
- Support Pre-Biased Output Startup
- Full Protection, Over Current Protection and Hiccup, Output Over/Under Voltage Protection, Over Temperature Protection

4 Applications

- NBIOT Module
- Gas Meter and Water Meter
- Single or Multi Cell Li-Ion Battery System
- Multi-Cell Dry Battery Systems



Typical Application

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ92110-DIN	DFNWB2x3-8L	-40~125°C	RoHS & Green	Level 1 Unlimited	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

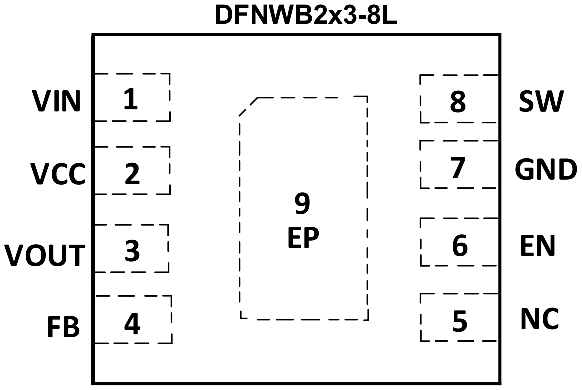


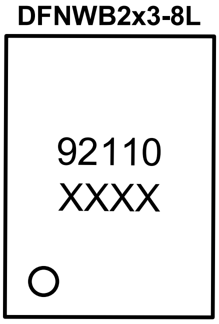
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I/O[1]	DESCRIPTION
No.	NAME		
1	VIN	I	**Supply Input Pin.** VIN supplies the internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
2	VCC	P	**Internal LDO Output for Control and Driver.** Decouple with a minimum 1μF ceramic capacitor as close to VCC as possible.
3	VOUT	O	**Output Feedback Terminal.** Connect this pin to output with a 330Ω resistor.
4	FB	I	**Feedback Input to the Converter.** Connect a resistor divider to set the output voltage.
5	NC	-	**Not Connection.**
6	EN	I	**Enable Pin.** Do not float. High = on, Low = off. Can be tied to VIN directly. Precision enable input allows adjustable UVLO by external resistor divider.
7	GND	G	**Power Ground Terminal.**
8	SW	O	**Switching Output of the Convertor.** Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
9	EP	G	**Exposed Pad.** Connect exposed pad to the PCB GND plane to achieve good thermal performance.

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



92110: Device number.
XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

T_{amb}=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{IN}	VIN to GND	-	-0.3	12	V
V_{SW}	SW to GND	-	-0.7(-5V in 10ns)	V_{IN}+0.7	V
V_{EN}	EN to GND	-	-0.3	12	V
All Other Pins		-	-0.3	6	V
T_{STG}	Storage temperature	-	-65	150	°C
T_J	Junction temperature	-	-40	150	°C

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are not tested at manufacturing.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EN}	EN to GND	-	3	-	10	V
V_{IN}	VIN to GND	-	3	-	10	V
V_{OUT}	VOUT to GND	-	0.8	-	5	V
I_{OUT}	Max continuous output current	-	-	1.2	-	A
T_J	Junction temperature	-	-40	-	125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±2000	V
$V_{ESD-CDM}$	Electrostatic discharge	Charged device model	±1000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

SYMBOL	THERMAL METRIC	RATING	UNIT
$R_{ΘJC}$	Junction to case thermal resistance	10	°C/W
$R_{ΘJA}$	Junction to ambient thermal resistance	40	°C/W

7.5 Electrical Characteristics

V_{IN}=5V, V_{EN}=5V, T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input UVLO and Quiescent Current						
VIN_{UVR}	VIN UVLO rising threshold	-	-	2.85	-	V
VIN_{UV_hys}	VIN UVLO hysteresis	-	-	0.11	-	V
I_{QS}	Shutdown supply current	V_{EN} < 0.3V V_{IN} = 5V	-	40	-	nA
I_Q	Quiescent supply current at no switching	No switching; V_{IN} = 5V	-	450	-	nA
$I_{Q\_100\%}$	Quiescent supply current at 100% duty	V_{IN} = 3.8V;100% duty	-	3.2	-	μA
Enable Threshold						
V_{EN_R}	Enable rising threshold	Low to high	1.35	-	-	V
V_{EN_F}	Enable falling threshold	High to low	-	-	0.4	V
Feedback Voltage and Soft-start Time						
V_{FB}	Feedback voltage	-	0.788	0.8	0.812	V
T_{SS}	Soft-start time	V_{OUT} from 0% to 100%	-	2	-	ms
High Side and Low Side MOSFETs						
R_{ON_HS}	High-side switch on resistance	-	-	290	-	mΩ
R_{ON_LS}	Low-side switch on resistance	V_{IN} = 5V	-	115	-	mΩ
LKG_{HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V	-	-	0.1	μA
LKG_{LS}	Low-side leakage	V_{EN} = 0V, V_{SW} = 5V	-	-	0.1	μA
Current Limit						
I_{LIMIT_LS}	Low-side current limit	-	-	1.6	-	A
Output UVP						
V_{UVP}	V_{OUT} UVP threshold	UVP trigger for 1us enter hiccup	-	25%	-	V_{OUT}
Output OVP						
V_{OVP}	V_{OUT} OVP threshold	-	-	113%	-	V_{OUT}
Switching Frequency						
F_{SW}	Oscillator frequency	Work at CCM mode	-	0.85	-	MHz
T_{ON_MIN}	Minimum switch on time(1)	-	-	150	-	ns
T_{OFF_MIN}	Minimum switch off time(1)	-	-	80	-	ns
D_{MAX}	Maximum duty cycle	-	-	100	-	%
T_{OTP_R}	Thermal shutdown(1)	-	-	160	-	°C
T_{OTP_Hys}	OTP hysteresis(1)	-	-	25	-	°C

(1) Guaranteed by design and engineering sample characterization.

8 Detailed Description

8.1 Overview

The CJ92110 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on-period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on-period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS- FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on-period or the LS-FET off and HS-FET on-period.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

8.2 Functional Block Diagram

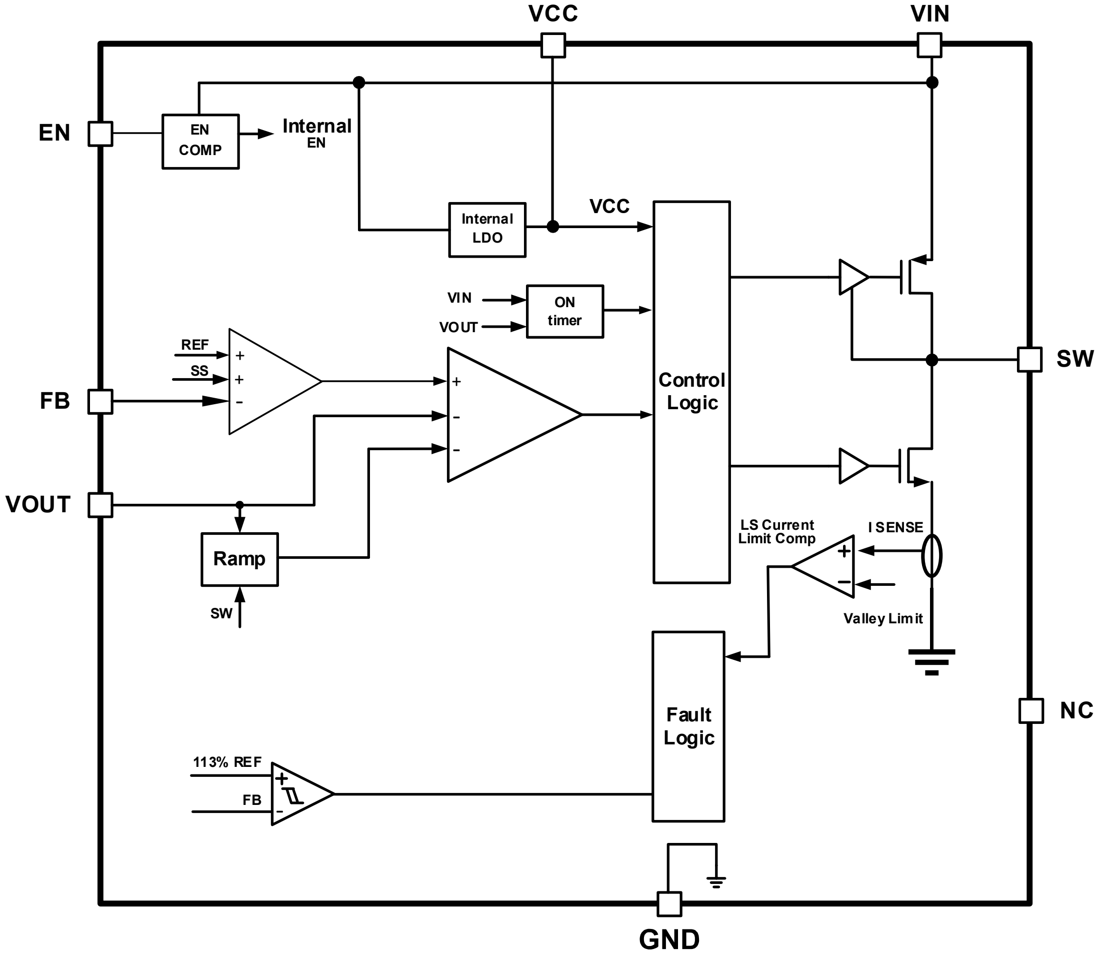


Figure 8-1 Function Block Diagram

8.3 Feature Description

8.3.1 Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 8-2). When feedback voltage is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period begins

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

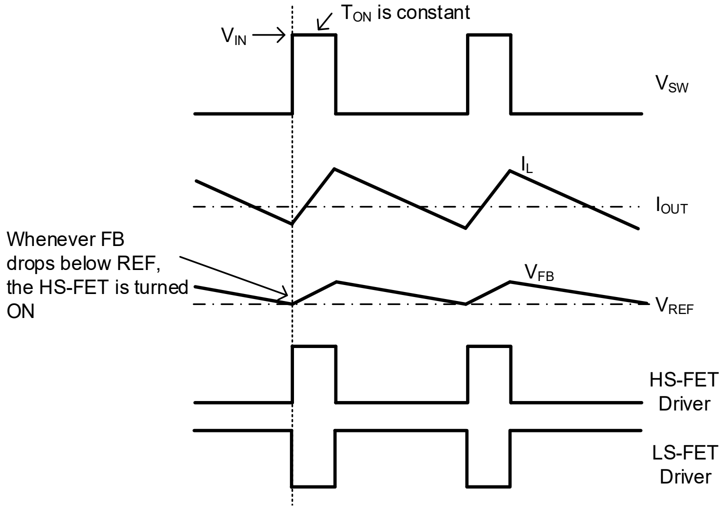


Figure 8-2 Heavy-Load Operation

8.3.2 Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 8-3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on- timer. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The LS-FET driver enters tri-state (Hi-Zi) whenever the inductor current reaches zero. As a result, the efficiency in light-load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

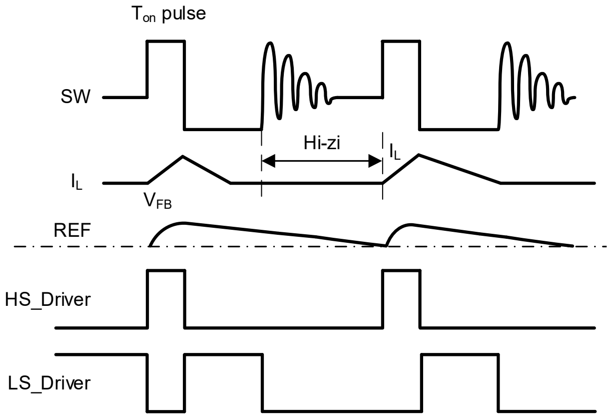


Figure 8-3 Light-Load Operation

8.3.3 Sleep Mode Operation

To decrease the consumption current of system, CJ92110 can work sleep mode at ultra-light load. As the output current decreases from the light-load to ultra-light load, the switching frequency will be lower and lower, which means switching pulse interval time will be longer than longer, whenever the pulse interval time (Hi-Zi period) is longer than 5μs, CJ92110 will work in sleep mode. During sleep mode, most of blocks will be turned off except the PWM compactor.

8.3.4 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The CJ92110 UVLO comparator monitors the input voltage. The UVLO rising threshold is 2.85V(typically), while its falling threshold is consistently 2.74V.

8.3.5 EN Control

EN is used to enable or disable the entire chip. Drive EN high (>1.35V typically) to turn on the regulator. Pull EN low(<0.4V) to turn off the regulator. Do not float EN. For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. To determine the automatic start-up voltage, calculate the values of the pull-up resistor (R_{UP} from VIN to EN) and the pull-down resistor (R_{DOWN} from EN to GND) with Equation (1):

$$VIN\_start = \frac{1.35V \times (R_{UP} + R_{DOWN})}{R_{DOWN}} \tag{1}$$

8.3.6 Soft Start (SS)

The CJ92110 employs a soft-start (SS) mechanism to ensure a smooth output during power-up. When EN rises high, the internal reference voltage ramps up gradually, and the output voltage ramps up smoothly as well. The soft-start time is 2ms typically.

8.3.7 Pre-Bias Start-Up

The CJ92110 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the voltage on the soft start is charged as well, IC will not switch. Once the soft-voltage is above the biased voltage, CJ92110 will switch normally.

8.3.8 VCC Regulator

A 5V(normally) integrated regulator powers most of the internal control circuits. Decouple 1μF ceramic capacitor as close to VCC pin as possible. This regulator takes power from VIN terminal and VCC voltage will be decreased when VIN is lower than 5V.

8.3.9 100% Duty Operation

When CJ92110 will automatically extend the frequency to support the application when VIN is close to VOUT. The frequency extend circuit will be triggered when Toff min time is reached. The CJ92110 can support up to 100% maximum duty cycle once V_{FB} is lower than internal V_{REF}.

8.3.10 Output Discharge

The CJ92110 involves a discharge function that provides a passive discharge path for the external output capacitor. The function is active when the CJ92110 is in EN disable mode. When EN is disabled, the HS-FET turns off, and the LS-FET turns on until inductor current reaches 0A then an internal 50Ω resistor will be connected to the SW pin to discharge the output capacitor for 10ms period.

8.3.11 Over-Current Protection (OCP) and Short Circuits Protection

The CJ92110 has a cycle-by-cycle over-current limiting control (OCL). The current-limit circuit employs a valley current-sensing algorithm. The part uses the RDS(ON) of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the device enters over-current protection mode, High Side FET will not allow to turn on until the valley current limit is removed. Meanwhile the output voltage will drop.

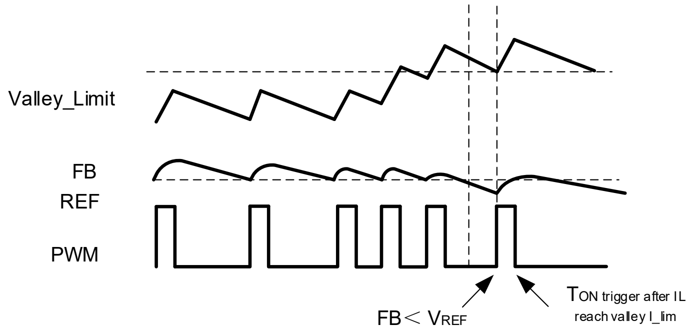


Figure 8-4 Valley current-limit control

When Feedback voltage drops below 25% of internal V_{REF}, the CJ92110 enters the hiccup mode to restart the part periodically. The hiccup duty cycle is very small to reduce power dissipation during short-circuit conditions. During OCP, the device attempts to recover from the over-current fault with hiccup mode. This means that the chip disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the over-current condition still remains when the soft start elapses, the device repeats this operation.

8.3.12 VOUT Over Voltage Protection

Once output voltage is over 113% of internal V_{REF} which is the over voltage threshold, CJ92110 will turn off both High side and Low Side MOSFETs. Meanwhile, IC will exist sleep mode and the CJ92110 will enter Output over-voltage discharge mode, the quiescent current will be increased. When output voltage falls below over voltage threshold, the CJ92110 starts to switch normally.

8.3.13 Thermal Shutdown

Thermal shutdown is employed in the CJ92110. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off. This is a non-latched protection. There is a hysteresis of about 25°C. Once the junction temperature drops to about 135°C, a soft start is initiated.

9 Application Information

9.1 Setting the Output Voltage

The CJ92110 output voltage can be set by an external resistor divider between VOUT and GND. To minimize the Output Voltage leakage consumption at light load, highly recommend use large resistor for the FB divider. See the Figure 9-1 and Table 1 to setup output voltage.

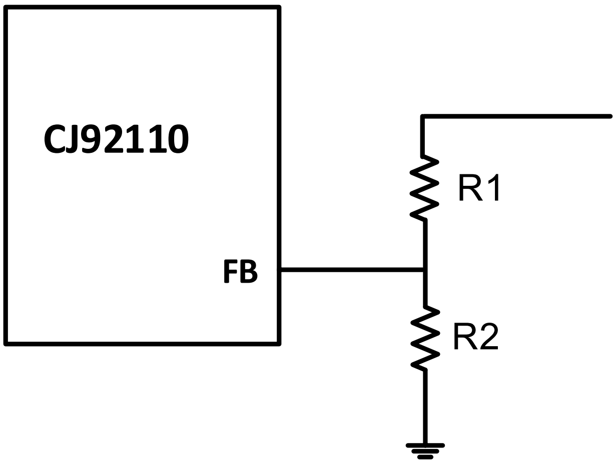


Figure 9-1 Output Voltage Configuration Circuits

The Output Voltage can be calculated by the following formula, the reference voltage is 0.8V.

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{\mathrm{R2}}) \tag{2}$$

Recommended parameters for typical output application as table 1 shown.

Table 1: Recommended Parameters for typical V_{OUT} applications

V_{IN} (V)	V_{OUT} (V)	R1 (MΩ)	R2 (MΩ)	C3 (pF)	L (µH)	C_{IN} (µF)	C_{OUT} (µF)
6	5	105	20	10	3.3~4.7	10	22
	4.1	82.5	20	10	3.3~4.7	10	22
	3.8	75	20	10	2.2~3.3	10	22
	3.3	62.5	20	10	2.2	10	22
	1.9	27.5	20	10	2.2	10	22
	1.2	10	20	10	2.2	10	22
8.4	5	105	20	10	4.7	10	22
	4.1	82.5	20	10	4.7	10	22
	3.8	75	20	10	3.3~4.7	10	22
	3.3	62.5	20	10	3.3~4.7	10	22
	1.9	27.5	20	10	2.2~3.3	10	22
	1.2	10	20	10	2.2~3.3	10	22

9.2 Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 60% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}} \tag{3}$$

Where ΔI_L is the inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \tag{4}$$

9.3 Selecting Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the stepdown converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations. The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$C_{IN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \tag{5}$$

The worst case occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \tag{6}$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{7}$$

Under worse-case is where $V_{IN} = 2V_{OUT.}$

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \tag{8}$$

9.4 Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right) \tag{9}$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor, F_{OSC} is the switching frequency. Note that, in real application, should consider that the ceramic capacitor capacitance has derating.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple caused by ESR is very small. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{8 \times F_{OSC} \times C_{OUT}}\right) \tag{10}$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \tag{11}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The CJ92110 can be optimized for a wide range of capacitance and ESR values.

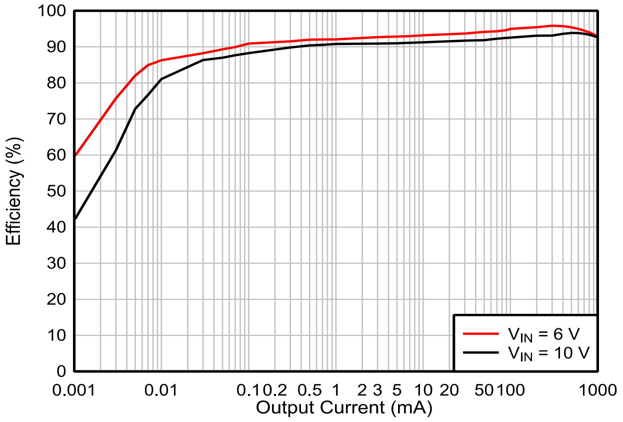
Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can’t reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{OUT_MAX} can be limited approximately by:

$$C_{OUT\_MAX} = (I_{limitave} - I_{OUT}) \times \frac{T_{SS}}{V_{OUT}} \tag{12}$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period, T_{ss} is the soft-start time (2ms typically).

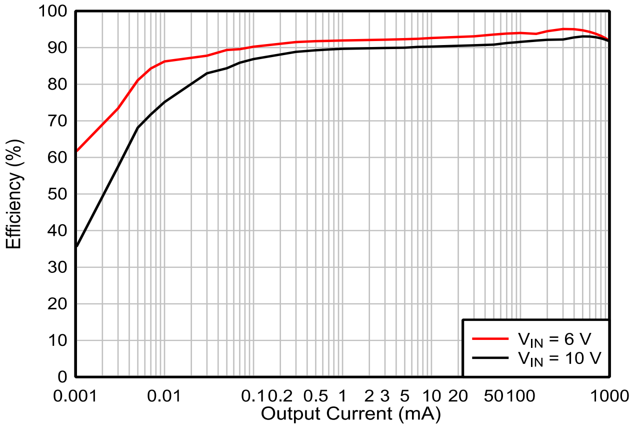
9.5 Typical Performance Characteristics

V_{IN} = 6V, V_{OUT} = 3.8V, C_{IN}=10μF, C_{OUT} =22μF, L1 = 3.3μH, and T_A = +25°C, unless otherwise noted.



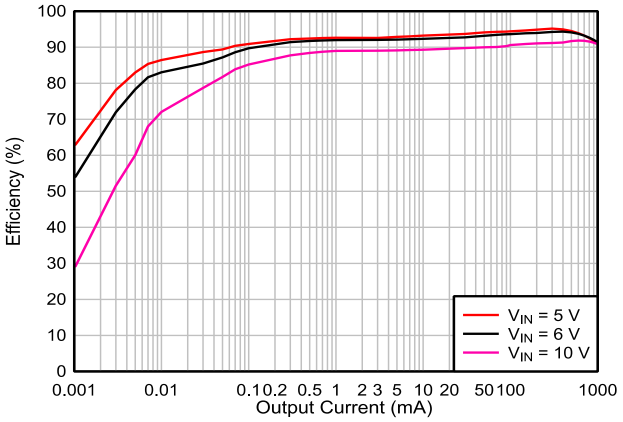
Efficiency vs. Load current

(V_{OUT}=5V, L=4.7μH, DCR=34mΩ)



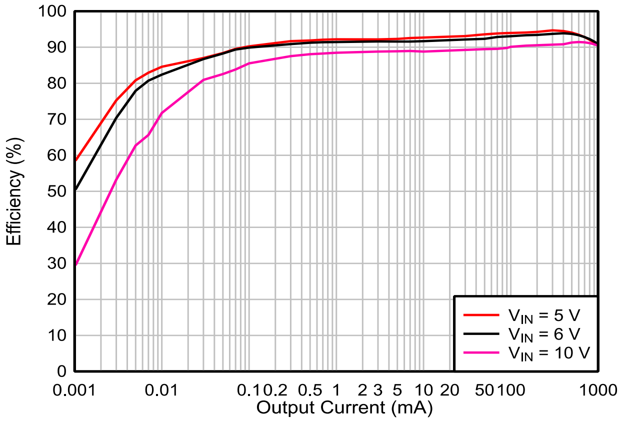
Efficiency vs. Load current

(V_{OUT}=4.1V, L=4.7μH, DCR=34mΩ)



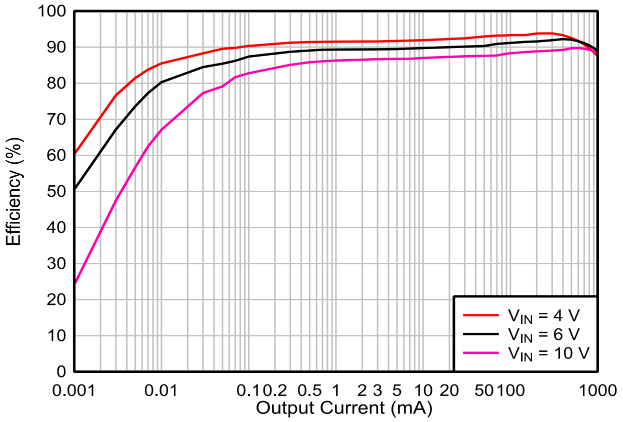
Efficiency vs. Load current

(V_{OUT}=3.8V, L=3.3μH, DCR=22mΩ)



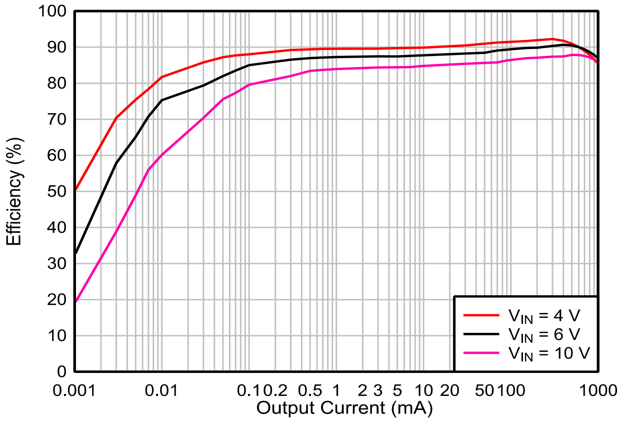
Efficiency vs. Load current

(V_{OUT}=3.3V, L=3.3μH, DCR=22mΩ)



Efficiency vs. Load current

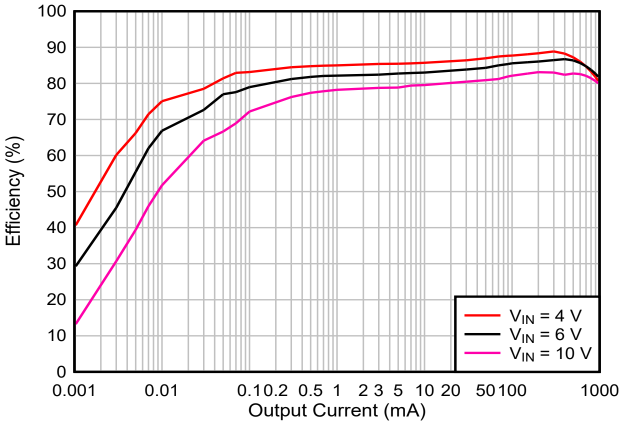
(V_{OUT}=2.5V, L=3.3μH, DCR=22mΩ)



Efficiency vs. Load current

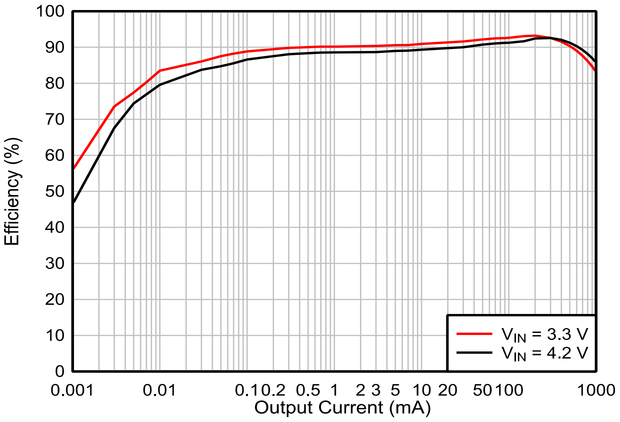
(V_{OUT}=1.9V, L=3.3μH, DCR=22mΩ)

V_{IN} = 6V, V_{OUT} = 3.8V, C_{IN}=10µF, C_{OUT} =22µF, L1 = 3.3µH, and T_A = +25°C, unless otherwise noted.



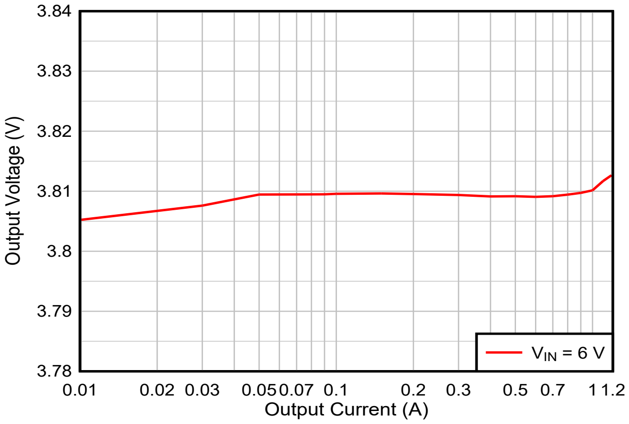
Efficiency vs. Load current

(V_{OUT}=1.2V, L=3.3µH, DCR=22mΩ)



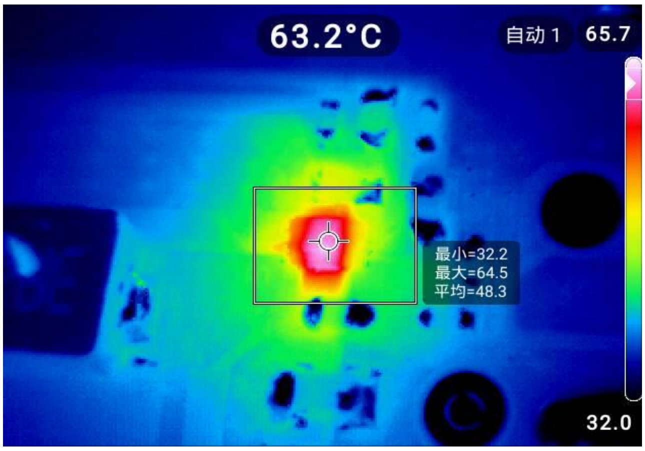
Efficiency vs. Load current

(V_{OUT}=1.9V, L=4.7µH, DCR=34mΩ)



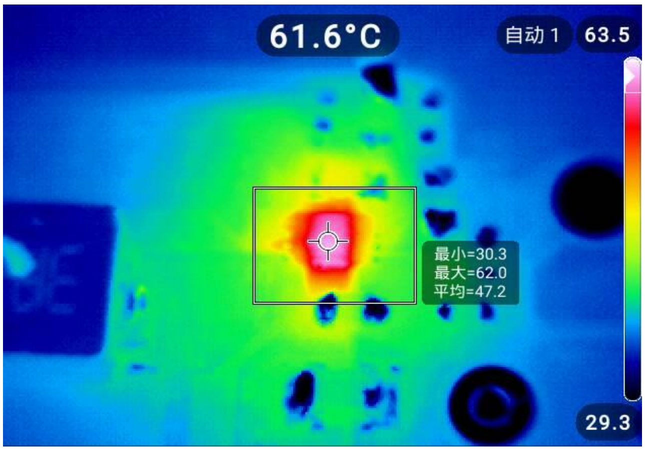
Load regulation

(V_{OUT}=3.8V, L=3.3µH, DCR=22mΩ)



Temperature

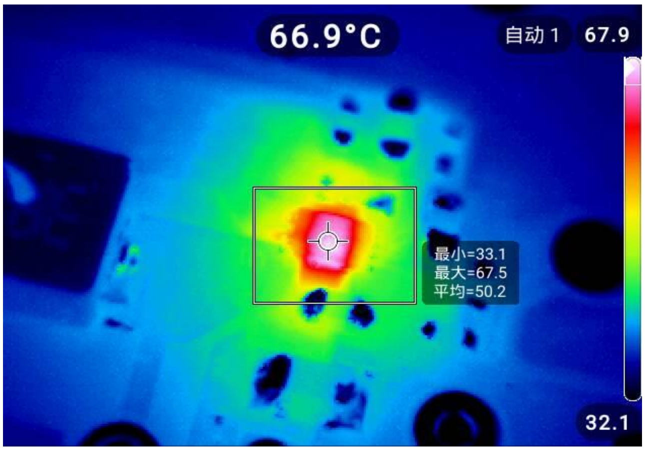
(V_{IN} =10V, V_{OUT} =3.8V, L=3.3µH)



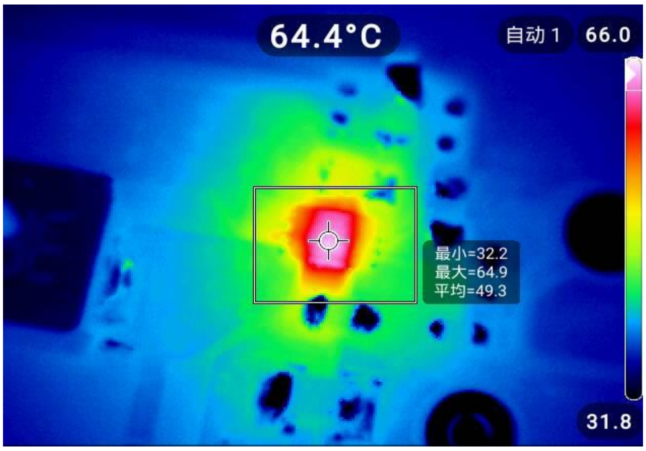
Temperature

(V_{IN} =10V, V_{OUT} =3.3V, L=3.3µH)

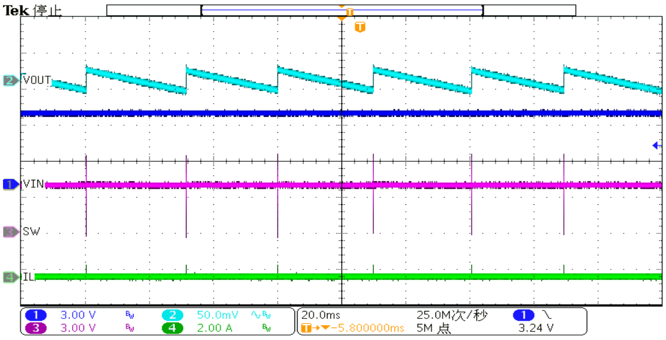
V_{IN} = 6V, V_{OUT} = 3.8V, C_{IN}=10µF, C_{OUT} =22µF, L1 = 3.3µH, and T_A = +25°C, unless otherwise noted.



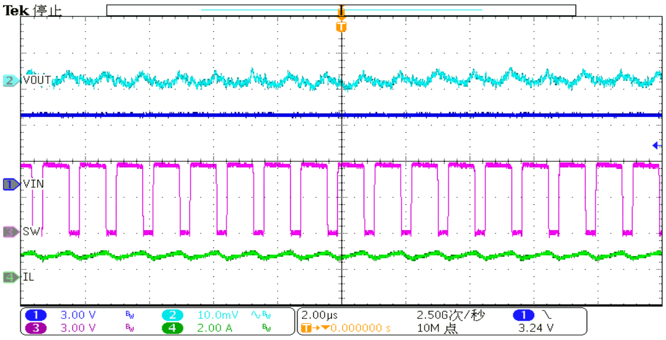
Temperature
(V_{IN} =6V, V_{OUT} =3.8V, L=3.3µH)



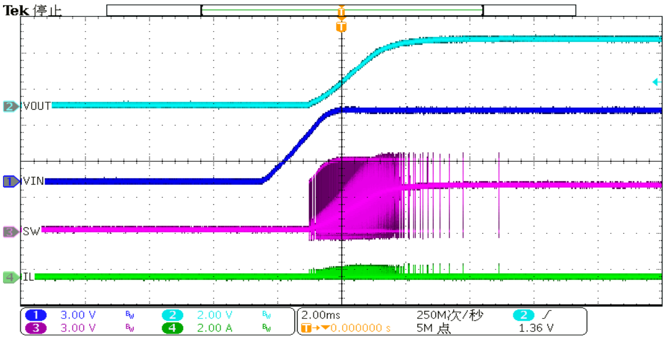
Temperature
(V_{IN} =6V, V_{OUT} =3.3V, L=3.3µH)



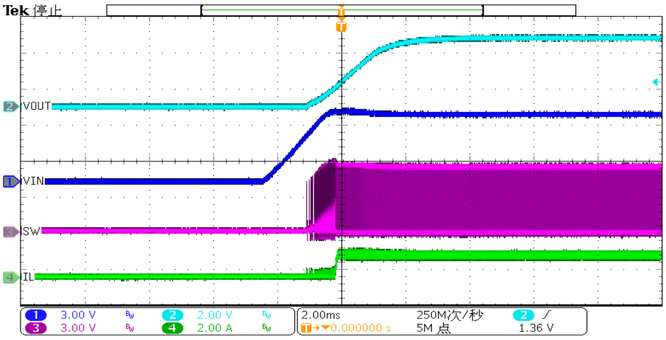
Output voltage ripple (I_{OUT}=0A)



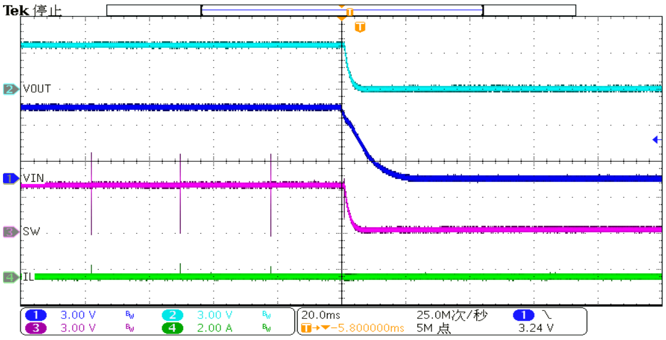
Output voltage ripple (I_{OUT}=1.2A)



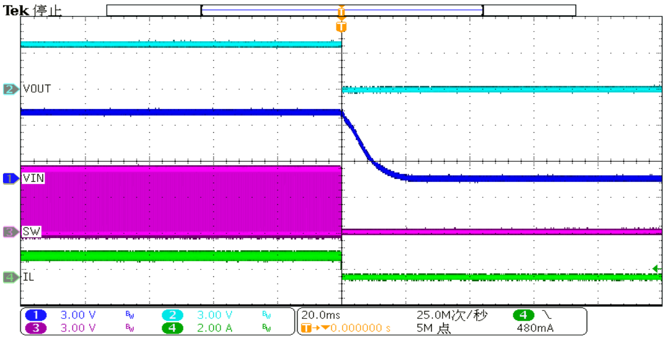
Start-Up through VIN (I_{OUT}=0A)



Start-Up through VIN (I_{OUT}=1.2A)

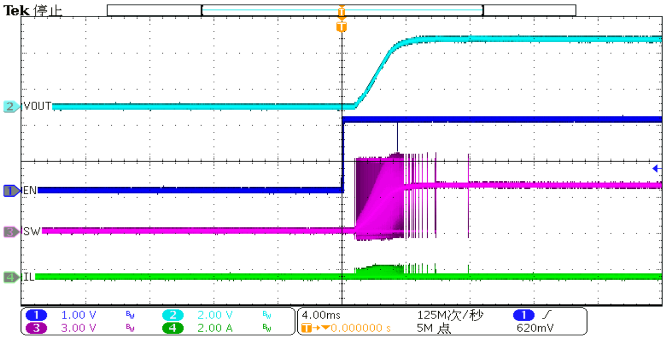


Shutdown through VIN (I_{OUT}=0A)

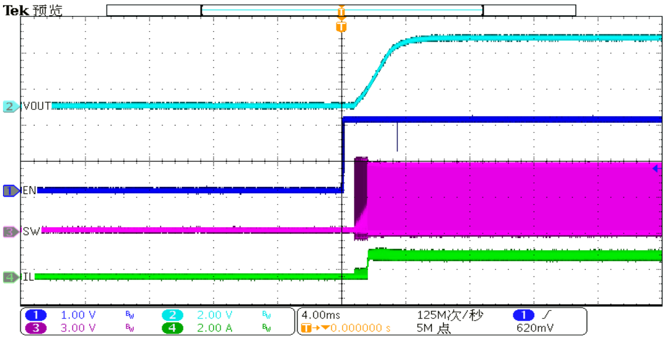


Shutdown through VIN (I_{OUT}=1.2A)

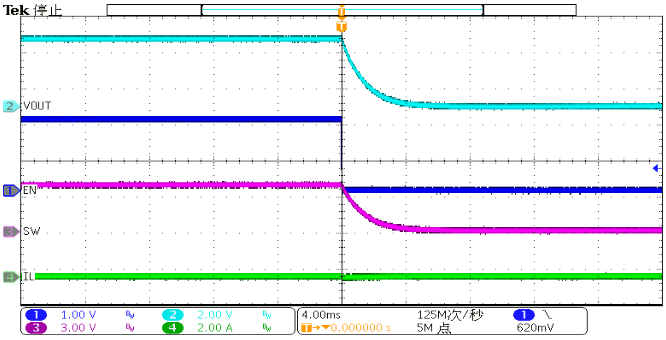
V_{IN} = 6V, V_{OUT} = 3.8V, C_{IN}=10μF, C_{OUT} =22μF, L1 = 3.3μH, and T_A = +25°C, unless otherwise noted.



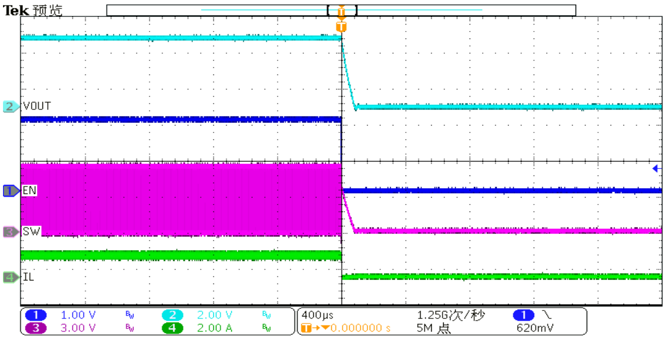
Start-Up through EN (I_{OUT}=0A)



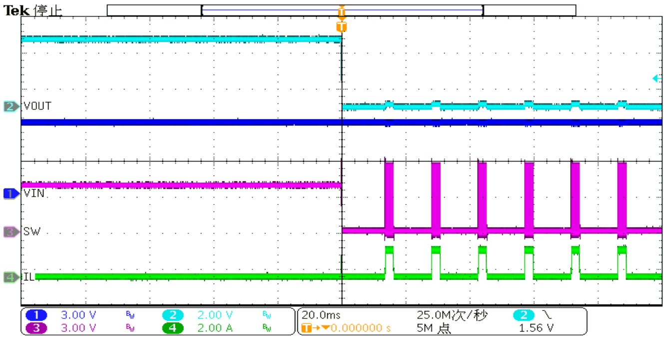
Start-Up through EN (I_{OUT}=1.2A)



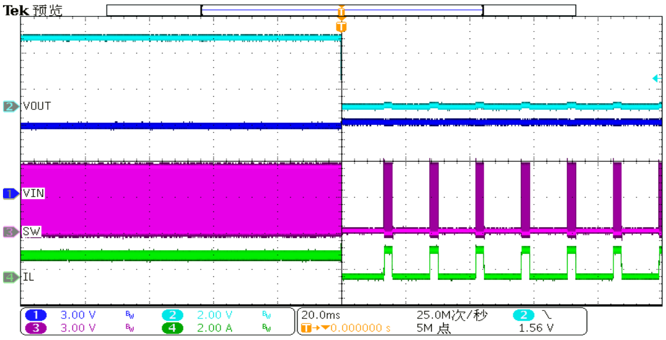
Shutdown through EN (I_{OUT}=0A)



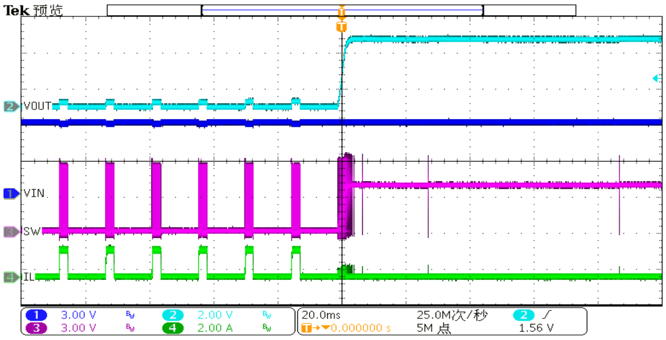
Shutdown through EN (I_{OUT}=1.2A)



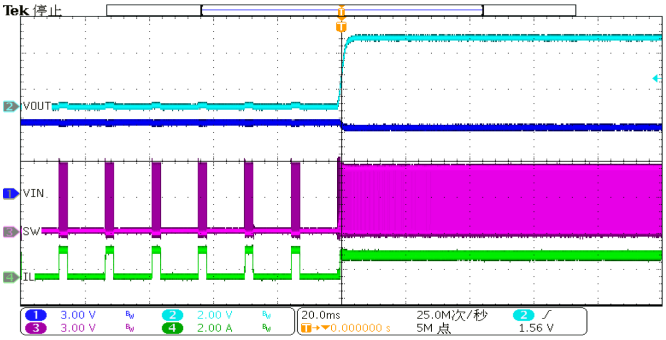
Short entry (I_{OUT}=0A)



Short entry (I_{OUT}=1.2A)

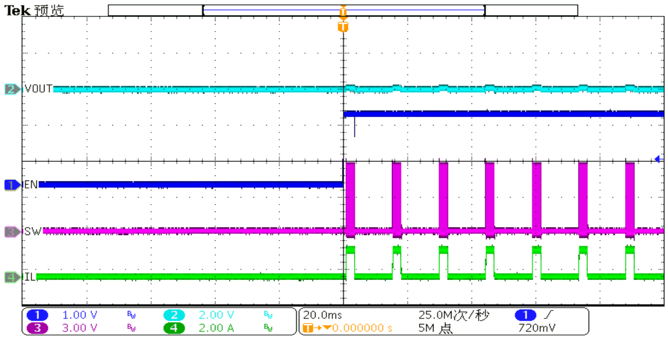


Short recovery (I_{OUT}=0A)

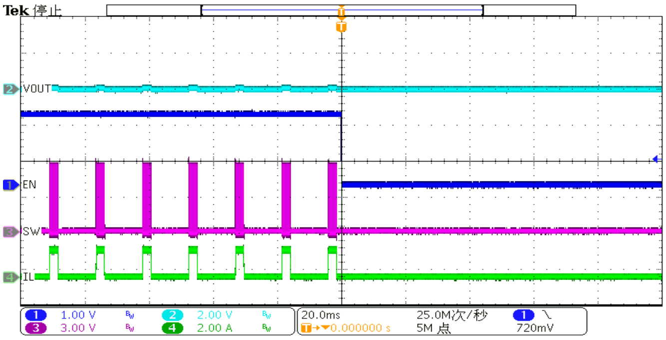


Short recovery (I_{OUT}=1.2A)

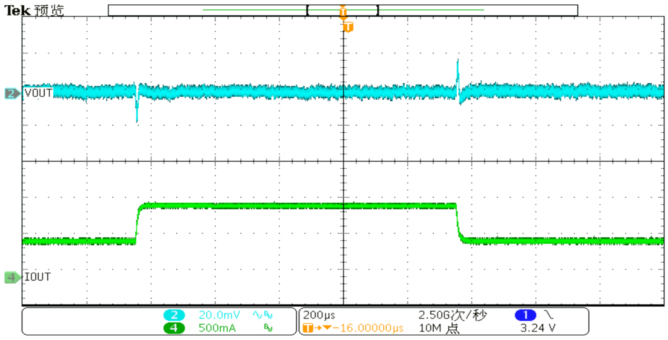
V_{IN} = 6V, V_{OUT} = 3.8V, C_{IN}=10μF, C_{OUT} =22μF, L1 = 3.3μH, and T_A = +25°C, unless otherwise noted.



Short EN Start-Up (V_{OUT}=GND)



Short EN shutdown(V_{OUT}=GND)



Transient
(I_{OUT}=500mA to 1A, L=3.3μH)

10 Layout

10.1 Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below and take figures as the reference.

- The high current paths (GND, VIN and SW) should be placed very close to the device with short, direct and wide traces.
- Place the input capacitor as close to VIN and GND as possible.
- Place the VCC bypass capacitor as close to VCC as possible.
- Keep the switching node (such as SW) far away from the Vout sense network.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

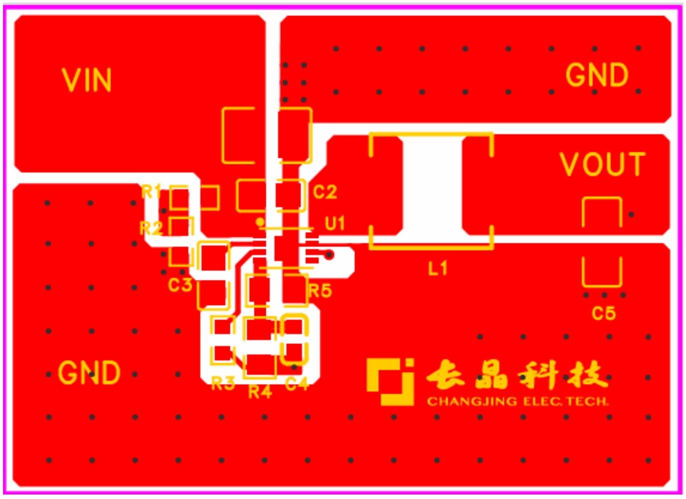


Figure 10-1 Recommend PCB Layout-Top Layer

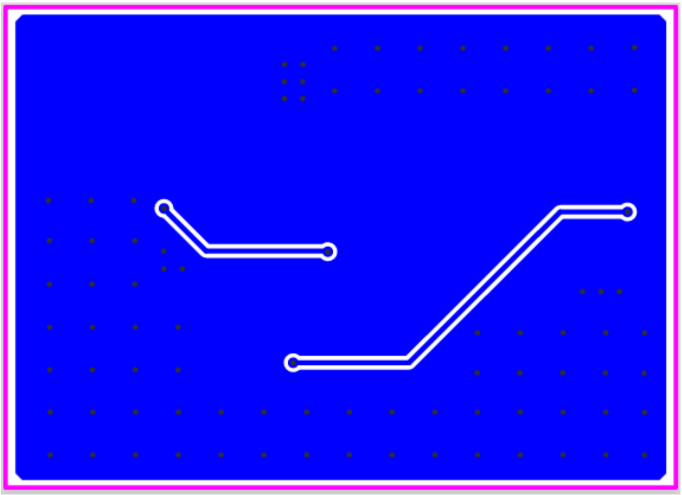


Figure 10-2 Recommend PCB Layout-Bottom Layer

11 Tape and Reel Information

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below and take figures as the reference.

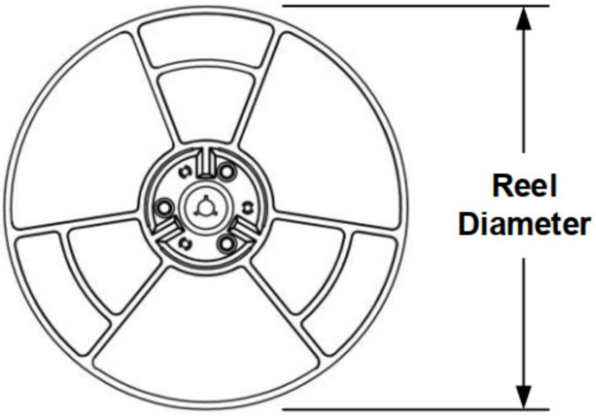


Figure 11-1 Reel Dimension

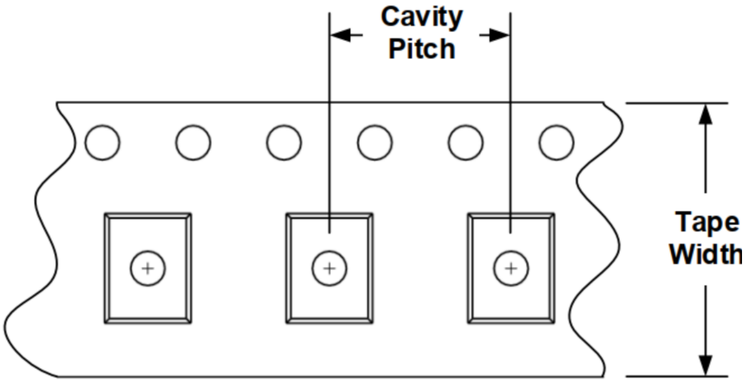
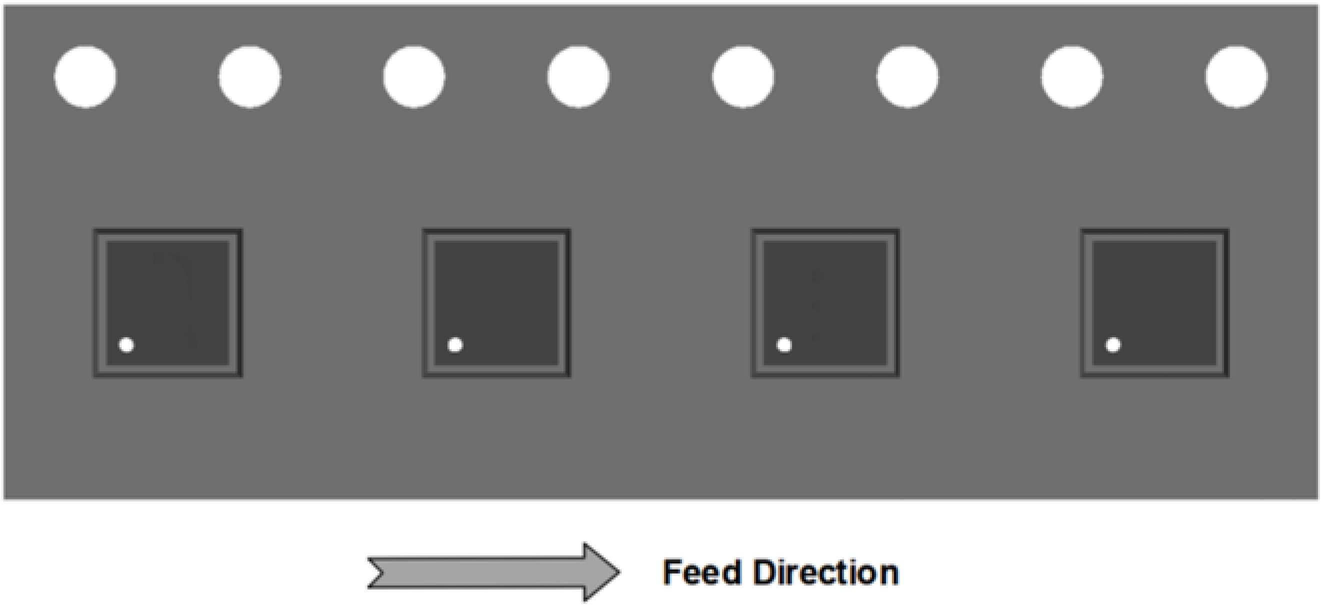


Figure 11-2 Tape Dimension



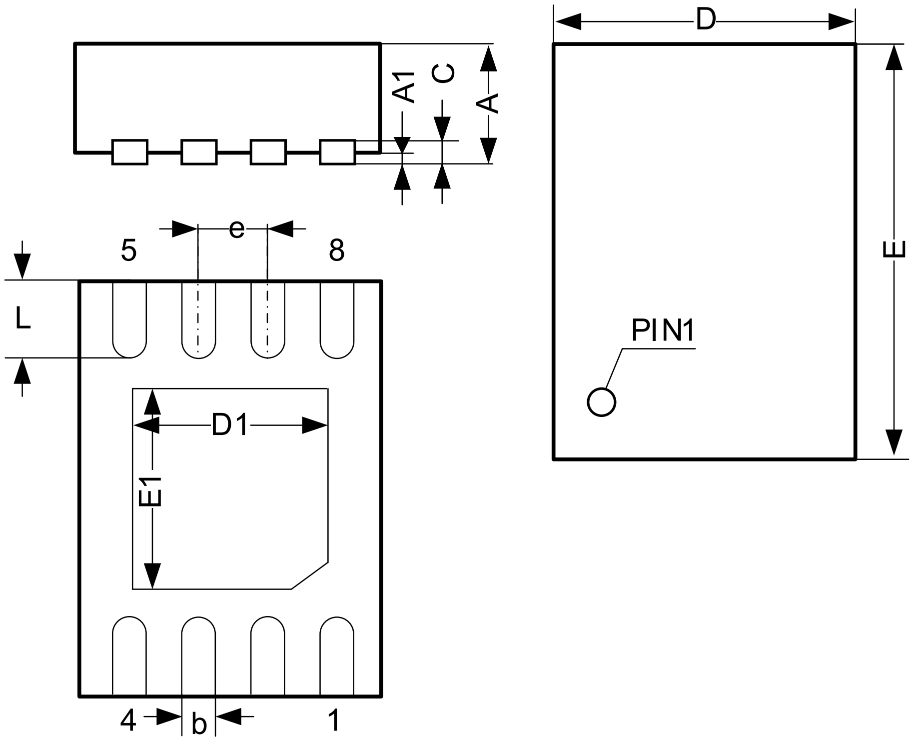
The picture is only used to provide the reference for PIN1 positioning in the carrier pocket, the appearance of the IC is subject to the real thing.

DEVICE	PACKAGE	SPQ	Reel Diameter (inch)	Tape Width (mm)	Cavity Pitch (mm)
CJ92110-DIN	DFNWB2x3-8L	4000	7	8	4

12 Mechanical Information

12.1 DFNWB2x3-8L Mechanical Information

12.1.1 DFNWB2x3-8L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.00	0.03	0.05
b	0.15	0.25	0.35
c	0.152 REF		
D	1.90	2.00	2.10
D1	1.40	1.50	1.60
E	2.90	3.00	3.10
E1	1.30	1.40	1.50
e	0.50 BSC		
L	0.30	0.40	0.50
Unit: mm			

13 Notes and Revision History

13.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

13.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

13.3 Revision History

August, 2025: rev - 1.1, Change the package name.

September, 2025: rev - 1.2, Change the Typical Application diagram.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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