30V, 4A, 350kHz, Synchronous, DC/DC Step-Down Converter

CJ92340 DC/DC Regulator

1 Introduction

The CJ92340 device is an easy-to-use synchronous step-down Buck. Which integrated low on resistance high-side and low-side power MOSFETs. The CJ92340 can deliver 4A of output current efficiently with constant on time (COT) control for fast loop response.

This CJ92340 device achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

This CJ92340 device has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuits protection, FB open short protection and thermal shutdown in case of excessive power dissipation. The CJ92340 is available in a space-saving ESOP8L package.

2 Available Packages

PART NUMBER	PACKAGE
CJ92340	ESOP8

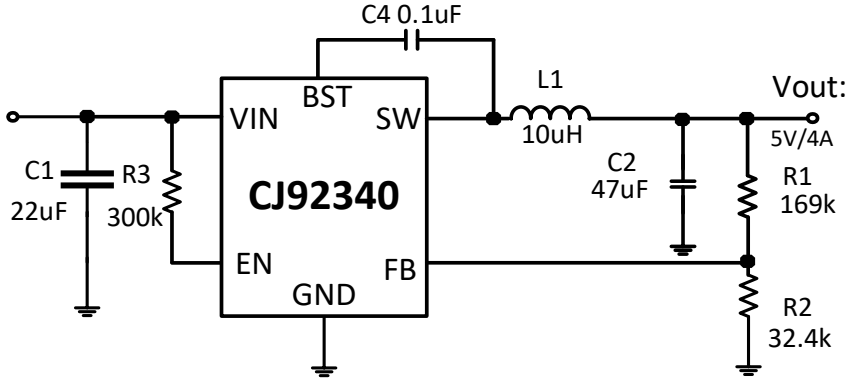
3 Features

- 4.5V to 30V Wide Input Range
- 4A Continuous Output Current
- 85mΩ /55mΩ Internal Power MOSFETs
- 185uA Low Quiescent Current
- Constant On Time Control for Fast Loop Response
- 350kHz Switching Frequency
- Support Up to 98% Large Duty Cycle
- Internal Soft Start
- Output Voltage adjustable from 0.8V
- Support Pre-Biased Output Startup
- Full Protection, Over Current Protection and Hiccup, Output Over Voltage Protection, FB Open Short Protection, Over Temperature Protection

4 Applications

- Robots
- Home Appliance and Whitegoods
- Multi-functional Printer
- Automotive
- Industrial Control

Typical Application



Typical Application Circuit

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ92340-PBN	ESOP8	-40 ~ 125°C	RoHS & Green	Level 1	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

ESOP8

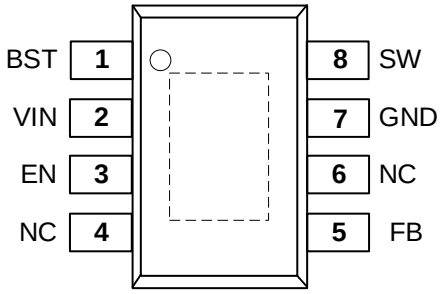


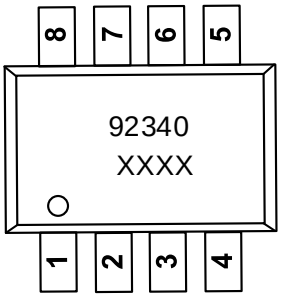
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I / O(1)	DESCRIPTION
No.	NAME		
1	BST	G	**Bootstrap**. Connect a capacitor between SW and BST pins to form a floating supply across the High-side switch driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
2	VIN	P	**Supply input Pin**. VIN supplies power for the internal MOSFET and regulator. The input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
3	EN	P	**Enable Pin**. Drive EN Pin High to enable IC, otherwise float or pull down EN to disable IC. EN pin Can be tied to VIN by a resistor. Precision enable input allows adjustable UVLO by external resistor divider.
4, 6	NC	I	Not Connected.
5	FB	I	**Feedback input to the convertor.** Connect a resistor divider to set the output voltage.
7	GND	P	**Power Ground terminal.**
8	SW	P	**Switching output of the convertor**. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
9	EP	G	**Exposed Pad.** Connect exposed pad to the PCB GND plane to achieve good thermal performance.

(1) I – Input; O – Output; P – Power; G - GND

6.3 Marking Information



"92340": Device code.
"XXXX": Date Code.

7 Specifications

7.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified) (1)

SYMBOL	DEFINITION	VALUE	UNIT
VIN	VIN to GND	-0.3 ~ 31	V
SW	SW to GND	-0.7(-5V in 10ns) to VIN+ 0.7	V
EN	Max Input current to EN pin	100(2)	uA
BST	BST to SW	-0.3 ~ 6	V
All other pins		-0.3 ~ 6	V
T_{STG}	Storage temperature	-55 ~ 150	°C
T_j	Junction temperature	-40 ~ 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) For details on Ens ABS max rating, please refer to the Enable Control section.

7.2 Recommended Operating Conditions

SYMBOL	DEFINITION	RATING	UNIT
BST	BST to SW	4~5	V
V_{IN}	V_{IN} to GND	4.5~30	V
V_{OUT}	V_{OUT} to GND	0.8 ~ 0.98 x VIN or VOUT<25	V
I_{OUT}	Max continuous Output Current	4	A

7.3 ESD Ratings

SYMBOL	DEFINITION	VALUE	UNIT
HBM	Human body model	±2000	V
CDM	Charged device mode	±1500	

7.4 Thermal Information

SYMBOL	DEFINITION	RATING	UNIT
$R_{\Theta JC(TOP)}$	Junction-to-case(top) thermal resistance	7(1)	°C/W
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	45(1)	°C/W
$R_{\Theta JC(TOP)}$	Junction-to-case(top) thermal resistance	52(2)	°C/W
$R_{\Theta JC(BOT)}$	Junction-to-case(bottom) thermal resistance	2.3(2)	°C/W
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	48(2)	°C/W

(1) Measured on DEMO board 2-layer 1Oz PCB, 63mmx48mm board.

(2) Measured on JESD51-7, 4-layer PCB, and PCB has no copper for thermal dissipation, Normal PCB with copper, thermal resistance will be smaller.

7.5 Electrical Characteristics

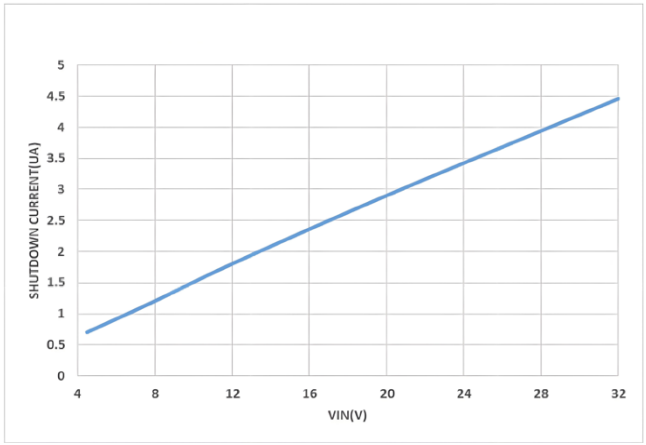
VIN=12V, V_{EN}=2V, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input UVLO and Quiescent Current						
VIN_{UVR}	VIN UVLO rising threshold		4.2	4.28	4.35	V
VIN_{UVF}	VIN UVLO falling threshold		3.8	3.9	4	V
VIN_{UV_hys}	VIN UVLO hysteresis			0.38		V
I_{QS}	Shutdown supply current	V_{EN} < 0.3V, V_{IN}=12V		1	3	uA
I_Q	Quiescent supply current	V_{IN}=12V, No load, V_{FB} = 0.83V, no switching		185		uA
High Side and Low Side MOSFETs						
LKG_{HS}	High-side leakage	V_{EN}=0V, V_{SW}=0V			1	uA
LKG_{LS}	Low-side leakage	V_{EN}=0V, V_{SW}=31V			1	uA
R_{ON_HS}	High-Side Switch on resistance	V_{BST-SW} = 5V		85		mΩ
R_{ON_LS}	Low-Side Switch on resistance	V_{IN} = 12V		55		mΩ
Feedback Voltage and SS						
V_{FB}	Feedback voltage	Ta=25°C	786	798	810	mV
I_{LK_FB}	Feedback leakage	V_{EN} = 1V, V_{FB} = 2V			0.1	uA
T_{SS}	Soft-Start time	V_{FB} from 0% to 100%		2.4		ms
Switching Frequency						
fsw	Oscillator frequency			350		kHz
Current Limit						
I_{Valley}	Low-Side Current limit	V_{OUT}=0V		4.5		A
ZCD				160		mA
Enable						
V_{EN_R}	EN Rising Threshold	Low to High	1.1	1.2	1.3	V
V_{EN_F}	EN falling Threshold	High to Low	0.88	0.98	1.08	V
V_{EN_Hys}	EN Threshold Hysteresis			0.22		V
R_{EN}	Enable input resistor			1500		kΩ
T_{ON_MIN}(1)	Minimum on time			60		ns
D_{MAX}	Max duty cycle			98		%
VOUT OVP/UVP threshold						
FB_{OVP}	Rising			110		%
FB_{UVP}				30		%
T_{OTP_R}(1)	Thermal shutdown(1)			160		°C
T_{OTP_Hys}(1)	OTP hysteresis(1)			30		°C
T_{OFF_MIN}(1)	Minimum off time			150		ns

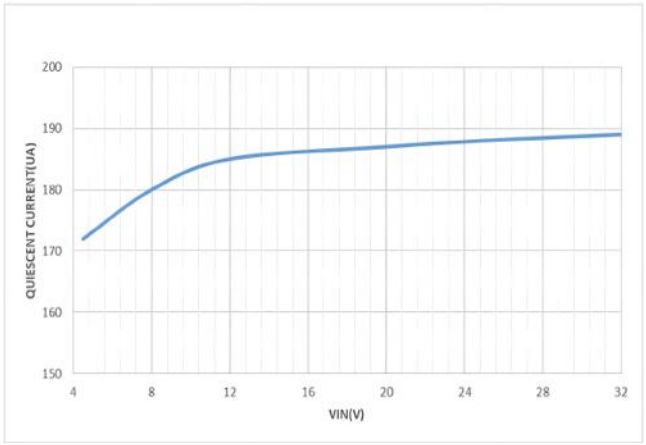
(1) Guaranteed by design

7.6 Typical Characteristics

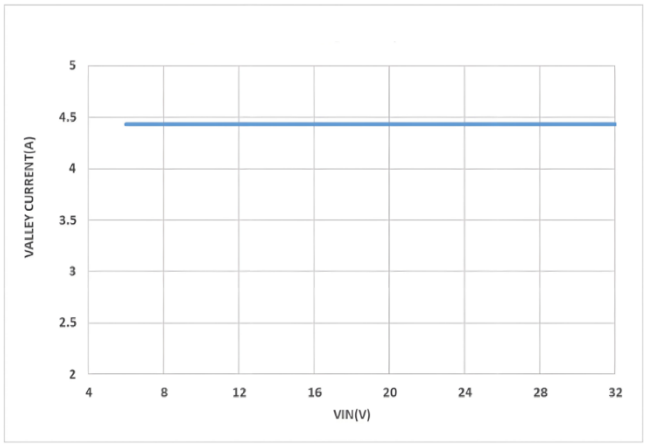
V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22uF, C_{OUT} = 44uF, L1 = 10uH (DCR=26mohm), and T_A = 25°C, unless otherwise noted.



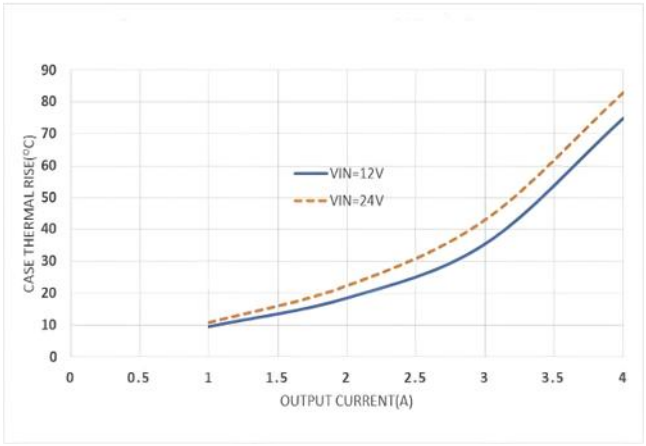
Shutsdown Current



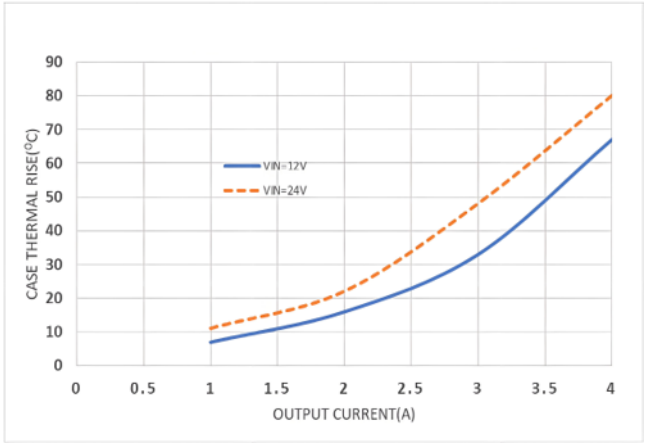
Quiescent Current



Valley Current Limit vs. Input Voltage



Case Temperature Rise vs. Load Current, V_{OUT}=5V



Case Temperature Rise vs. Load Current, V_{OUT}=3.3V

8 Function Description

8.1 Overview

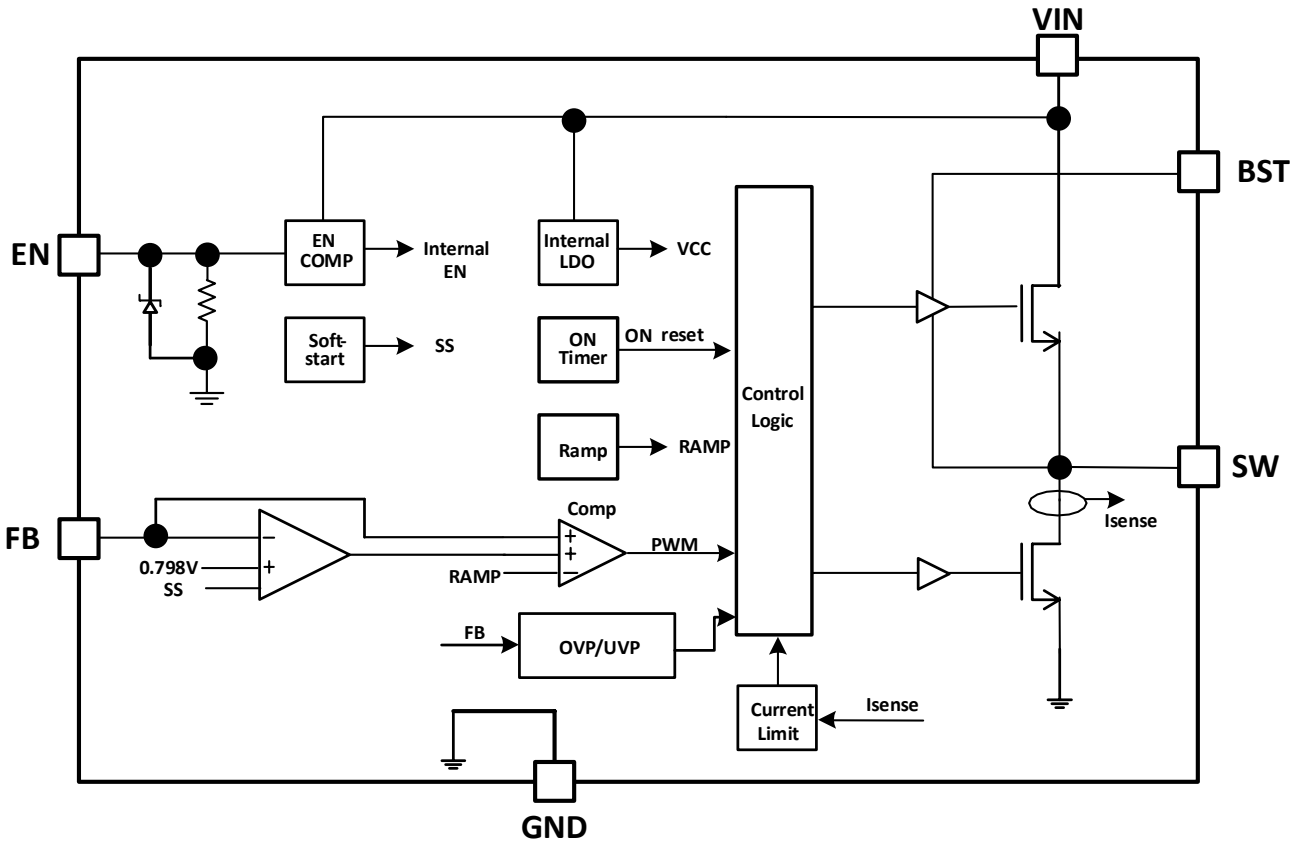


Figure 8-1 Function block diagram

8.2 Pulse-Width Modulation (PWM) Control

The CJ92340 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (VFB) is below the reference voltage (VREF), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when VFB drops below VREF. By repeating operation this way, the converter regulates the output voltage. The integrated low- side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. To avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

With the load decrease, the inductor current decrease too. Once the inductor current touch zero, the operation is transition from continuous-conduction-mode (CCM) to discontinuous- conduction-mode (DCM).

When the CJ92340 works in pulse-frequency modulation (PFM) mode during light-load operation, the CJ92340 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side will be off the CJ92340 enters Hi-zi state. The output

capacitors discharge slowly to GND through R1 and R2. When VFB drops below the reference voltage, the HS-FET is turned on again. This operation improves device efficiency greatly when the output current is low.

8.3 Enable (EN) control

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1.5MΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN is clamped internally using a 5.5V Zener diode. EN can connected to VIN directly by a resistor.

The EN Pin can connect to VIN by a pull-up resistor, but EN input current need below 100uA. For example, if VIN=24V, the I_{Zener}=(24-5.5)/RPULL-UP<100uA, So, $R_{PULL-UP}$>185KΩ.

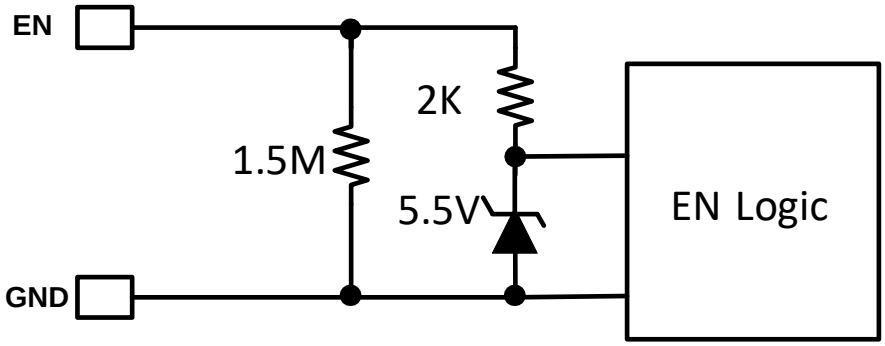


Figure 8-2 Zener Diode between EN and GND

8.4 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The CJ92340 UVLO comparator monitors the input voltage. The UVLO rising threshold is 4.28V(typically), while its falling threshold is consistently 3.9V.

8.5 Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (VSS) that ramps up linearly. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 2.4ms(typically) internally.

8.6 Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The CJ92340 has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the LS limit compactor active. The device enters over current protection mode. High side will not be turned on until the valley current limit disappear. Meanwhile, the output voltage drops until VFB is below the under voltage (UV) threshold (typically 30% of the reference). Once UV is triggered, the CJ92340 enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

8.7 Pre-Bias Start-Up

The CJ92340 is designed for monotonic start-up into pre-biased loads. If the output is pre- biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

8.8 Output OVP and UVP

The CJ92340 monitors a resistor divided VFB to detect over- and under-voltage. When VFB becomes higher than 110%(typically) of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the circuit will turn on the low side MOSFET to discharge the output. LSFET will turn off until the negative current (-2.5A typically) limit is triggered then LSFET will remain off for 5us to turn on again. IC will repeat this behavior until the output OVP condition is removed. When VFB drops below 30%(typically) of VREF, the UVP comparator output goes high, and the CJ92340 enters the hiccup protection.

8.9 Large Duty Cycle Operation

CJ92340 will automatically extend the frequency to support the application when VIN is close to VOUT. The frequency extend circuit will be triggered when Toff min time is reached. The CJ92340 can support up to 98% maximum duty cycle.

8.10 Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

9 Application and Implementation

9.1 Typical Application Circuit

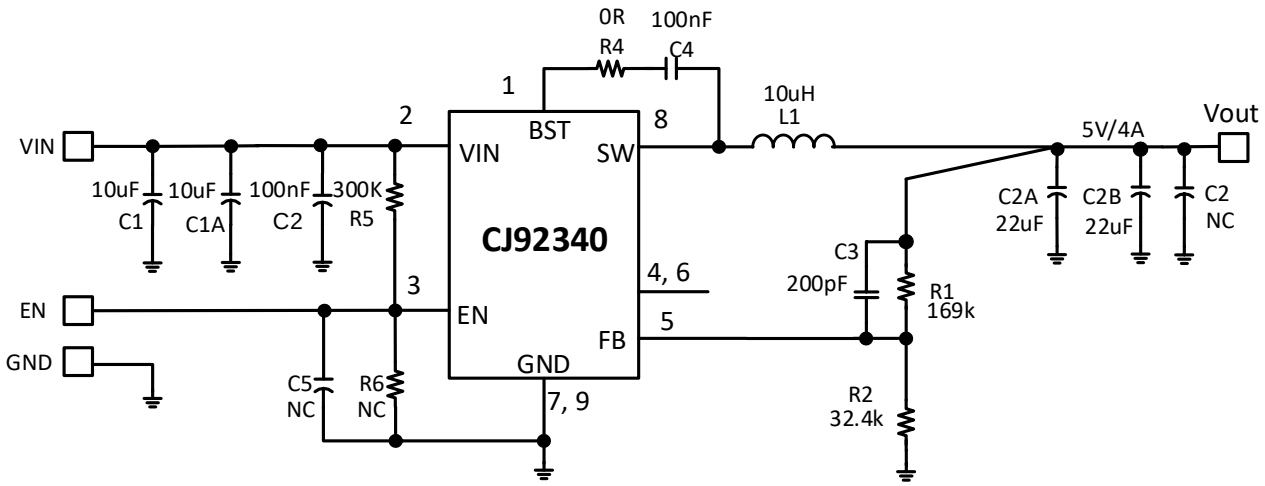


Figure 9-1 Typical VOUT=5V/4A application

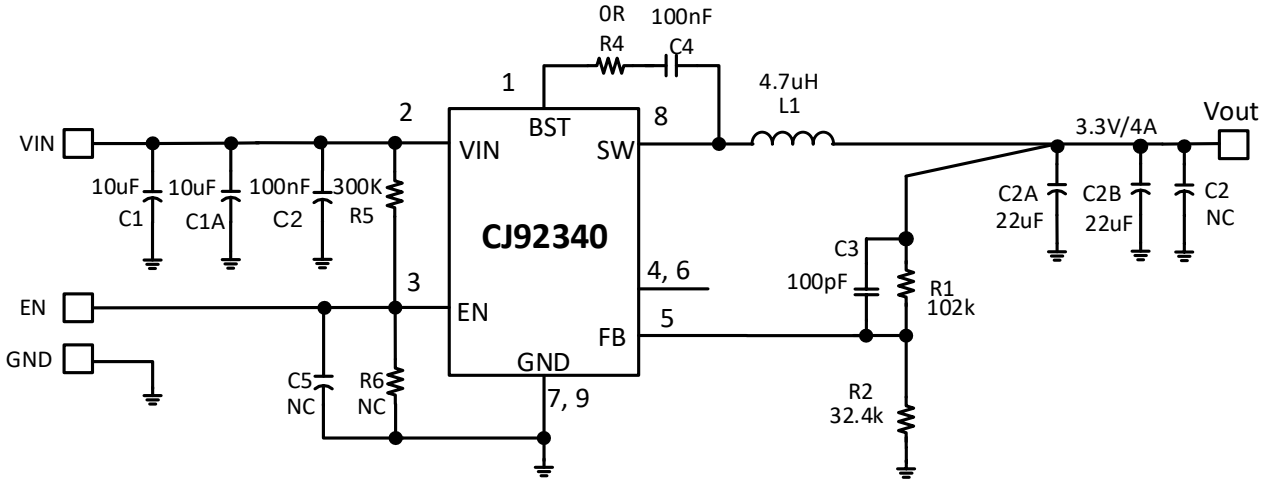


Figure 9-2 Typical VOUT=3.3V/4A application

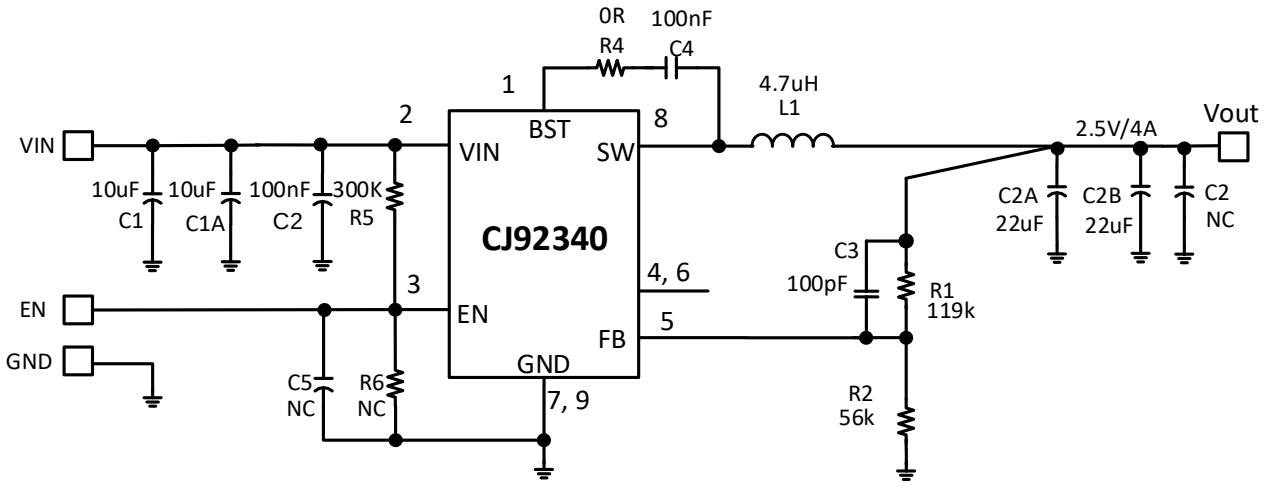


Figure 9-3 Typical VOUT=2.5V/4A application

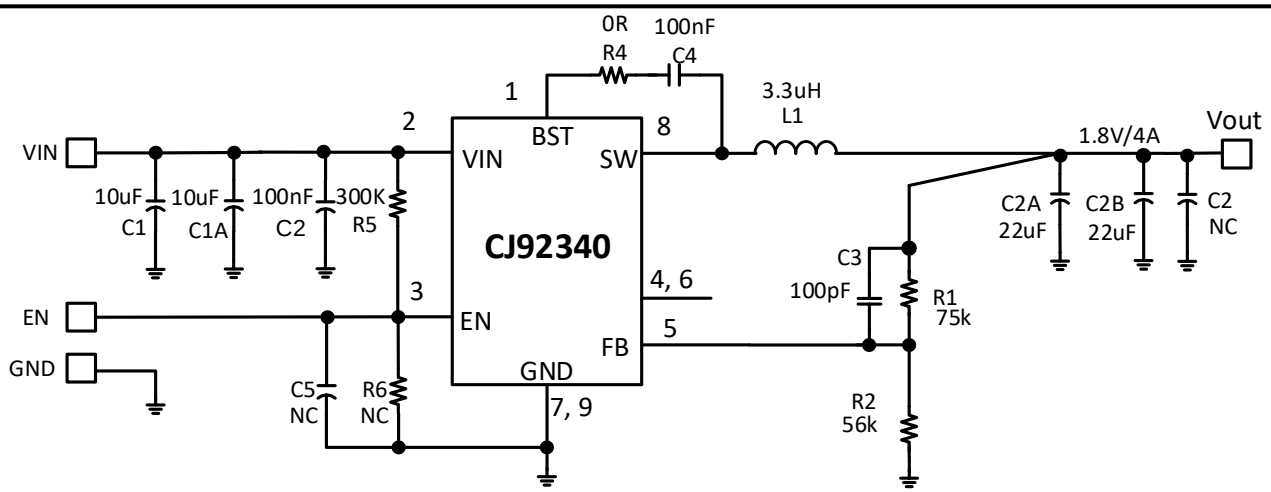


Figure 9-4 Typical VOUT=1.8V/4A application

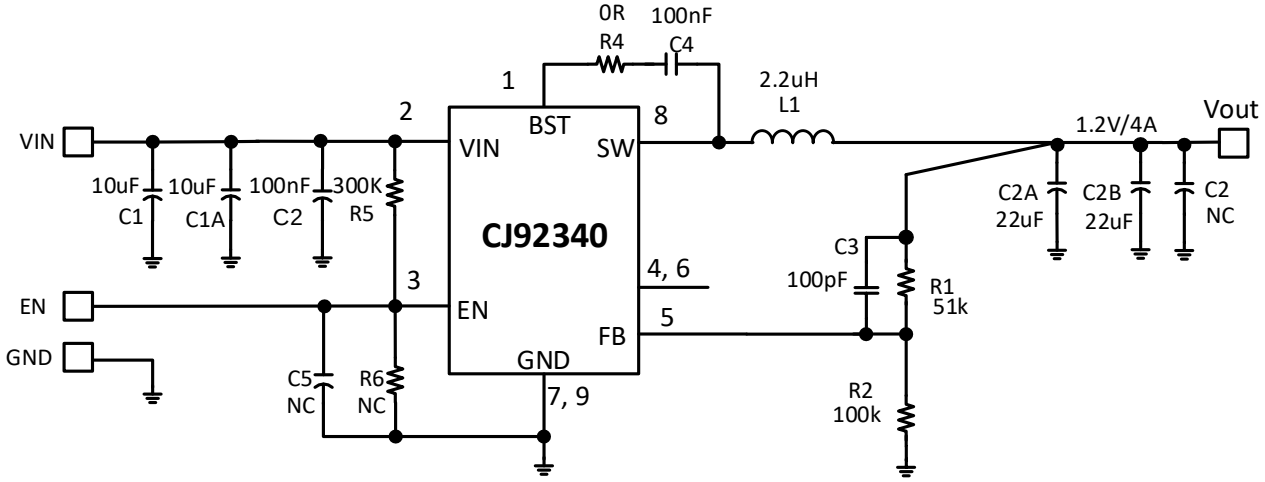


Figure 9-5 Typical VOUT=1.2V/4A application

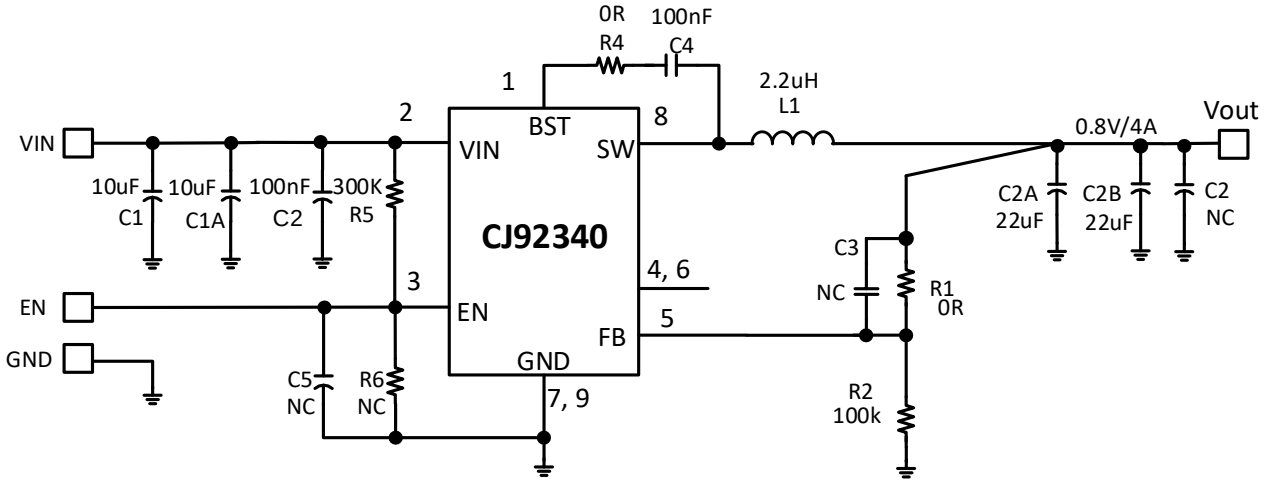


Figure 9-6 Typical VOUT=0.8V/4A application

9.2 Setting the Output Voltage

The CJ92340 output voltage can be set by the external resistor dividers. First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It recommended to choose a value within 2k to 100k for R2. The reference voltage is fixed at 0.798V. The feedback network is shown below Figure.

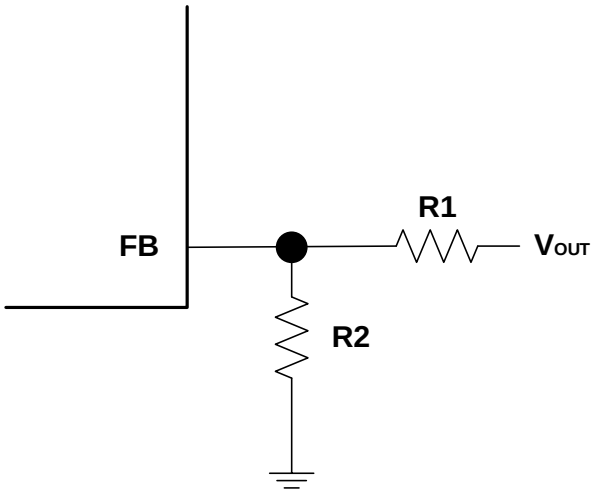


Figure 9-7 Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT} = V_{FB}(R_1 + R_2)/R_2$$

9.3 Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 60% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔIL is the inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{L\,(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

9.4 Selecting Input capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the stepdown converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations. The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst case occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}}$$

9.5 Selecting the Output Capacitor

The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}})$$

Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor, F_{OSC} is the switching frequency. Note that, in real application, should consider that the ceramic capacitor capacitance has derating.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple caused by ESR is very small. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (\frac{1}{8 \times F_{OSC} \times C_{OUT}})$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The CJ92340 can be optimized for a wide range of capacitance and ESR values.

Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{OUT_max} can be limited approximately by:

$$C_{OUT\_MAX} = (I_{limit_{ave}} - I_{OUT}) \times T_{SS}/V_{OUT}$$

Where, ILIM_AVG is the average start-up current during soft-start period, T_{SS} is the soft-start time (2.4ms typically 10% V_{OUT} to 90% V_{OUT}).

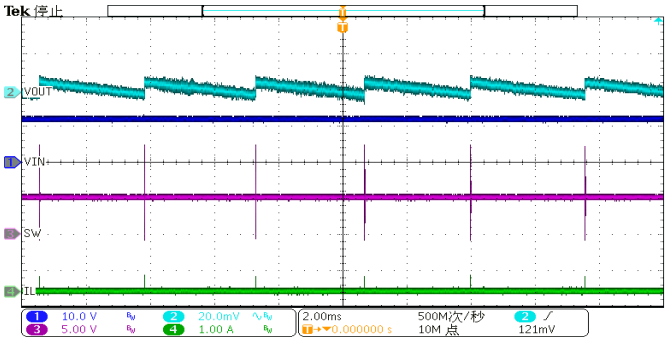
The recommended parameters for typical output application as table 1 shown.

Table 1: **Resistor Selection for Common Output Voltages**

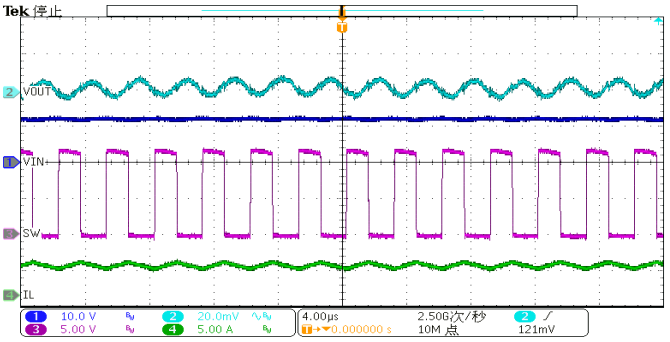
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (uF)
5	169	32.4	10	44
3.3	102	32.4	4.7	44
2.5	119	56	4.7	44
1.8	75	56	3.3	44
1.2	51	100	2.2	44
1	25	100	2.2	44
0.8	0	100	2.2	44

9.6 Application Curve

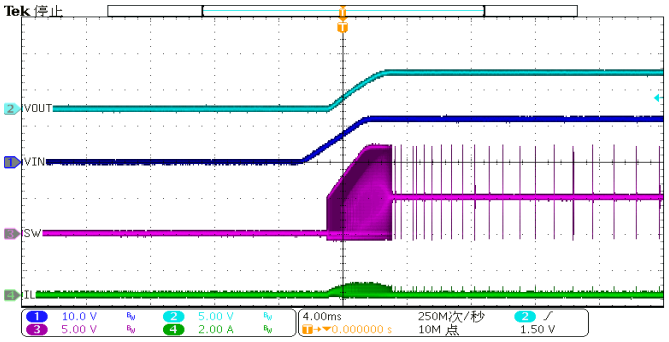
V_{IN} = 12V, V_{OUT} = 5V, C_{IN} =10uF, C_{OUT} = 44uF, L1 = 10uH, and T_A = 25°C, Frequency = 350kHz, unless otherwise noted.



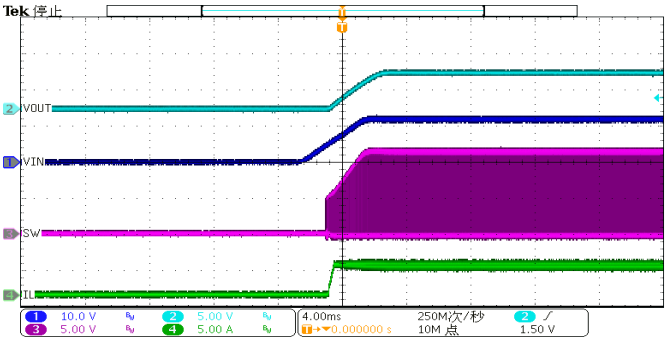
Output Voltage ripple (IOUT=0A)



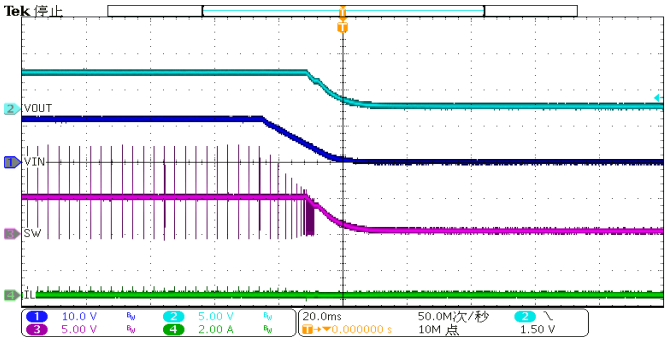
Output Voltage ripple (IOUT=4A)



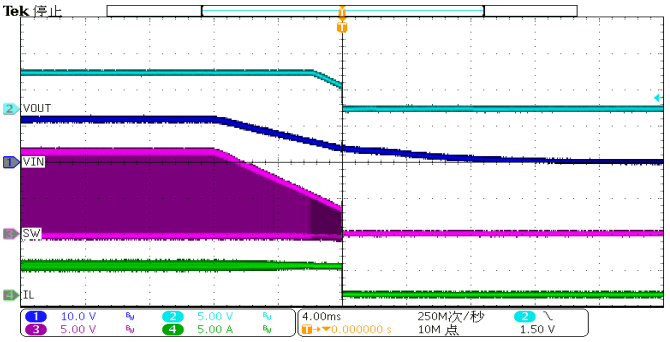
Start – Up through VIN (IOUT=0A)



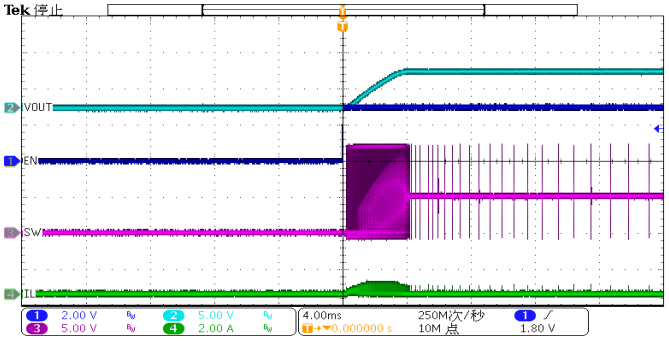
Start – Up through VIN (IOUT=4A)



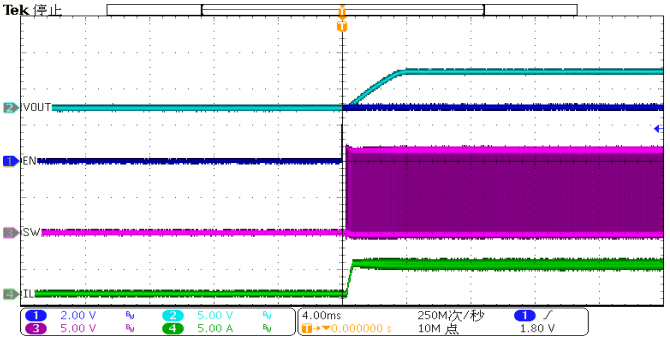
Shutdown through VIN (IOUT=0A)



Shutdown through VIN (IOUT=4A)

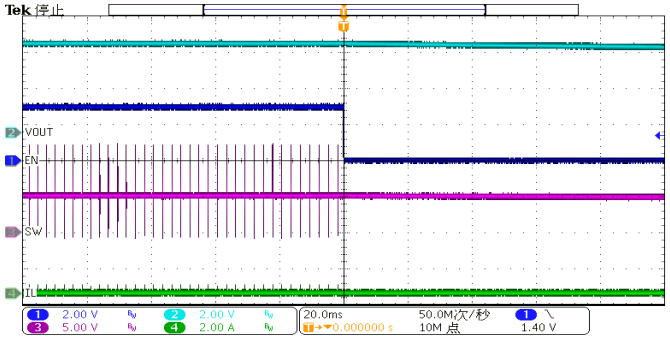


Start – Up through EN (IOUT=0A)

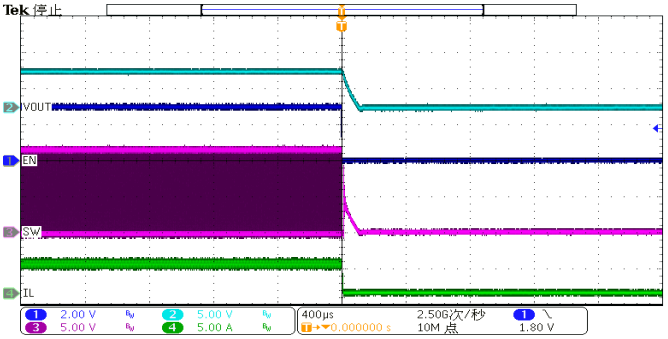


Start – Up through EN (IOUT=4A)

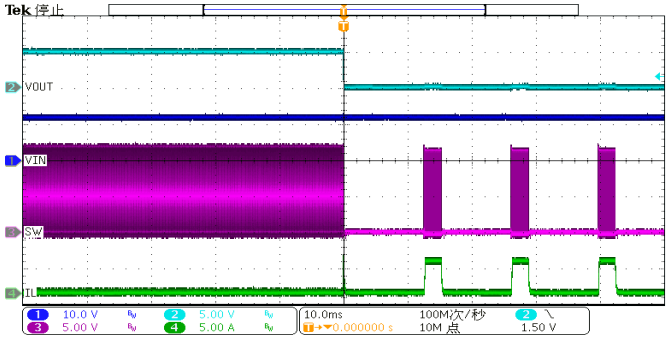
V_{IN} = 12V, V_{OUT} = 5V, C_{IN} =10uF, C_{OUT} = 44uF, L1 = 10uH, and T_A = 25°C, Frequency = 350kHz, unless otherwise noted. *(continued)*



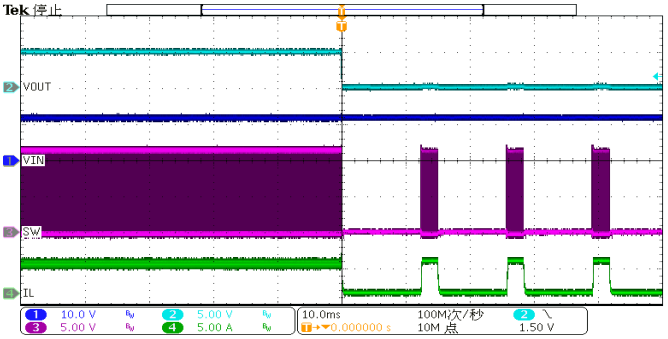
Shutdown through EN (IOUT=0A)



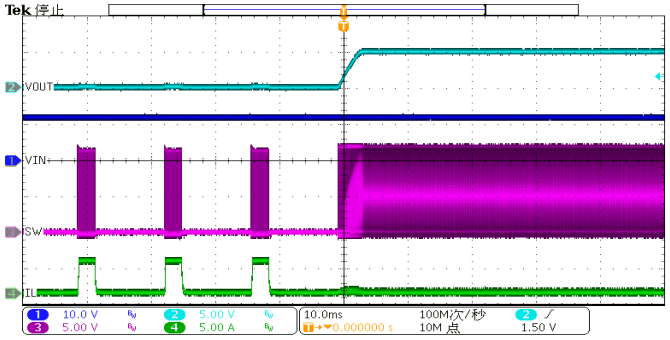
Shutdown through EN (IOUT=4A)



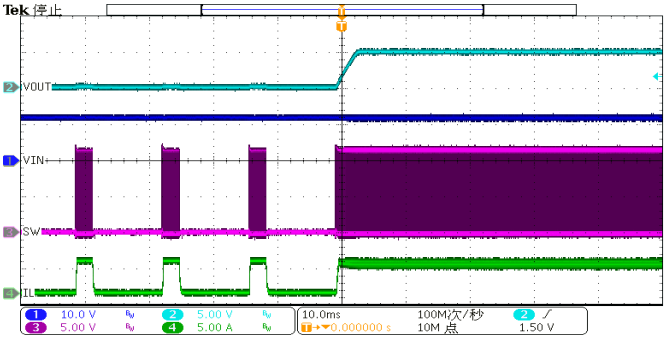
Short Entry (IOUT-0A)



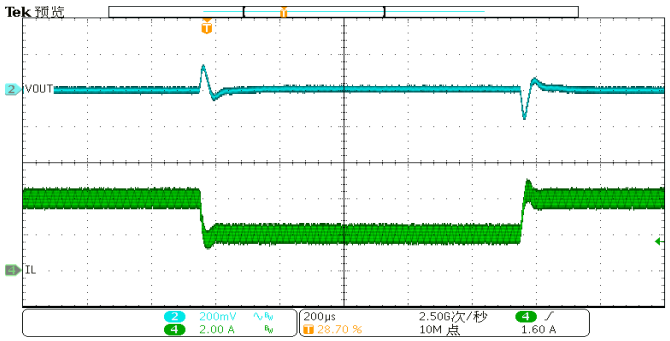
Short Entry (IOUT-4A)



Short Recovery (IOUT=0A)

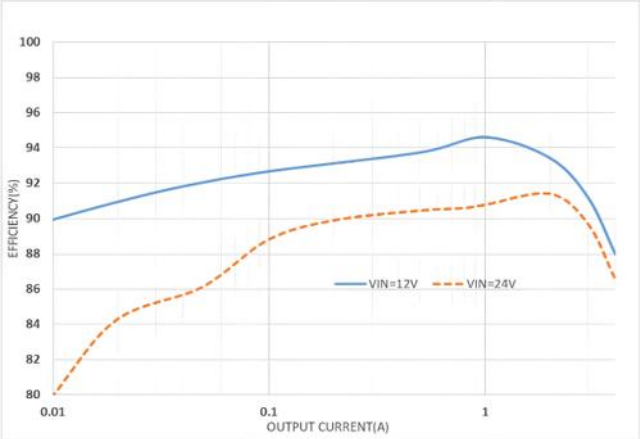


Short Recovery (IOUT=4A)

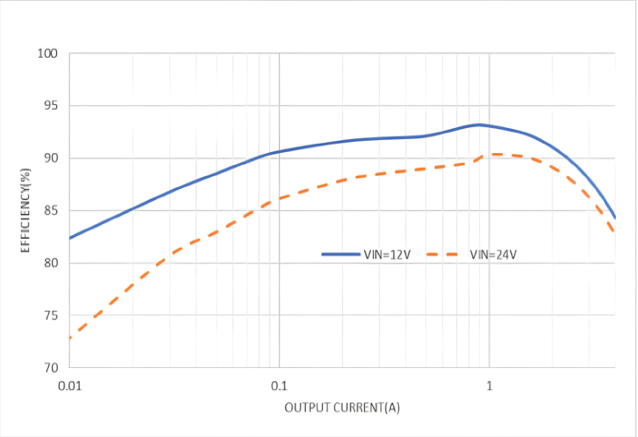


Load Transient (VOUT=5V, L = 10uH, feedback cap=200pF, 2A to 4A, 2.5A/us)

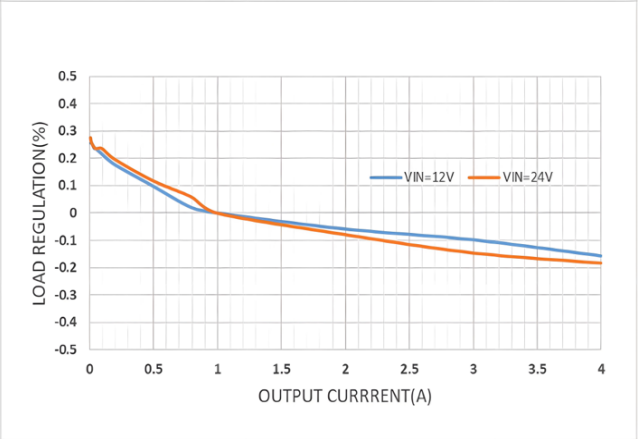
V_{IN} = 12V, V_{OUT} = 5V, C_{IN} =10uF, C_{OUT} = 44uF, L1 = 10uH, and T_A = 25°C , Frequency = 350kHz, unless otherwise noted. *(continued)*



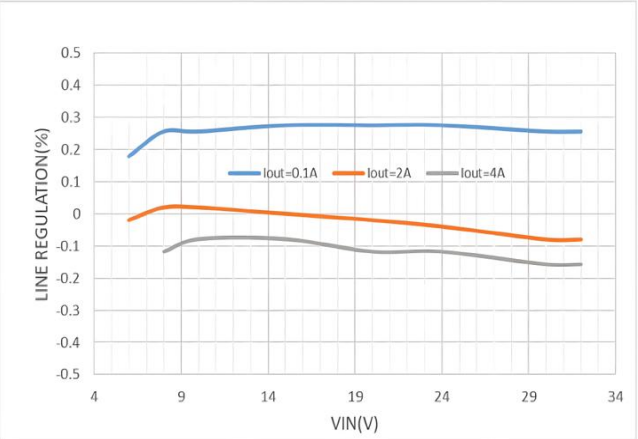
Efficiency vs. Load Current, L=6.8uH,DCR= 48mohm V_{OUT}=5V



Efficiency vs. Load Current, L=6.8uH,DCR= 48mohm V_{OUT}=3.3V



Load Regulation



Line Regulation

10 Layout

10.1 Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below and take figures as the reference.

- The high current paths (GND, VIN and SW) should be placed very close to the device with short, direct and wide traces.
- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

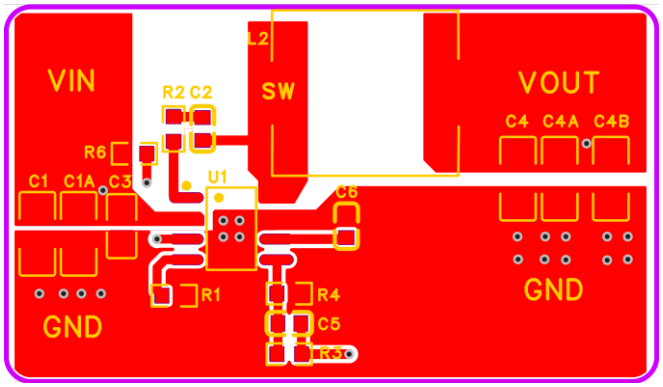


Figure 10-1. Top Layer

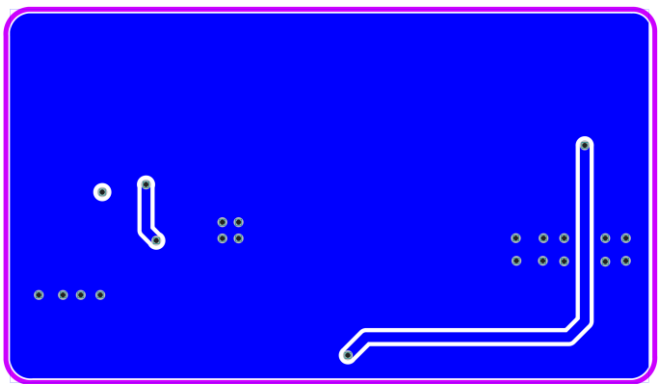
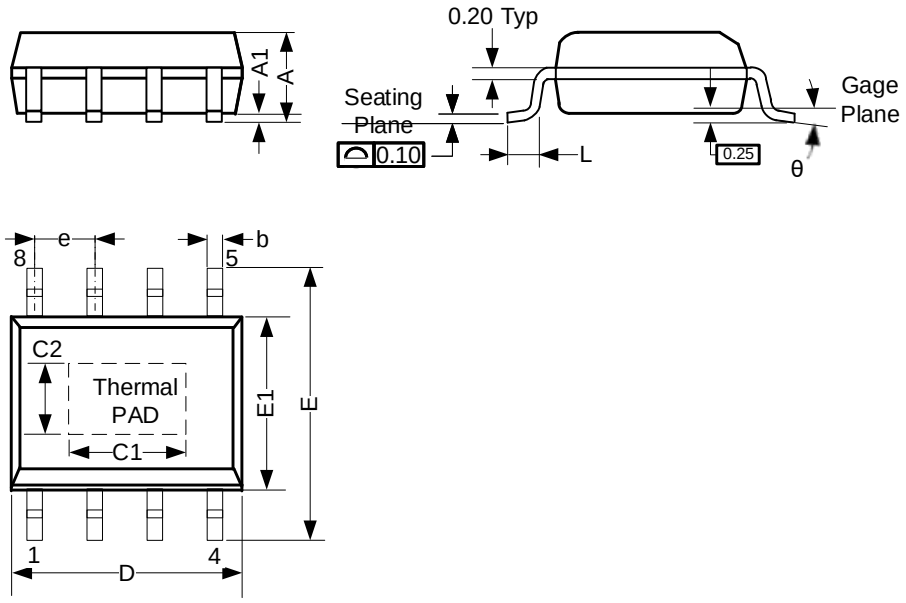


Figure 10-2. Bottom Layer

11 Mechanical Information

11.1 ESOP8 Mechanical Information

ESOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	–	–	1.65
A1	0.00	–	0.15
b	0.39	–	0.47
C1	3.15	–	3.45
C2	2.26	–	2.56
D	4.80	–	5.00
E	5.80	–	6.20
E1	3.80	–	4.00
e	1.27BSC		
L	0.41	–	1.27
θ	0°	–	8°

12 Notes and Revision History

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

12.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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