30V, 5A, Synchronous, DC/DC Step-Down Converter

CJ92350 DC/DC Regulator

1 Introduction

The CJ92350 device is an easy-to-use synchronous step-down Buck. Which integrated low on resistance high-side and low-side power MOSFETs. The CJ92350 can deliver 5A of output current efficiently with constant on time (COT) control for fast loop response.

This CJ92350 device achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

This CJ92350 device has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuits protection, FB open short protection and thermal shutdown in case of excessive power dissipation. The CJ92350 is available in a space-saving ESOP8L package.

2 Available Packages

PART NUMBER	PACKAGE
CJ92350	ESOP8

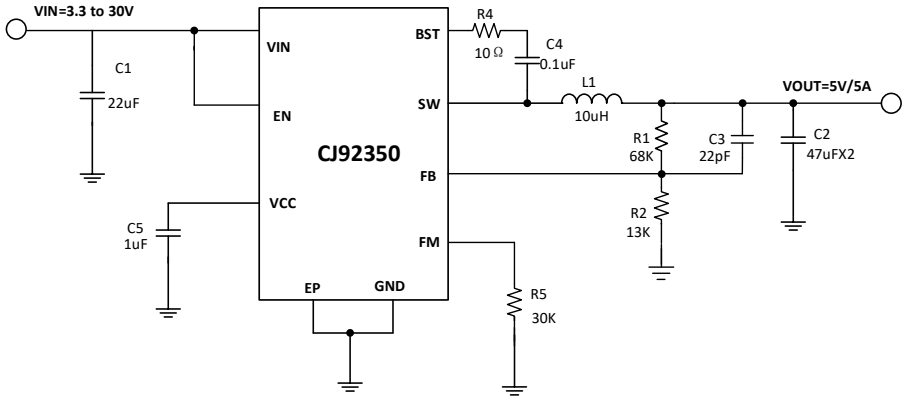
3 Features

- 3.6V to 30V Wide Input Range
- 5A Continuous Output Current
- 43mΩ /27mΩ Internal Power MOSFETs
- 350uA Low Quiescent Current
- Constant On Time Control for Fast Loop Response
- 250kHz/300kHz/400kHz Switching Frequency
- PFM and FPWM Mode Selectable
- Support Up to 100% Large Duty Cycle
- Output Discharge
- Output Voltage adjustable from 0.8V
- Support Pre-Biased Output Startup
- Full Protection, Over Current Protection and Hiccup, Output Over Voltage Protection, FB Open Short Protection, Over Temperature Protection

4 Applications

- Telecom and Networking Systems
- IP camera
- Automotive Cigarette Lighter Adapter
- Wall charger
- General Purpose Point-of-Load (POL)

Typical Application



Typical Application Circuit

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ92350-PBN	ESOP8	-40 ~ 125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products.

Customized: Products manufactured to meet the specific needs of customers.

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available.

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers.

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

ESOP8

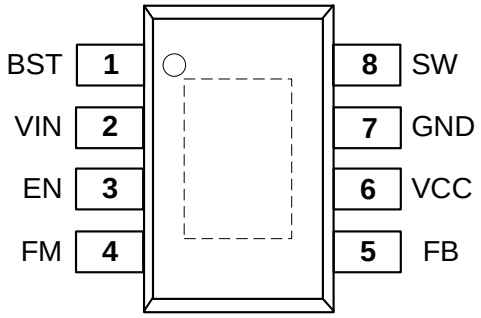


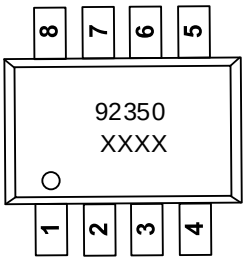
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I / O(1)	DESCRIPTION
No.	NAME		
1	BST	G	**Bootstrap**. Connect a capacitor between SW and BST pins to form a floating supply across the High-side switch driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
2	VIN	P	**Supply input Pin**. VIN supplies power for the internal MOSFET and regulator. The input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
3	EN	P	**Enable Pin**. Pull high to enable Buck. Pull to GND or Float this pin to disable Buck.
4	FM	I	**Operation mode and frequency selection**. Program FM to select CCM, pulse skip mode, and the operating switching frequency. Connect a resistor between FM pin and GND can configure the frequency.
5	FB	I	**Feedback input to the convertor.** Connect a resistor divider to set the output voltage.
6	VCC	O	**Internal 5V LDO regulator output**. Decouple VCC with a 1μF capacitor. The VCC LDO is shutdown when EN is pulled low.
7	GND	P	**Power Ground terminal.**
8	SW	P	**Switching output of the convertor**. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
9	EP	G	**Exposed Pad.** Connect exposed pad to the PCB GND plane to achieve good thermal performance.

(1) I – Input; O – Output; P – Power; G - GND

6.3 Marking Information



"92350": Device code.
"XXXX": Date Code.

7 Specifications

7.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified) (1)

SYMBOL	DEFINITION	VALUE	UNIT
VIN	VIN to GND	-0.3 ~ 31	V
SW	SW to GND	-0.7(-5V in 10ns) to VIN+ 0.7	V
EN	EN to GND	-0.3 ~ 31	V
BST	BST to SW	-0.3 ~ 6	V
All other pins		-0.3 ~ 6	V
T_{STG}	Storage temperature	-65 ~ 150	°C
T_j	Junction temperature	-40 ~ 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

SYMBOL	DEFINITION	RATING	UNIT
BST	BST to SW	4~5	V
V_{IN}	V_{IN} to GND	4.5~30	V
V_{OUT}	V_{OUT} to GND	0.8 ~ VIN	V
I_{OUT}	Max continuous Output Current	5	A

7.3 ESD Ratings

SYMBOL	DEFINITION	VALUE	UNIT
HBM	Human body model	±2000	V
CDM	Charged device mode	±2000	

7.4 Thermal Information

SYMBOL	DEFINITION	RATING	UNIT
$R_{\Theta JC(TOP)}$	Junction-to-case(top) thermal resistance	6	℃/W
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	30	℃/W

Measured on DEMO board 2-layer PCB, 63mmx48mm board.

7.5 Electrical Characteristics

VIN=12V, V_{EN}=2V, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input UVLO and Quiescent Current						
VIN_{UVR}	VIN UVLO rising threshold			3.3		V
VIN_{UVF}	VIN UVLO falling threshold			2.8		V
VIN_{UV_hys}	VIN UVLO hysteresis			0.5		V
I_{QS}	Shutdown supply current	V_{EN} < 0.3V, V_{IN}=12V		1	3	uA
I_Q	Quiescent supply current	V_{IN}=12V, No load, V_{FB} = 0.83V, no switching		350		uA
VCC REGULATOR						
V_{CC}	V_{CC} regulator	VIN>5.2V		5		V
I_{VCC}	VCC Current Limit		20			mA
High Side and Low Side MOSFETs						
LKG_{HS}	High-side leakage	V_{EN}=0V, V_{SW}=0V			1	uA
LKG_{LS}	Low-side leakage	V_{EN}=0V, V_{SW}=18V			1	uA
R_{ON_HS}	High-Side Switch on resistance	V_{BST-SW} = 5V		43		mΩ
R_{ON_LS}	Low-Side Switch on resistance	V_{IN} = 12V		27		mΩ
Output Discharge Resistor						
$R_{Discharge}$				200		Ω
Feedback Voltage and SS						
V_{FB}	Feedback voltage	Ta=25°C	788	800	812	mV
I_{LK_FB}	Feedback leakage	V_{EN} = 1V, V_{FB} = 2V			0.1	uA
T_{SS}	Soft-Start time	V_{FB} from 0% to 100%		6		ms
Switching Frequency						
fsw	Oscillator frequency	FM=PGND, PFM		250		kHz
		FM=30k, PFM		300		kHz
		FM=75k, PFM		400		kHz
		FM=150k, CCM		400		kHz
		FM=270k, CCM		300		kHz
		FM Float, CCM		250		kHz
T_{ON_MIN}	Minimum on time			70		ns
T_{OFF_MIN}	Minimum off time			150		ns
FB_{UV}				75%		V_{FB}
T_{OTP_R}	Thermal shutdown (1)			160		°C
T_{OTP_Hys}	OTP hysteresis (1)			30		°C
D_{MAX}	Max duty cycle			100		%

Electrical Characteristics

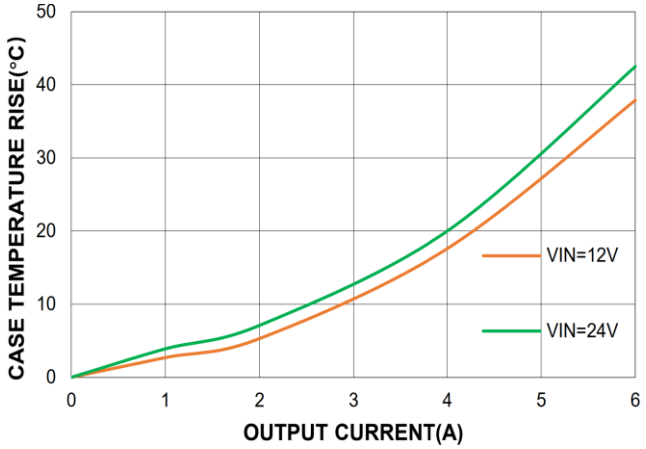
VIN=12V, V_{EN}=2V, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit						
I_{LIM_LS}	Low-Side Current valley limit			5.5		A
I_{LIM_HS}	High-Side Current peak limit			7		A
I_{NOC}	Negative Current Limit			4		A
Enable						
V_{EN_R}	EN Rising Threshold	Low to High		1.25		V
V_{EN_F}	EN falling Threshold	High to Low		1.05		V
V_{EN_Hys}	EN Threshold Hysteresis			0.2		V
R_{EN}	Enable input resistor			2400		kΩ
VOUT OVP/UVP threshold						
$V_{OVP\_rising\_th}$	Rising			115%		V_{FB}
$V_{OVP\_falling\_th}$				105%		V_{FB}
$V_{UVP\_falling\_th}$				75%		V_{FB}
$V_{UVP\_rising\_th}$				85%		V_{FB}

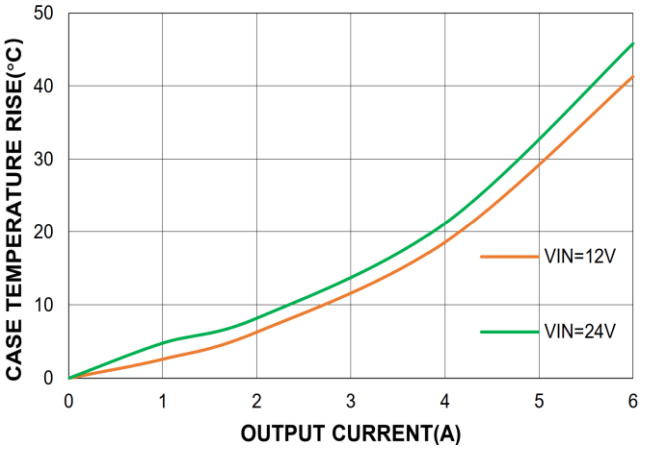
(1) Guaranteed by design

7.6 Typical Characteristics

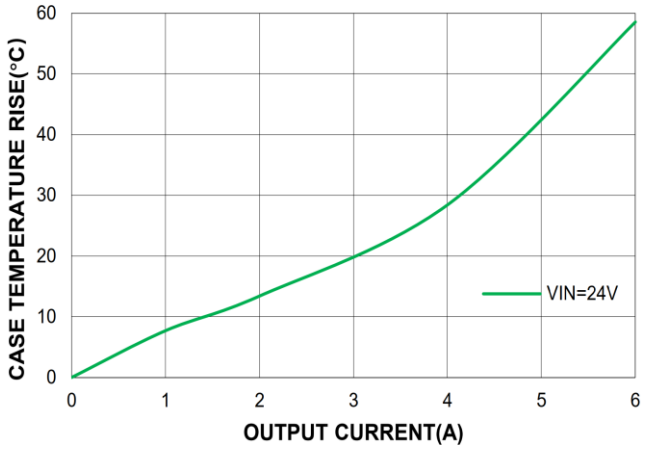
V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22uF, C_{OUT} = 44uF, T_A = 25°C, unless otherwise noted.



Case Temperature Rise vs. Load Current, V_{OUT}=3.3V



Case Temperature Rise vs. Load Current, V_{OUT}=5V



Case Temperature Rise vs. Load Current, V_{OUT}=12V

8 Function Description

8.1 Overview

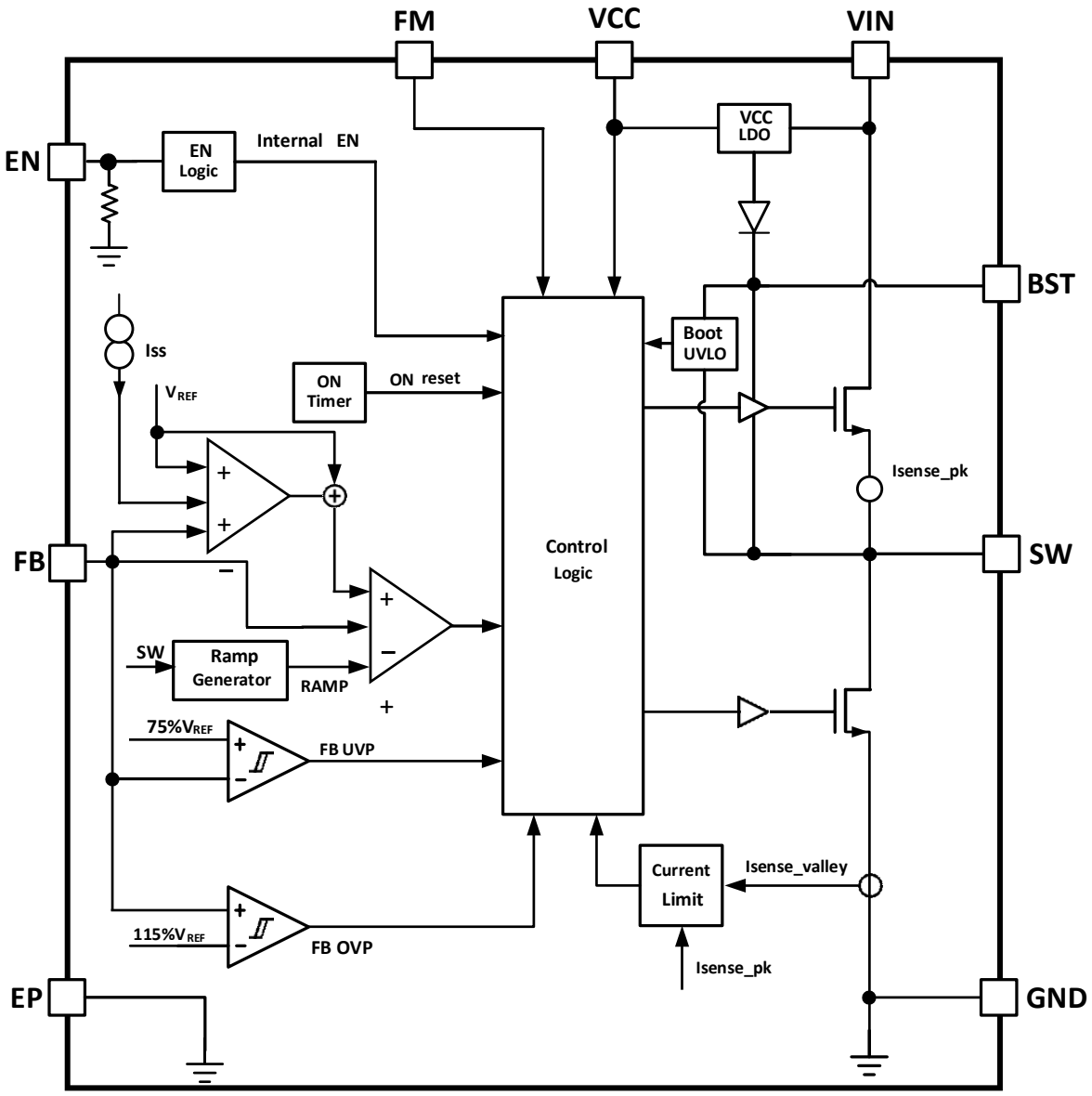


Figure 8-1 Function block diagram

8.2 Pulse-Width Modulation (PWM) Control

The CJ92350 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (VFB) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when VFB drops below V_{REF}. By repeating operations this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There is a dead short between the input and GND if both the HS-FET and LS- FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS- FET off and HS-FET on period.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

8.3 Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high, and the inductor current is always above zero amps. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period begins. In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

8.4 Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM). It works on Light-load operation mode. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on- timer. When the HS-FET is turned off, the LS- FET is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The LS-FET driver enters tri-state (Hi-Z) whenever the inductor current reaches zero. The output capacitors discharge to GND through the LS- FET slowly. As a result, the efficiency in light- load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

As the output current increases from the light- load condition, the current modulator regulation time becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with below Equation:

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L_{OUT} \times F_{SW} \times V_{IN}}$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

8.5 Under-Voltage Lockout (UVLO) Protection

The CJ92350 has under-voltage lockout (UVLO) protection: the part starts up only when VIN/VCC UVLO threshold (3.3V typically). The part shuts down when the VIN/VCC voltage is lower than the UVLO falling threshold voltage (typically 2.8V), the UVLO protection is non-latch off.

8.6 Enable (EN) control

EN is used to enable or disable the entire chip. Pull EN high (1.25V typically) to turn on the regulator. Pull EN low (<1.05V typically) to turn off the regulator. For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. To determine the automatic start-up voltage, calculate the values of the pull-up resistor (RUP from VIN to EN) and the pull- down resistor (RDOWN from EN to GND) with the below.

$$VIN_{Start} = \frac{1.25V \times (R_{UP} + R_{DOWN})}{R_{DOWN}}$$

If an application requires a higher UVLO, use EN to adjust the input voltage UVLO by using two external resistors (see the below figure).

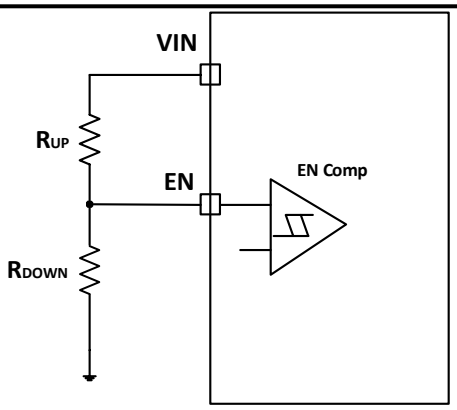


Figure 8-2 Adjustable UVLO Application Circuits

8.7 Soft Start (SS)

The CJ92350 employs a soft-start mechanism to ensure a smooth output during power-up. When the chip starts (both EN>1.25V and VIN/VCC are above UVLO), the internal circuitry generates a soft-start voltage (VSS) that ramps up linearly. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. Soft-start time is fixed 6mS (typically 10% V_{OUT} to 90% V_{OUT}).

8.8 Over-Current limit (OCL)

The CJ92350 has a cycle-by-cycle over-current limiting control (OCL). The current-limit circuit employs a valley current-sensing algorithm. The part uses the RDS(ON) of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, PWM is not allowed to initiate a new cycle, even if FB is lower than REF (see the below Figure).

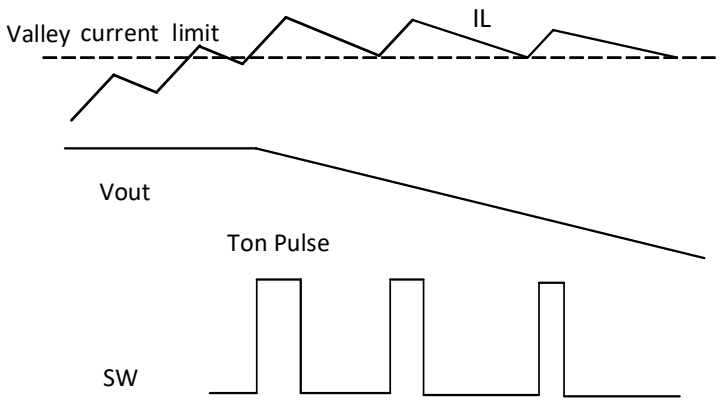


Figure 8-3 Valley Current-Limit Control

Since the comparison is done during the LSFET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (IOC) can be calculated with the below Equation:

$$I_{OC} = I_{LIMIT} + \frac{\Delta I_{inductor}}{2}$$

The OCL itself limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, causing the output voltage to fall off. Eventually, the voltage crosses the under-voltage protection (UVP) threshold and enters the hiccup protection.

8.9 OVP/UVP

The CJ92350 monitors a resistor-divided VFB to detect over- and under-voltage. When VFB becomes higher than 115% of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the circuit will turn on the low side MOSFET to discharge the output. LSFET will turn off until the negative current limit is triggered then LSFET

will remain off for 5us to turn on again. IC will repeat this behavior until the output OVP condition is removed.

When VFB drops below 75% of VREF, the UVP comparator output goes high, and the CJ92350 enters the hiccup protection.

8.10 Pre-Bias Start-Up

If the output is pre-biased to a certain voltage during start-up, the CJ92350 disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

8.11 FM Select Frequency/Mode Programmable

The CJ92350 can set up the operation mode and PWM frequency by connecting FM pin to GND with a resistor. Below table shows the configuration.

Table 1: Frequency and Mode configuration

R_{FM}(kΩ)	Work Mode	Frequency (KHz)
0	PFM	250
30	PFM	300
75	PFM	400
150	FPWM	400
270	FPWM	300
Float	FPWM	250

8.12 Large Duty Cycle Operation

When CJ92350 will automatically extend the frequency to support the application when V_{IN} is close to V_{OUT}. The frequency extend circuit will be triggered when T_{OFF} min time is reached. The CJ92350 can support up to 100% duty cycle. Large duty cycle operation is disabled when OC is triggered.

8.13 Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

8.14 Output Discharge

During the EN off period, the output is discharged via a 200Ω resistor on the SW. This discharge FET is turned off when V_{OUT} is fully discharged or the 10ms timer is finished.

9 Application and Implementation

9.1 Typical Application Circuit

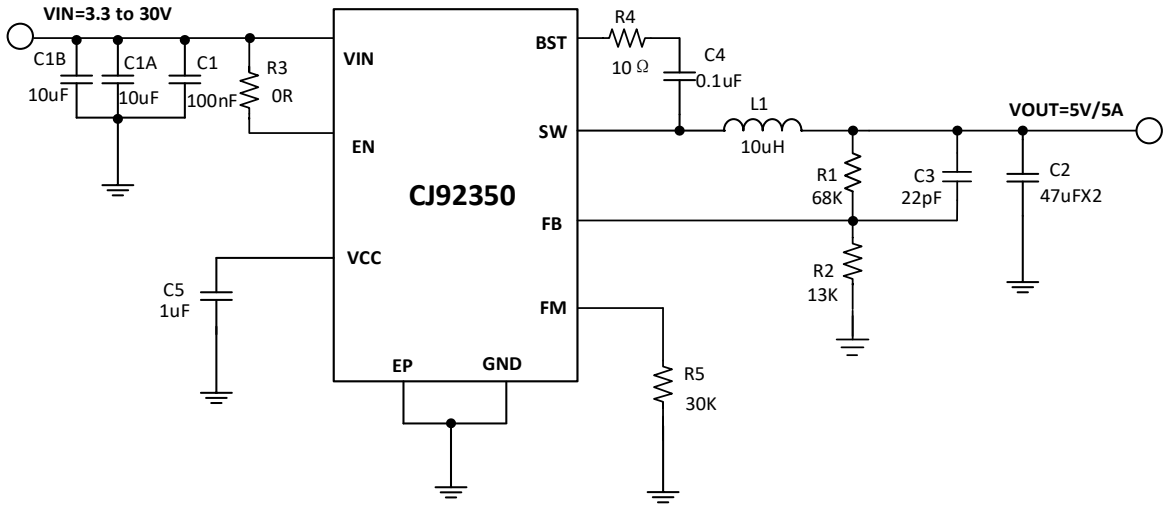


Figure 9-1 Typical VOUT=5V/5A application

Table2: Frequency setting

R5/kΩ	MODE	SWITCHING Frequency/kHz
GND	DCM	250
30		300
75		400
150	CCM	400
270		300
Float		250

9.2 Setting the Output Voltage

The CJ92350 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.8V. The feedback network is shown below Figure.

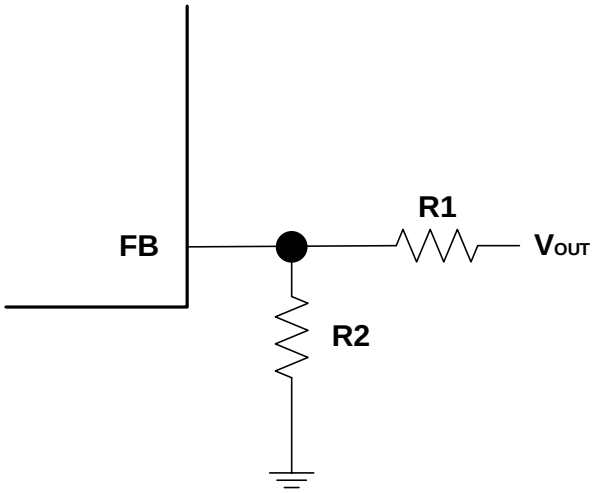


Figure 9-2 Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT} = \frac{V_{FB}(R_1 + R_2)}{R_2}$$

Table 3 lists the recommended feedback resistor values for common output voltages.

Table 3: Resistor Selection for Common Output Voltages (1)(2)

VIN(V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C3(pF)	Lout(μH)	C_{OUT} (μF)
12	3.3	40.7	13	22	4.7	47x2
	5	68	13	22	6.8	47x2
	9	133	13	22	6.8	47x2
24	3.3	40.7	13	22	6.8	47x2
	5	68	13	22	10	47x2
	9	133	13	22	10	47x2
	12	182	13	22	10	47x2
	15	232	13	22	10	47x2
	20	312	13	22	10	47x2

Note 1: For a detailed design circuit, please refer to the Typical Application Circuits.

Note2: The table recommends parameters based on Fsw=300KHz

9.3 Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 60% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by the equation as below:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔIL is the inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Table 4 lists the recommended values of inductors at different frequency:

Table 4: Power Inductor Selection

V_{IN} (V)	F_{SW} (KHZ)	L1 (μH)
12	250	8.2
	300	6.8
	400	4.7
24	250	15
	300	10
	400	6.8

9.4 Selecting Input capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the stepdown converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations. The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}}$$

9.5 Selecting the Output Capacitor

The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be

estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor, F_{OSC} is the switching frequency. Note that, in real application, it should consider that the ceramic capacitor capacitance has derating.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple caused by ESR is very small. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The CJ92350 can be optimized for a wide range of capacitance and ESR values.

Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but the maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{OUT_MAX} can be limited approximately by:

$$C_{OUT_{MAX}} = \left(I_{limit_{ave}} - I_{OUT}\right) \times \frac{T_{SS}}{V_{OUT}}$$

Where ILIM_AVG is the average start-up current during soft-start period, T_{SS} is the soft-start time (2.4ms typically 10% V_{OUT} to 90% V_{OUT}).

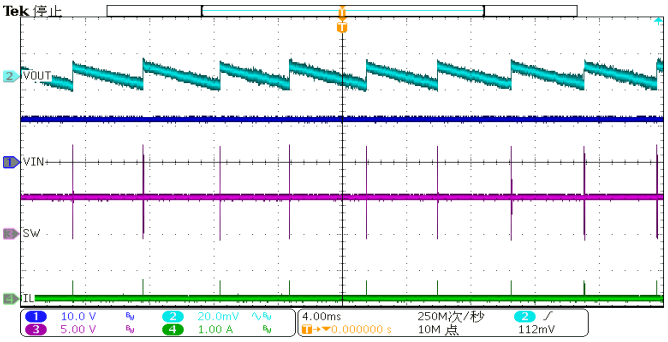
The recommended parameters for a typical output application as table 5 shown.

Table 5: Resistor Selection for Common Output Voltages

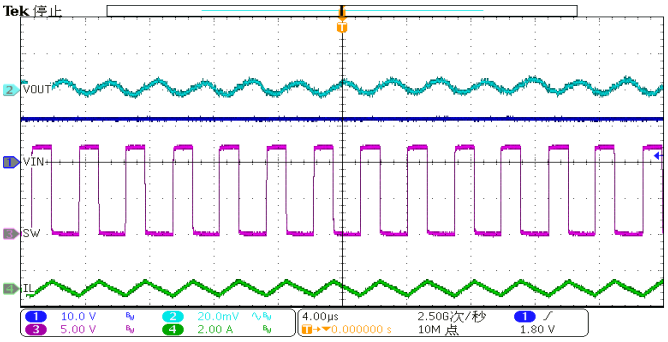
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (uF)
5	169	32.4	10	44
3.3	102	32.4	4.7	44
2.5	119	56	4.7	44
1.8	75	56	3.3	44
1.2	51	100	2.2	44
1	25	100	2.2	44
0.8	0	100	2.2	44

9.6 Application Curve

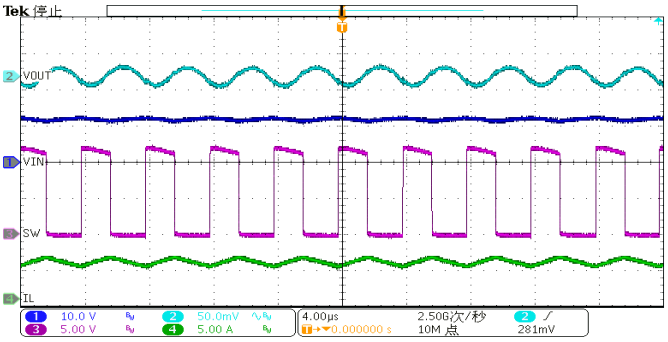
V_{IN} = 12V, V_{OUT} = 5V, C_{IN} =10uF, C_{OUT} = 44uF, L1 = 10uH, and T_A = 25°C, Frequency = 300kHz, unless otherwise noted.



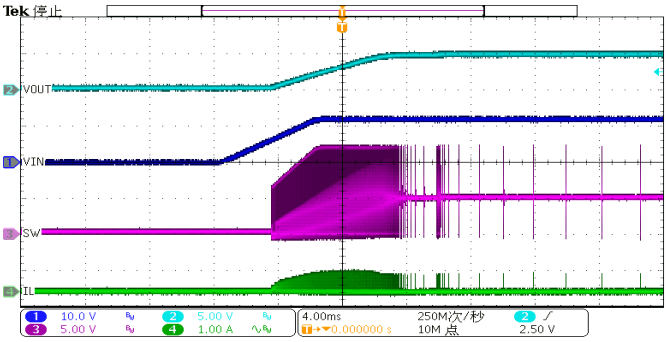
Output Voltage ripple (PFM, I_{OUT}=0A)



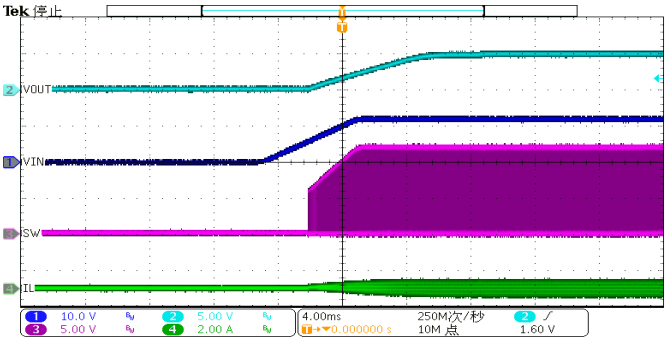
Output Voltage ripple (FPWM, I_{OUT}=0A)



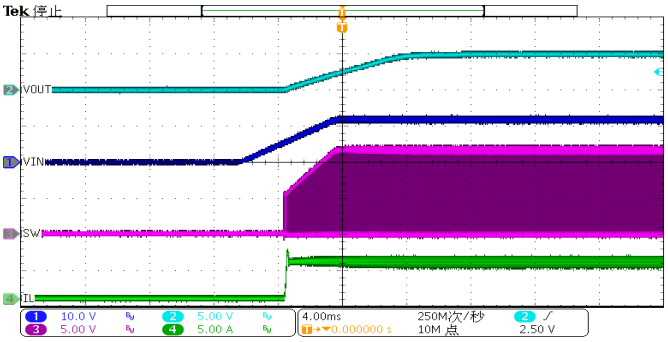
Output Voltage ripple (I_{OUT}=5A)



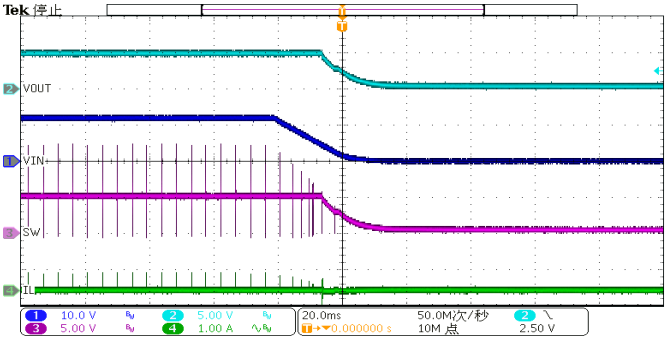
Start – Up through VIN (PFM, I_{OUT}=0A)



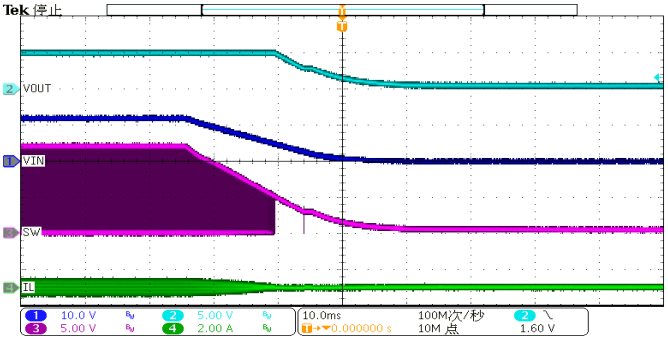
Start – Up through VIN (FPWM, I_{OUT}=0A)



Start – Up through VIN (I_{OUT}=5A)

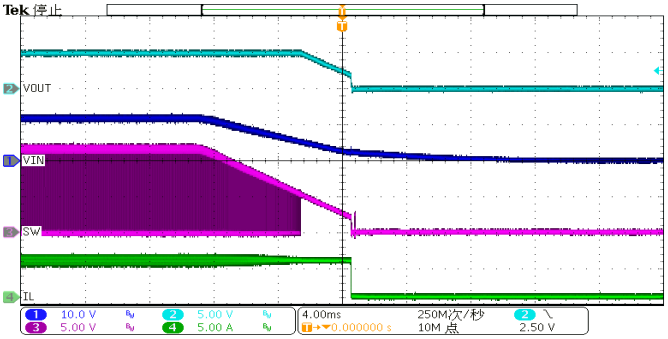


Shutdown through VIN (PFM, I_{OUT}=0A)

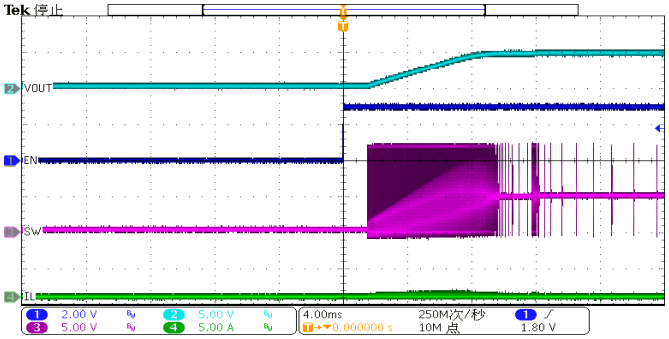


Shutdown through VIN (FPWM, I_{OUT}=0A)

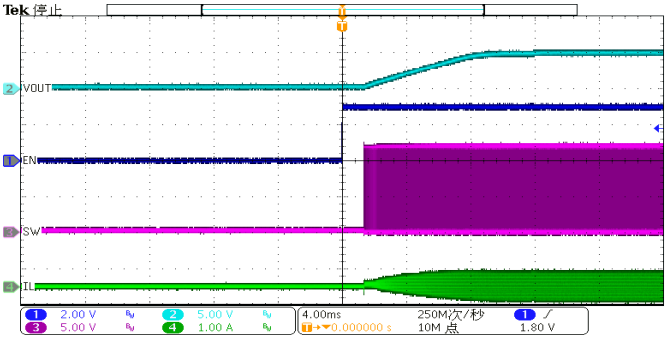
V_{IN} = 12V, V_{OUT} = 5V, C_{IN} =10uF, C_{OUT} = 44uF, L1 = 10uH, and T_A = 25°C, Frequency = 300kHz, unless otherwise noted. *(continued)*



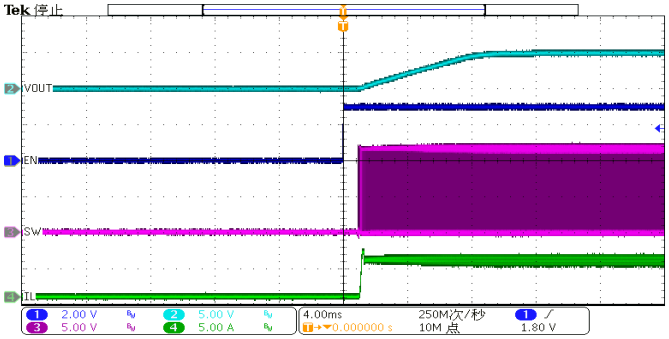
Shutdown through VIN (I_{OUT}=5A)



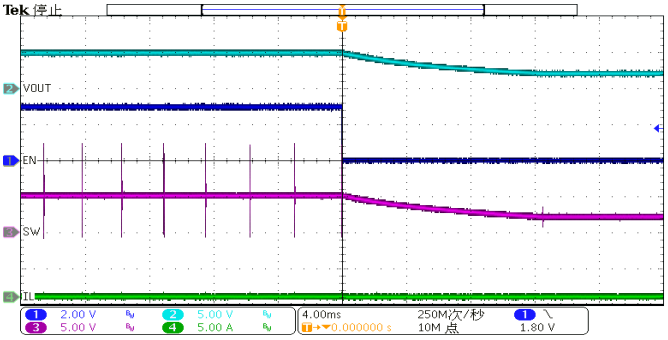
Start – Up through EN (PFM, I_{OUT}=0A)



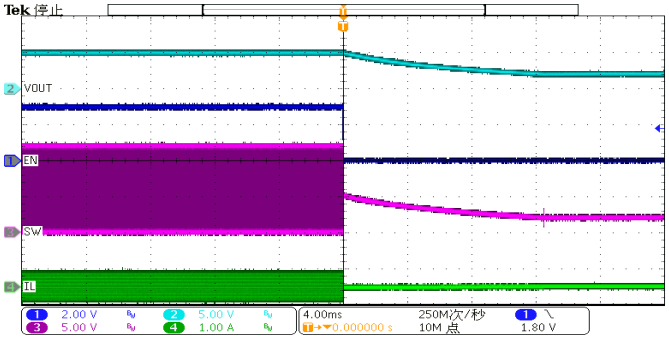
Start – Up through EN (FPWM, I_{OUT}=0A)



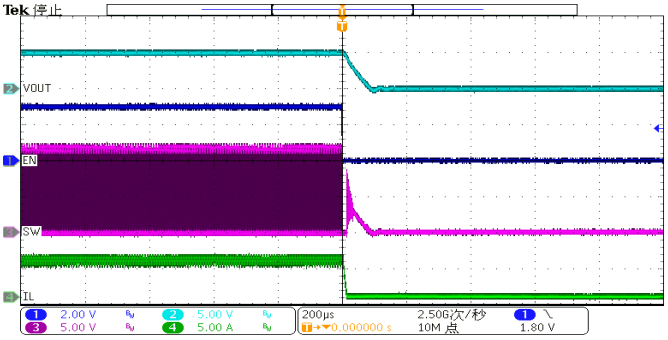
Start – Up through EN (I_{OUT}=5A)



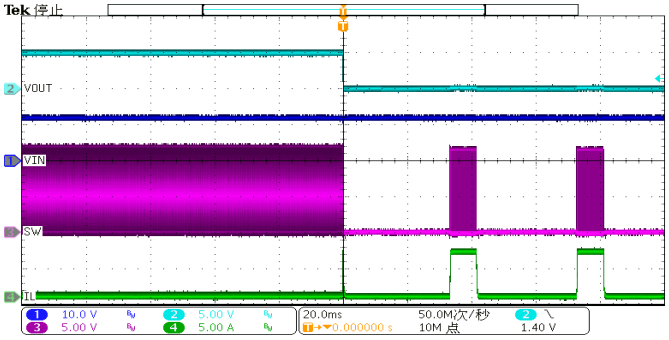
Shutdown through EN (PFM, I_{OUT}=0A)



Shutdown through EN (FPWM, I_{OUT}=0A)

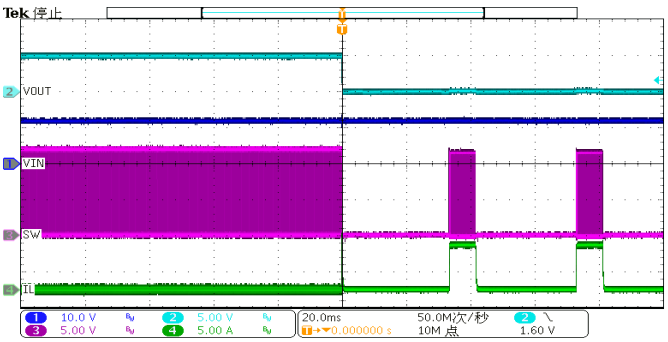


Shutdown through EN (I_{OUT}=5A)

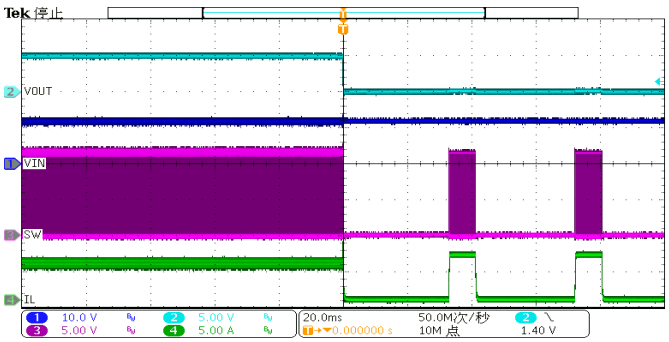


Short Entry (PFM I_{OUT}=0A)

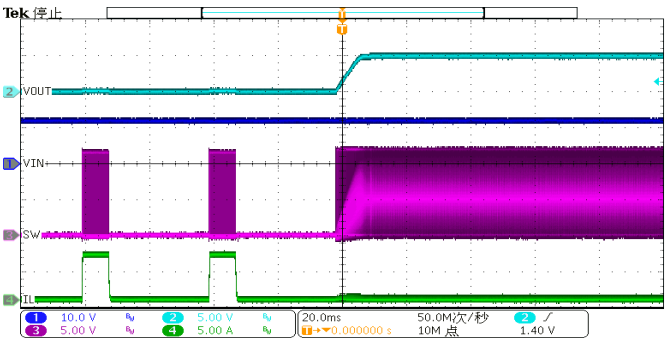
V_{IN} = 12V, V_{OUT} = 5V, C_{IN} =10uF, C_{OUT} = 44uF, L1 = 10uH, and T_A = 25°C, Frequency = 300kHz, unless otherwise noted. *(continued)*



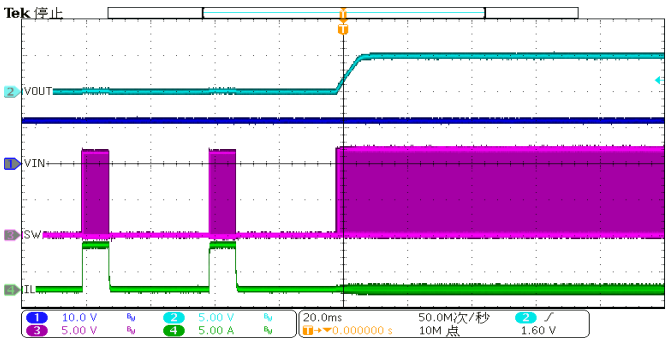
Short Entry (FPWM I_{OUT}=0A)



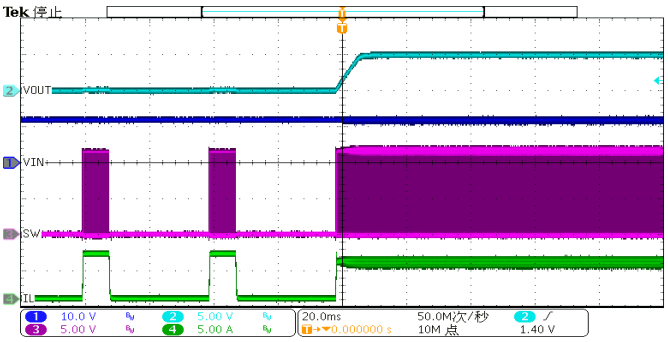
Short Entry (I_{OUT}=5A)



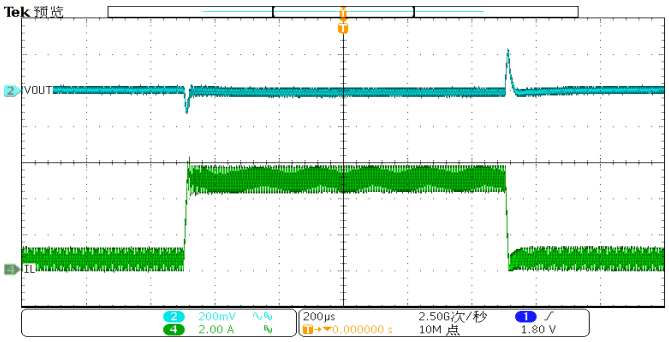
Short Recovery (PFM I_{OUT}=0A)



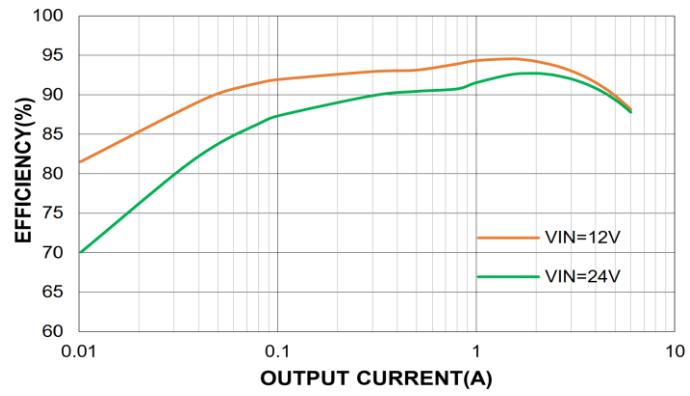
Short Recovery (FPWM I_{OUT}=0A)



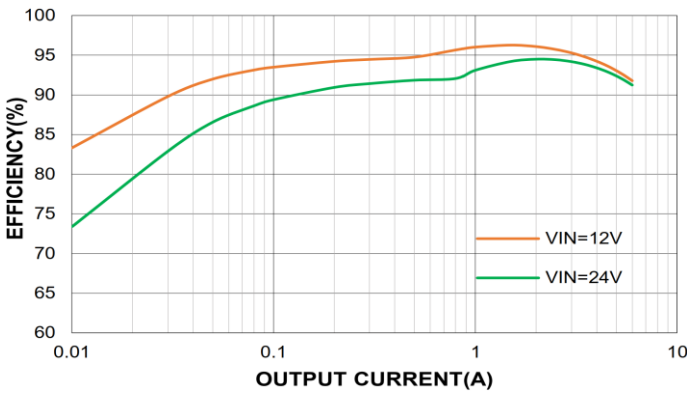
Short Recovery (I_{OUT}=5A)



Load Transient (0.5A to 5A, 3A/us)

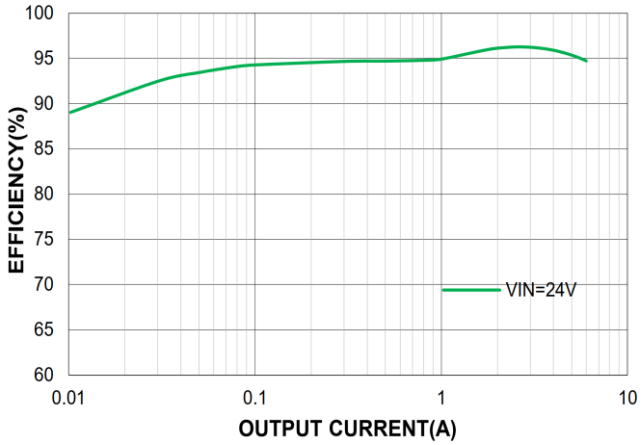


Efficiency vs. Load Current, L=6.8uH,DCR= 25mohm
V_{OUT}=3.3V

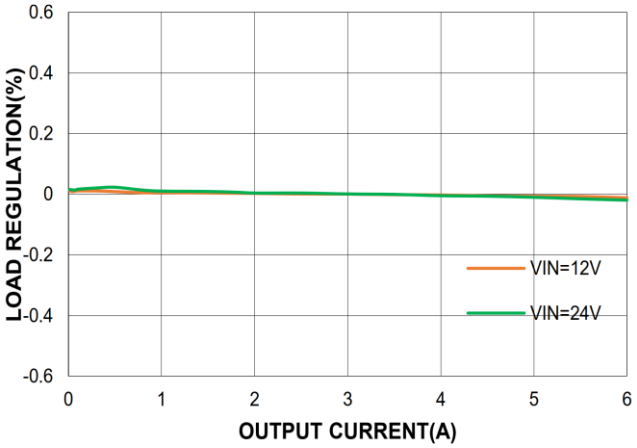


Efficiency vs. Load Current, L=10uH,DCR= 30mohm
V_{OUT}=5V

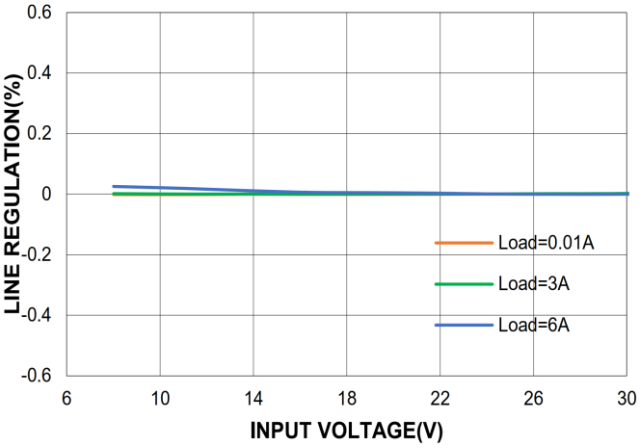
V_{IN} = 12V, V_{OUT} = 5V, C_{IN} =10uF, C_{OUT} = 4*22uF, L1 = 10uH, and T_A = 25°C, Frequency = 300kHz, unless otherwise noted. *(continued)*



Efficiency vs. Load Current, L=10uH,DCR= 30mohm V_{OUT}=12V



Load Regulation, V_{OUT}=5V



Line regulation, V_{OUT}=5V

10 Layout

10.1 Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to the figure below and follow the guidelines below and take figures as the reference.

- The high current paths (GND, VIN and SW) should be placed very close to the device with short, direct and wide traces.
- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

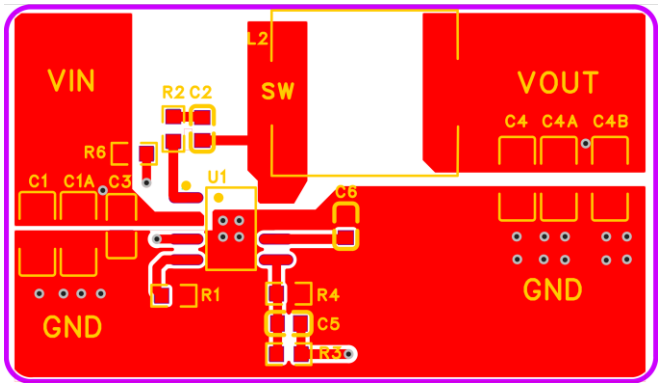


Figure10-1. Top layer

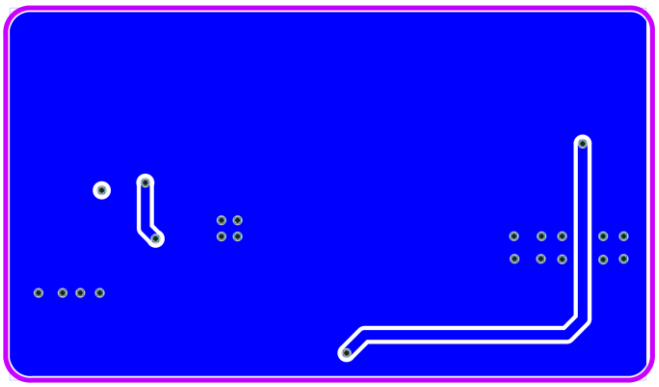
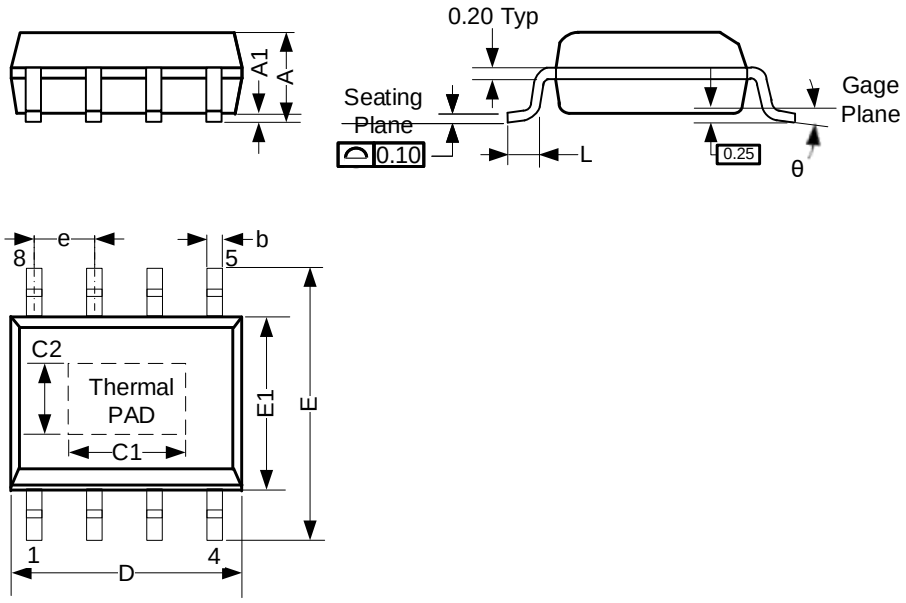


Figure10-1. Bottom layer

11 Mechanical Information

11.1 ESOP8 Mechanical Information

ESOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	–	–	1.70
A1	0.00	–	0.15
b	0.33	–	0.51
C1	3.15	–	3.45
C2	2.26	–	2.56
D	4.80	–	5.00
E	5.80	–	6.20
E1	3.80	–	4.00
e	1.27BSC		
L	0.41	–	1.27
θ	0°	–	8°

12 Notes and Revision History

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

12.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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