



**5 Orderable Information**

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ92360-QAN	FCQFN2x3-13	-40~125°C	RoHS & Green	Level 1 Unlimited	Tape and Reel 5000 Units / Reel	Active

**Note:**

**ECO PLAN:** For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

**MSL:** Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

**SORT:** Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

## 6 Pin Configuration and Marking Information

### 6.1 Pin Configuration

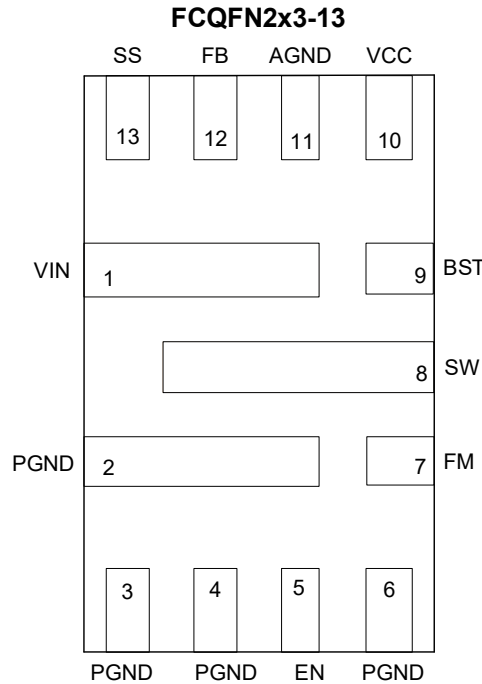


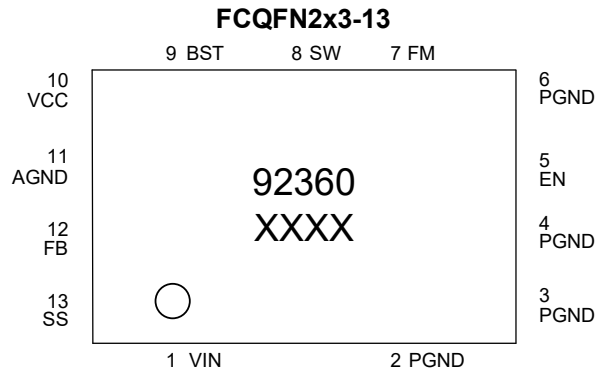
Figure 6-1 Pin Configuration

### 6.2 Pin Function

PIN		I/O <sup>(1)</sup>	DESCRIPTION
No.	NAME		
1	VIN	P	<b>Input Supply Pin.</b> VIN supplies the internal bias LDO and drain of the internal high-side FET. Place a capacitor (CIN) as close as to the IC as possible to prevent large voltage spikes from appearing at the input.
2,3,4,6	PGND	G	<b>Power Ground terminal.</b> PGND is the reference ground of the regulated output voltage. Use wide PCB traces to make the connection.
5	EN	I	<b>Enable Pin.</b> Pull high to enable Buck. Pull to GND or Float this pin to disable Buck.
7	FM	I	<b>Operation mode and frequency selection.</b> Program FM to select CCM, pulse skip mode, and the operating switching frequency. Connecting a resistor between FM pin and GND can configure the frequency.
8	SW	P	<b>Switching output of the converter.</b> Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
9	BST	P	<b>Bootstrap.</b> Connect a capacitor between SW and BST pins to form a floating supply across the High-side switch driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
10	VCC	P	<b>Internal 5V LDO regulator output.</b> Decouple VCC with a 1μF capacitor. The VCC LDO shutdown when EN is pulled low.
11	AGND	G	<b>Analog ground.</b> Connect AGND to PGND.
12	FB	I	<b>Feedback input to the converter.</b> Connect a resistor divider to set the output voltage.
13	SS	I	<b>Soft-Start Program Pin.</b> Connect a capacitor (Recommend 10nF~100nF) between SS pin to GND to set the Soft start slew rate. SS pin can't be float

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



92360: Device number.  
XXXX: Code, indicates weekly record information.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

$T_{amb}=25^{\circ}\text{C}$ , unless otherwise specified.<sup>(1)</sup>

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{IN}$	VIN to GND	-	-0.3	31	V
$V_{SW}$	SW to GND	-	-0.7(-5V in 10ns)	$V_{IN}+0.7$	V
$V_{EN}$	EN to GND	-	-0.3	31	V
$V_{BST} - V_{SW}$	BST to SW	-	-0.3	6	V
All Other Pins		-	-0.3	6	V
$T_{STG}$	Storage temperature	-	-65	150	$^{\circ}\text{C}$
$T_J$	Junction temperature	-	-40	150	$^{\circ}\text{C}$

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

### 7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{BST} - V_{SW}$	BST to SW	-	4	-	5	V
$V_{IN}$	VIN to GND	-	3.6	-	30	V
$V_{OUT}$	VOUT to GND	-	0.6	-	$V_{IN}$	V
$I_{OUT}$	Max continuous output current	-	-	6	-	A

### 7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) <sup>(1)</sup>	$\pm 1000$	V
$V_{ESD-CDM}$	Electrostatic discharge	Charged device model	$\pm 2000$	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

### 7.4 Thermal Information

SYMBOL	THERMAL METRIC	RATING	UNIT
$R_{\theta JC}$	Junction to case(top) thermal resistance	8	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Junction to ambient thermal resistance	32	$^{\circ}\text{C}/\text{W}$

**Note:** Measured on DEMO board 4-layer PCB, 63mmx48mm board.

**7.5 Electrical Characteristics**
 $V_{IN}=12V$ ,  $V_{EN}=2V$ ,  $T_A=25^{\circ}C$ , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Input UVLO and Quiescent Current</b>						
$V_{IN_{UVR}}$	VIN UVLO rising threshold	-	-	3.3	-	V
$V_{IN_{UVF}}$	VIN UVLO falling threshold	-	-	2.8	-	V
$V_{IN_{UV\_hys}}$	VIN UVLO hysteresis	-	-	0.5	-	V
$I_{QS}$	Shutdown supply current	$V_{EN} < 0.3V$ , $V_{IN}=12V$	-	1	3	$\mu A$
$I_Q$	Quiescent supply current	$V_{IN}=12V$ , No load, $V_{FB} = 0.83V$ , no switching	-	350	-	$\mu A$
<b>VCC Regulator</b>						
$V_{CC}$	VCC regulator	$V_{IN} > 5.2V$	-	5	-	V
$I_{VCC}$	VCC current limit	High to low	20	-	-	mA
<b>High Side and Low Side MOSFETs</b>						
$LK_{GHS}$	High-side leakage	$V_{EN} = 0V$ , $V_{SW} = 0V$	-	-	1	$\mu A$
$LK_{GLS}$	Low-side leakage	$V_{EN} = 0V$ , $V_{SW} = 18V$	-	-	1	$\mu A$
$R_{ON\_HS}$	High-side switch on resistance	$V_{BST-SW} = 5V$	-	32	-	m $\Omega$
$R_{ON\_LS}$	Low-side switch on resistance	$V_{IN} = 12V$	-	20	-	m $\Omega$
<b>Output Discharge Resistor</b>						
$R_{Discharge}$		-	-	200	-	$\Omega$
<b>Feedback Voltage and SS</b>						
$V_{FB}$	Feedback voltage	$T_a=25^{\circ}C$	591	600	609	mV
$I_{LK\_FB}$	Feedback leakage	$V_{EN} = 1V$ , $V_{FB} = 2V$	-	-	0.1	$\mu A$
$I_{SS}$	Soft-start current	-	-	10	-	$\mu A$
<b>Switching Frequency</b>						
$F_{SW}$	Oscillator frequency	FM=PGND, PFM	-	250	-	kHz
		FM=30k, PFM	-	300	-	kHz
		FM=75k, PFM	-	400	-	kHz
		FM=150k, CCM	-	400	-	kHz
		FM=270k, CCM	-	300	-	kHz
		FM Float, CCM	-	250	-	kHz
$T_{ON\_MIN}$	Minimum switch on time	-	-	70	-	ns
$T_{OFF\_MIN}$	Minimum switch off time	-	-	150	-	ns
$FB_{UV}$	FB UV hiccup	-	-	75%	-	$V_{FB}$
$T_{OTP\_R}$	Thermal shutdown <sup>(1)</sup>	-	-	160	-	$^{\circ}C$
$T_{OTP\_Hys}$	OTP hysteresis <sup>(1)</sup>	-	-	30	-	$^{\circ}C$
$D_{MAX}$	Maximum duty cycle	-	-	100	-	%

<b>Current Limit</b>						
I <sub>LIM_LS</sub>	Low-Side current valley limit	-	-	7	-	A
I <sub>LIM_HS</sub>	High-Side current peak limit	-	-	8	-	A
I <sub>NOC</sub>	Negative current limit	-	-	4	-	A
<b>Enable</b>						
V <sub>EN_R</sub>	EN rising threshold	Low to high	-	1.25	-	V
V <sub>EN_F</sub>	EN falling threshold	High to low	-	1.05	-	V
V <sub>EN_Hys</sub>	EN threshold hysteresis	-	-	0.2	-	V
R <sub>EN</sub>	Enable input resistor	-	-	2400	-	kΩ
<b>VO<sub>UT</sub> OVP/UVP threshold</b>						
V <sub>OVP_rising_th</sub>	Output OVP rising threshold	-	-	115%	-	V <sub>FB</sub>
V <sub>OVP_falling_th</sub>	Output OVP falling threshold	-	-	105%	-	V <sub>FB</sub>
V <sub>UVP_falling_th</sub>	UVP falling threshold	-	-	75%	-	V <sub>FB</sub>
V <sub>UVP_rising_th</sub>	UVP rising threshold	-	-	85%	-	V <sub>FB</sub>

(1) Guaranteed by design and engineering sample characterization.

## 8 Detailed Description

### 8.1 Overview

The CJ92360 device is an easy-to-use synchronous step-down buck converter, which integrated low on resistance high-side and low-side power MOSFETs. The CJ92360 can deliver 6A of output current efficiently with constant on time (COT) control for fast loop response.

This CJ92360 achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

This CJ92360 device has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuits protection, FB open short protection and thermal shutdown in case of excessive power dissipation. The CJ92360 is available in a space-saving FCQFN2x3-13 package.

### 8.2 Functional Block Diagram

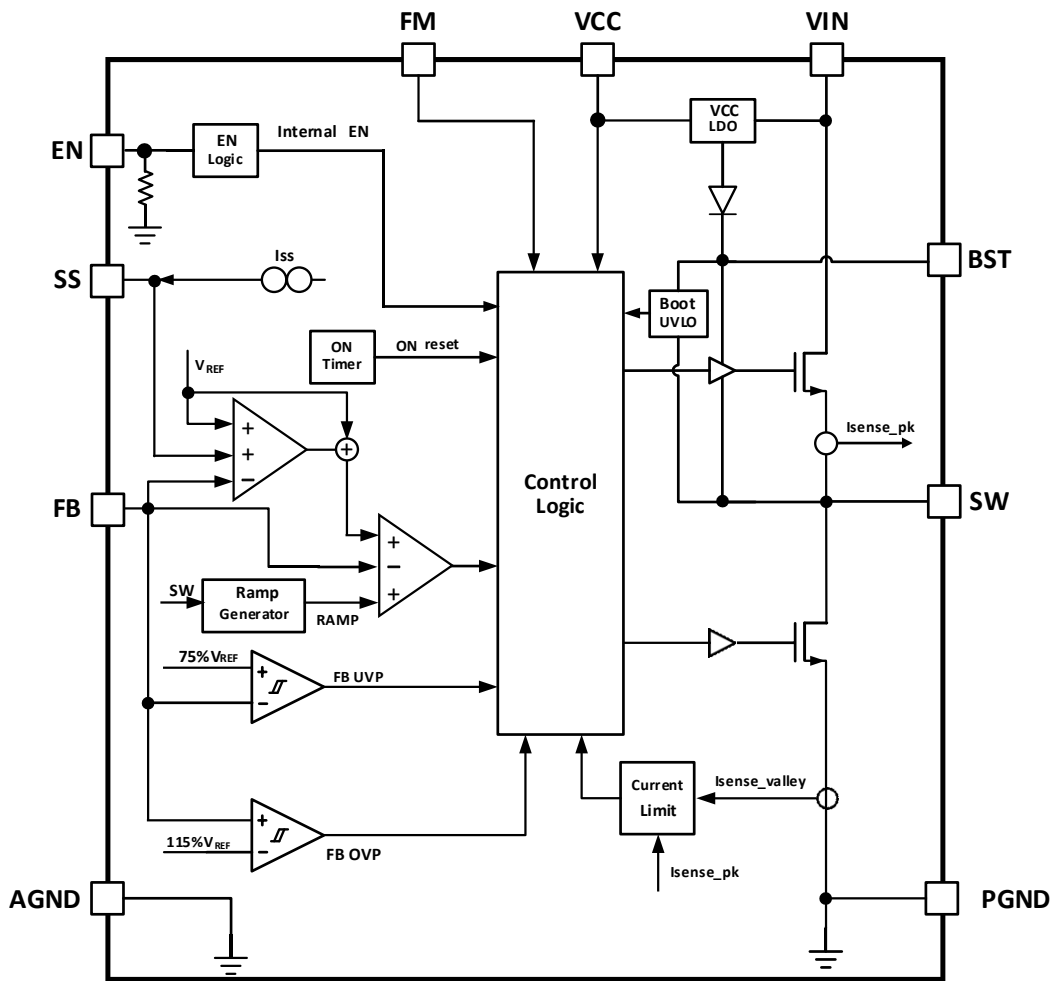


Figure 8-1 Function Block Diagram

### 8.3 Feature Description

#### 8.3.1 Pulse-Width Modulation (PWM) Control

The CJ92360 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (VFB) is below the reference voltage (VREF), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when VFB drops below VREF. By repeating operations this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affecting the line or load regulation.

#### 8.3.2 Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high, and the inductor current is always above zero amps. When VFB is below VREF, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period begins. In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

#### 8.3.3 Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM). It works in Light-load operation mode. When VFB is below VREF, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, VFB cannot reach VREF while the inductor current is approaching zero. The LS-FET driver enters tri-state (Hi-Z) whenever the inductor current reaches zero. The output capacitors discharge to GND through the LS-FET slowly. As a result, the efficiency in light-load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the CJ92360 reduces the switching frequency naturally. High efficiency is achieved at light load

As the output current increases from the light-load condition, the current modulator regulation time becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with the following Equation:

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L_{OUT} \times F_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

**8.3.4 Under-Voltage Lockout (UVLO) Protection**

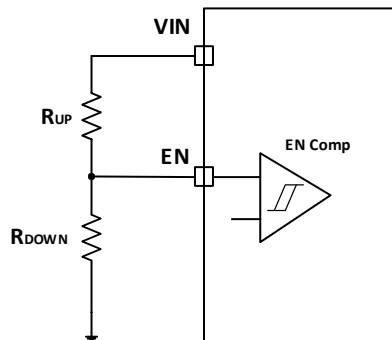
The CJ92360 has under-voltage lockout (UVLO) protection: the part starts up only when VIN/VCC UVLO threshold (3.3V typically). The part shuts down when the VIN/VCC voltage is lower than the UVLO falling threshold voltage (typically 2.8V), the UVLO protection is non-latch off.

**8.3.5 Enable (EN) Control**

EN is used to enable or disable the entire chip. Pull EN high (>1.25V typically) to turn on the regulator. Pull EN low (<1.05V typically) to turn off the regulator. For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. To determine the automatic start-up voltage, calculate the values of the pull-up resistor (R<sub>UP</sub> from VIN to EN) and the pull-down resistor (R<sub>DOWN</sub> from EN to GND) with the below.

$$VIN\_start = \frac{1.25V \times (R_{UP} + R_{DOWN})}{R_{DOWN}} \tag{2}$$

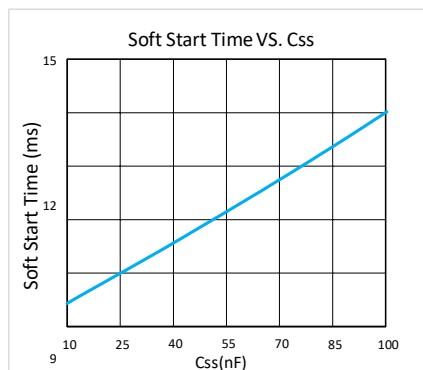
If an application requires a higher UVLO, use EN to adjust the input voltage UVLO by using two external resistors (see the below figure).



**Figure 8-2 Adjustable UVLO Application Circuits**

**8.3.6 Soft Start (SS)**

The CJ92360 employs a soft-start mechanism to ensure a smooth output during power-up. When the chip starts (both EN>1.25V and VIN/VCC is above UVLO), an internal current source charges up the SS capacitor. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time can be programmable by connecting a capacitor between SS pin and GND pin, the relationship of soft-start time and SS capacitor as shown below (See Figure 8-3).

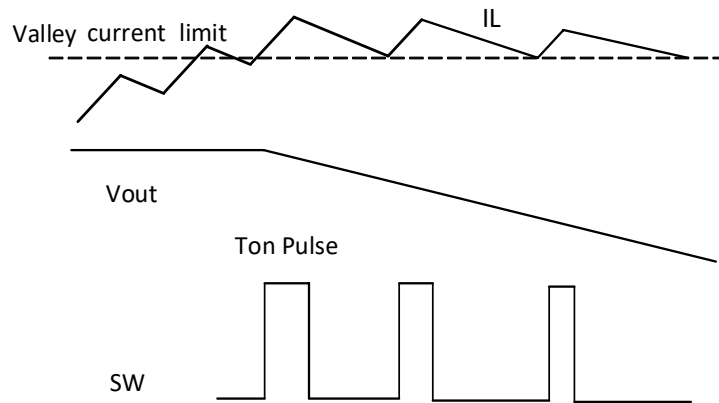


**Figure 8-3 Soft – Start Time VS. C<sub>SS</sub>**

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

**8.3.7 Over-Current limit (OCL)**

The CJ92360 has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the LS limit compactor active. The device enters over the current protection mode. High side will not be turned on until the valley current limit disappears. Meanwhile, the output voltage drops until VFB is below the under voltage (UV) threshold (typically 75% of the reference). Once UV is triggered, the CJ92360 enters hiccup mode to restart the part periodically. During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over- current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection (see the Figure below).



**Figure 8-4 Valley Current-Limit Control**

Since the comparison is done during the LSFET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (IOC) can be calculated with the following Equation:

$$I_{OC} = I_{LIMIT} + \frac{\Delta I_{inductor}}{2} \tag{3}$$

The OCL itself limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, causing the output voltage to fall off. Eventually, the current crosses the under-voltage protection (UVP) threshold and enters the hiccup protection.

**8.3.8 OVP/UVP**

The CJ92360 monitors a resistor-divided VFB to detect over- and under-voltage. When VFB becomes higher than 115% of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the circuit will turn on the low side MOSFET to discharge the output. LSFET will turn off until the negative current limit is triggered then LSFET will remain off for 5us to turn on again. IC will repeat this behavior until the output OVP condition is removed.

When VFB drops below 75% of VREF, the UVP comparator output goes high, and the CJ92360 enters the hiccup protection.

### 8.3.9 FM Select Frequency/Mode Programmable

The CJ92360 can set up the operation mode and PWM frequency by connecting FM pin to GND with a resistor. Below table shows the configuration.

**Table 1: Frequency and Mode Configuration**

R <sub>FM</sub> (kΩ)	MODE	SWITCHING FREQUENCY (kHz)
0	PFM	250
30	PFM	300
75	PFM	400
150	FPWM	400
270	FPWM	300
Float	FPWM	250

### 8.3.10 Large Duty Cycle Operation

When CJ92360 will automatically extend the frequency to support the application when V<sub>IN</sub> is close to V<sub>OUT</sub>. The frequency extend circuit will be triggered when T<sub>OFF</sub> min time is reached. The CJ92360 can support up to 100% duty cycle. Large duty cycle operation is disabled when OC is triggered.

### 8.3.11 Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

### 8.3.12 Output Discharge

During the EN off period, the output is discharged via a 200Ω resistor on the SW. This discharge FET is turned off when V<sub>OUT</sub> is fully discharged or the 10ms timer is finished.

## 9 Application Implementation

### 9.1 Typical Application Circuit

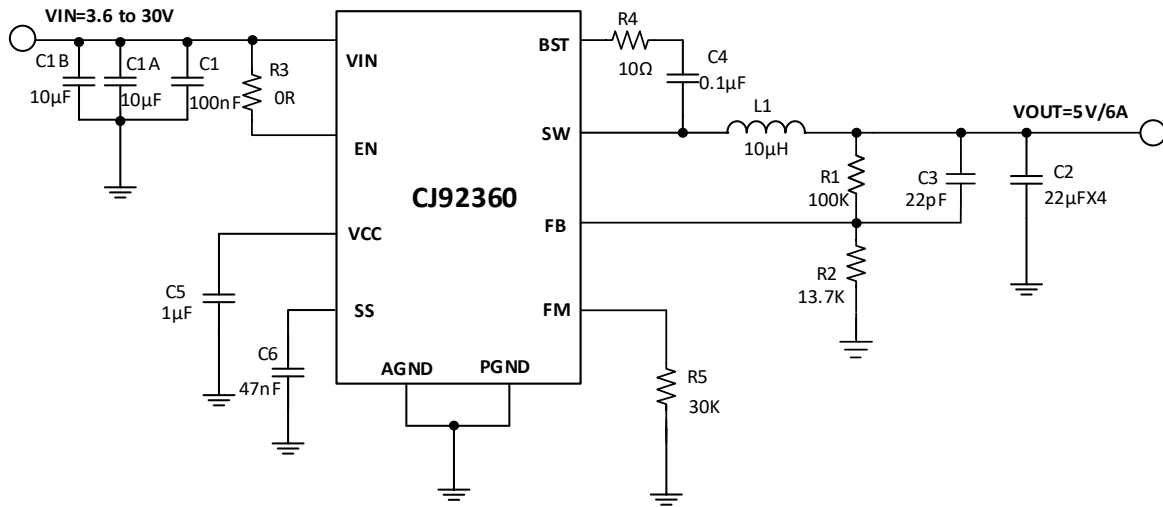


Figure 9-1 Typical  $V_{OUT}=5V/6A$  application

Table 2: Frequency Setting

R5 (kΩ)	MODE	SWITCHING FREQUENCY (kHz)
GND	DCM	250
30		300
75		400
150	CCM	400
270		300
Float		250

9.2 Application Selection

9.2.1 Setting the Output Voltage

The CJ92360 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.6V. The feedback network is shown below Figure.

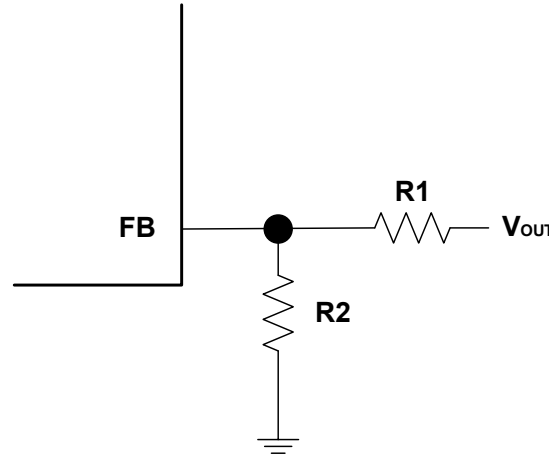


Figure 9-2 Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT} = \frac{V_{FB}(R_1 + R_2)}{R_2} \tag{4}$$

Table 3 lists the recommended feedback resistor values for common output voltages.

Table 3: Resistor Selection For Common Output Voltages <sup>(1) (2)</sup>

V <sub>IN</sub> (V)	V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)	C3 (pF)	L <sub>OUT</sub> (μH)	C <sub>OUT</sub> (μF)
12	5	100	13.7	22	6.8	22x4
	9	193	13.7	22	6.8	22x4
20.5	5	100	13.7	22	10~15	22x4
	9	193	13.7	22	10~15	22x4
	12	261	13.7	22	10~15	22x4
	15	330	13.7	22	10~15	22x4
	20	442	13.7	22	10~15	22x4

(1) For a detailed design circuit, please refer to the Typical Application Circuit

(2) The table recommends parameters based on F<sub>sw</sub>=300kHz

9.2.2 Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 60% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by the equation as below:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \tag{5}$$

Where  $\Delta I_L$  is the inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \tag{6}$$

Table 4 lists the recommended values of inductors at different frequency:

**Table 4: Power Inductor Selection**

V <sub>IN</sub> (V)	F <sub>sw</sub> (kHz)	L1 (μH)
12	250	8.2
	300	6.8
	400	4.7
20.5	250	15
	300	10
	400	6.8

### 9.3 Selecting Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the stepdown converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations. The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{7}$$

The worst case occurs at V<sub>IN</sub> = 2V<sub>OUT</sub>, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \tag{8}$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{9}$$

Under worse-case is where V<sub>IN</sub> = 2V<sub>OUT</sub>.

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \tag{10}$$

### 9.4 Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right) \quad (11)$$

Where L is the inductor value, and  $R_{ESR}$  is the equivalent series resistance (ESR) value of the output capacitor,  $F_{OSC}$  is the switching frequency. Note that, in real application, should consider that the ceramic capacitor capacitance has derating.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple caused by ESR is very small. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{8 \times F_{OSC} \times C_{OUT}}\right) \quad (12)$$

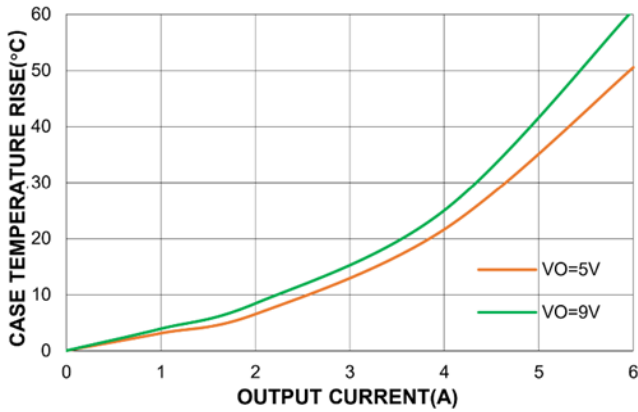
In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (13)$$

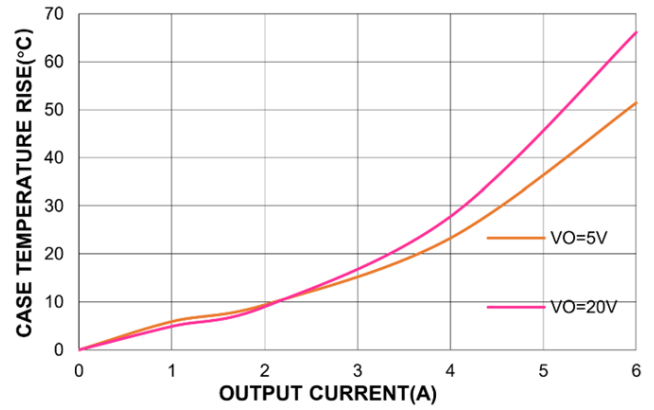
The characteristics of the output capacitor also affect the stability of the regulation system. The CJ92360 can be optimized for a wide range of capacitance and ESR values.

### 9.5 Typical Performance Characteristics

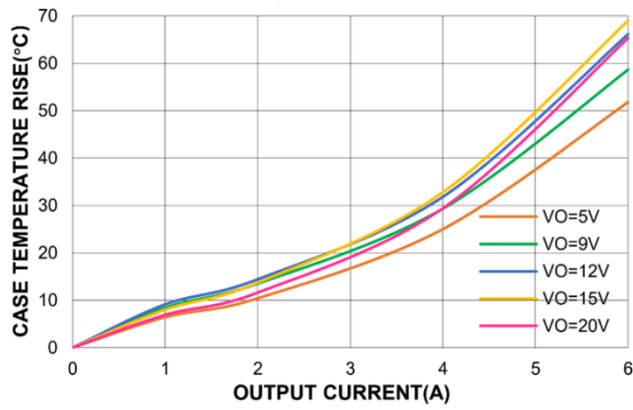
$V_{IN} = 12/24V$ ,  $V_{OUT} = 5V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 4 \times 22\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



Case Temperature Rise vs. Load Current,  $V_{IN}=12V$

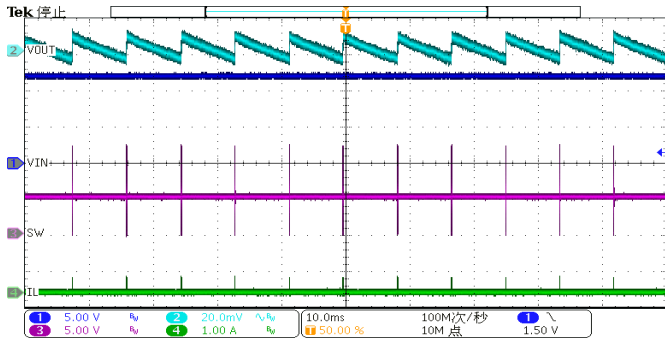


Case Temperature Rise vs. Load Current,  $V_{IN}=20.5V$

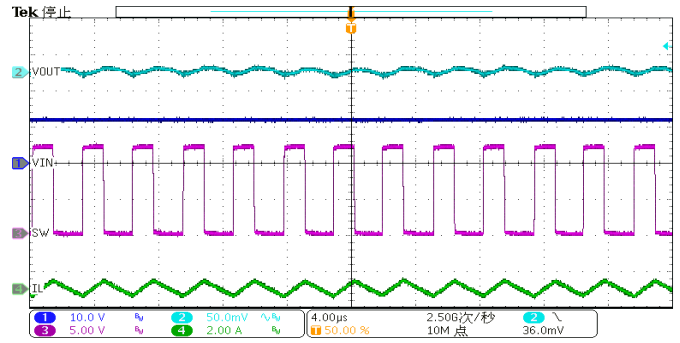


Case Temperature Rise vs. Load Current,  $V_{IN}=24V$

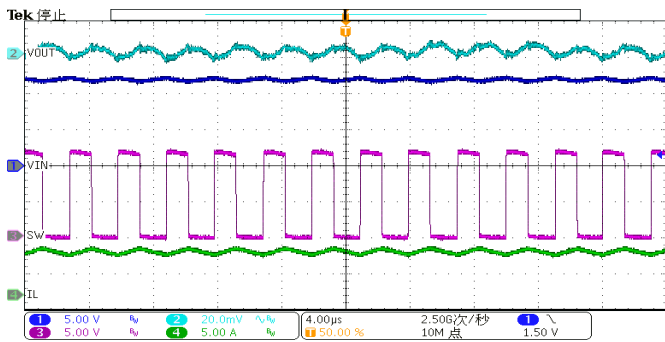
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 4 \times 22\mu F$ ,  $L1 = 10\mu H$ , and  $T_A = +25^\circ C$ , Frequency = 300kHz, unless otherwise noted.



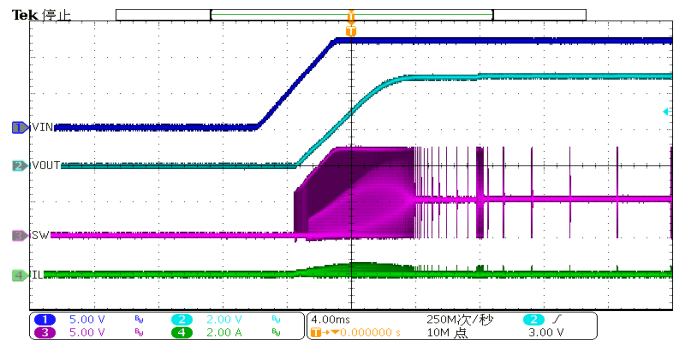
Output Voltage ripple (PFM,  $I_{OUT}=0A$ )



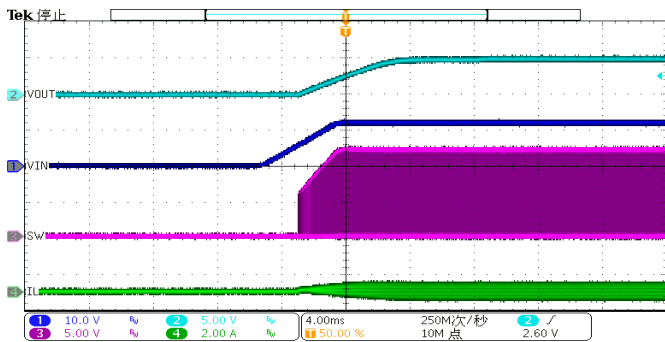
Output Voltage ripple (FPWM,  $I_{OUT}=0A$ )



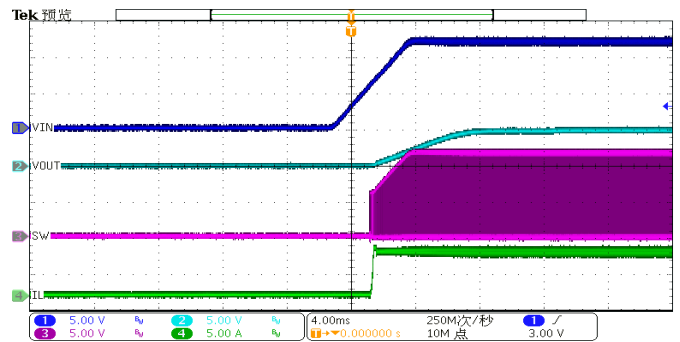
Output Voltage ripple ( $I_{OUT}=6A$ )



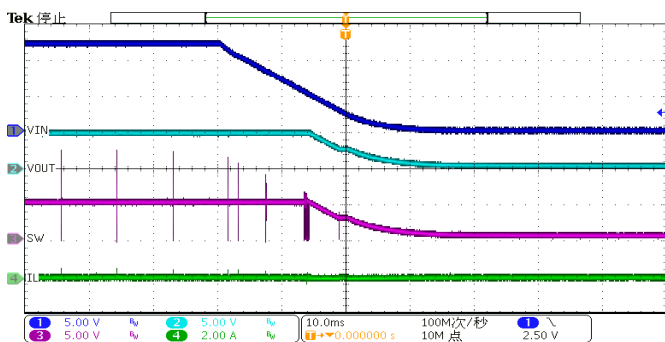
Start - Up through VIN (PFM,  $I_{OUT}=0A$ )



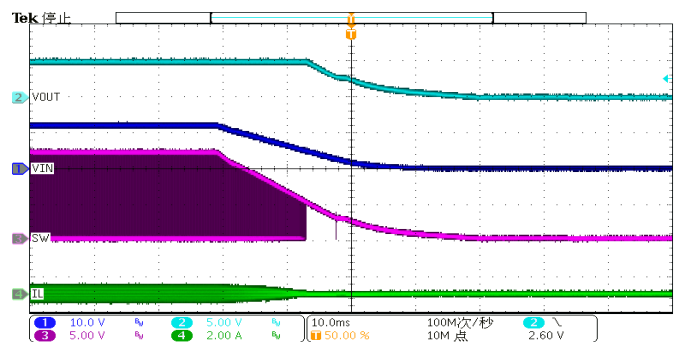
Start - Up through VIN (FPWM,  $I_{OUT}=0A$ )



Start - Up through VIN ( $I_{OUT}=6A$ )

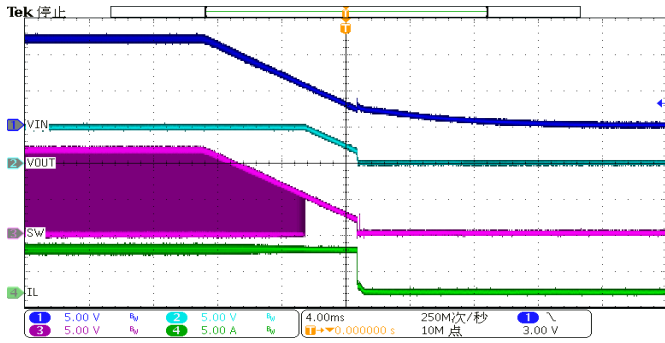


Shutdown through VIN (PFM,  $I_{OUT}=0A$ )

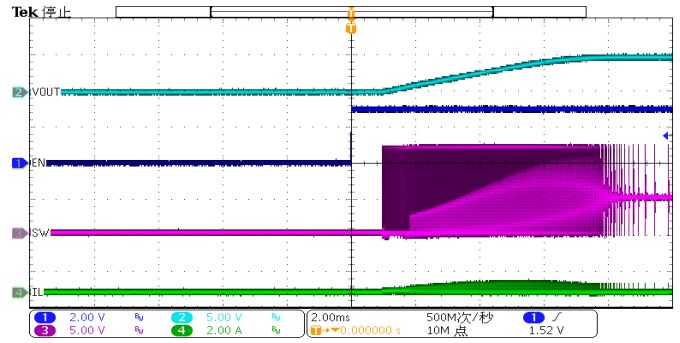


Shutdown through VIN (FPWM,  $I_{OUT}=0A$ )

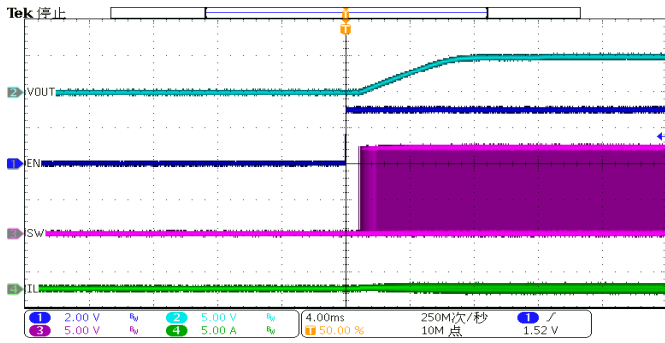
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 4 \times 22\mu F$ ,  $L1 = 10\mu H$ , and  $T_A = +25^\circ C$ , Frequency = 300kHz, unless otherwise noted.



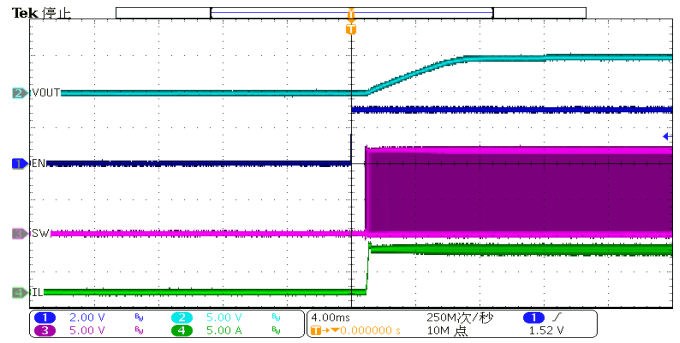
Shutdown through VIN ( $I_{OUT}=6A$ )



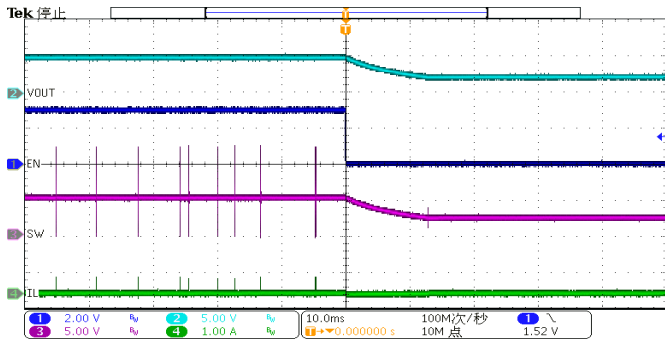
Start – Up through EN (PFM,  $I_{OUT}=0A$ )



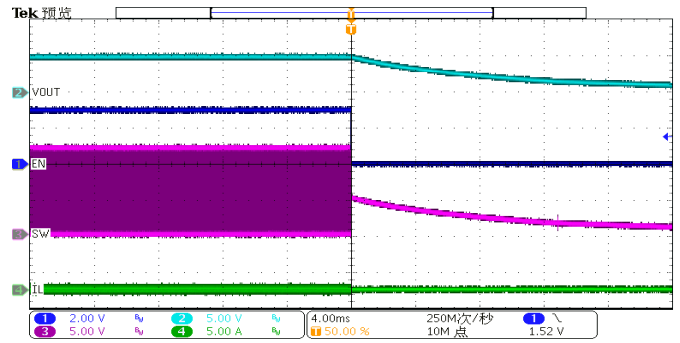
Start – Up through EN (FPWM,  $I_{OUT}=0A$ )



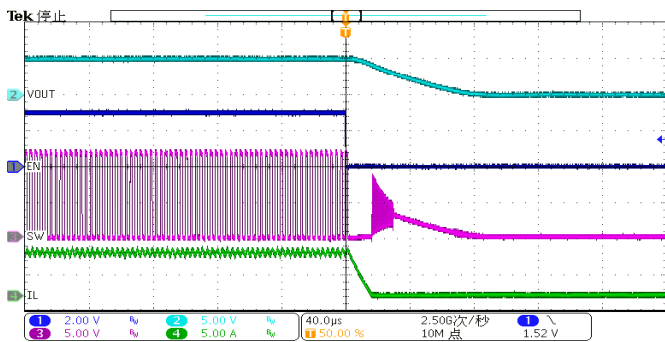
Start – Up through EN ( $I_{OUT}=6A$ )



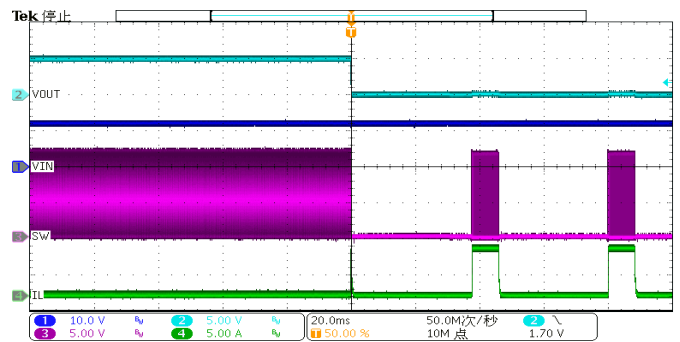
Shutdown through EN (PFM,  $I_{OUT}=0A$ )



Shutdown through EN (FPWM,  $I_{OUT}=0A$ )

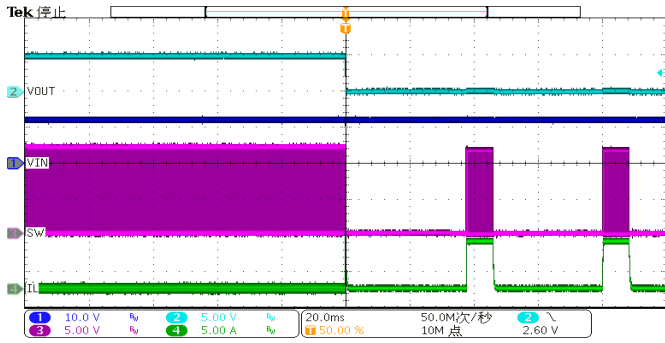


Shutdown through EN ( $I_{OUT}=6A$ )

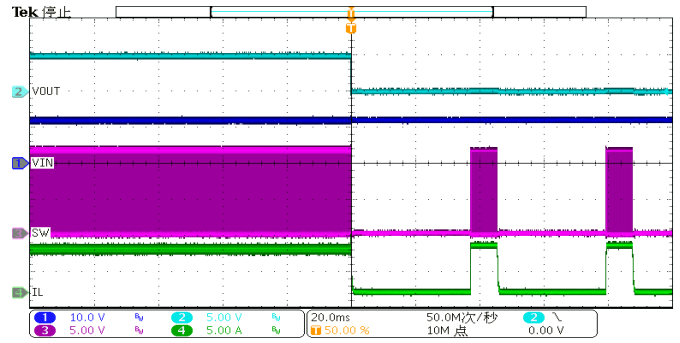


Short Entry (PFM  $I_{OUT}=0A$ )

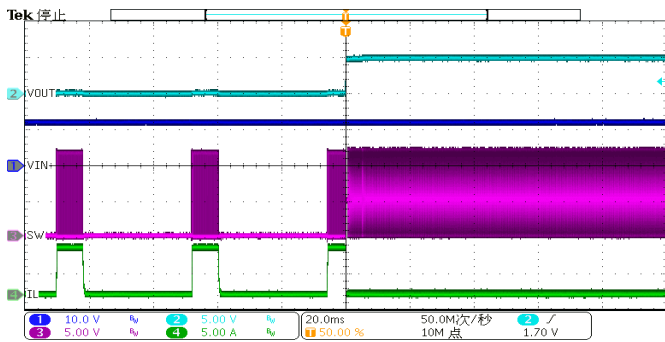
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 4 \times 22\mu F$ ,  $L1 = 10\mu H$ , and  $T_A = +25^\circ C$ , Frequency = 300kHz, unless otherwise noted.



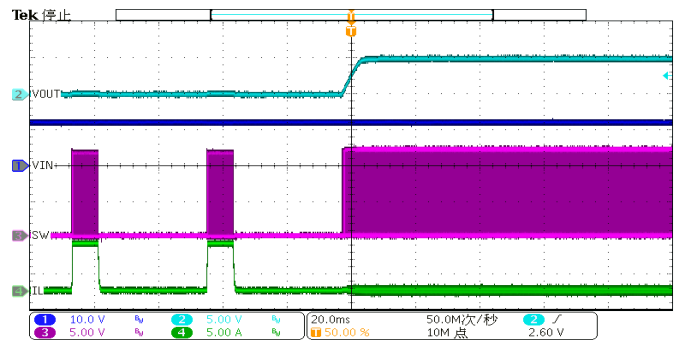
Short Entry (FPWM  $I_{OUT}=0A$ )



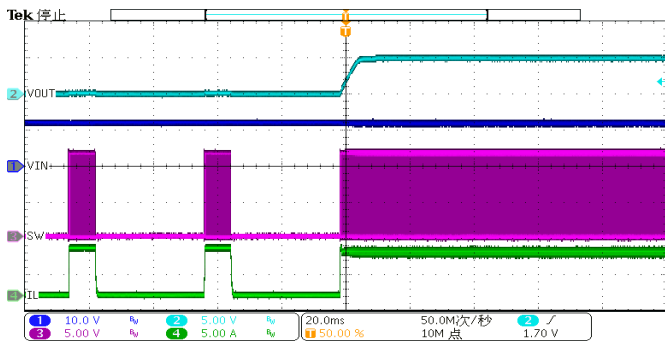
Short Entry ( $I_{OUT}=6A$ )



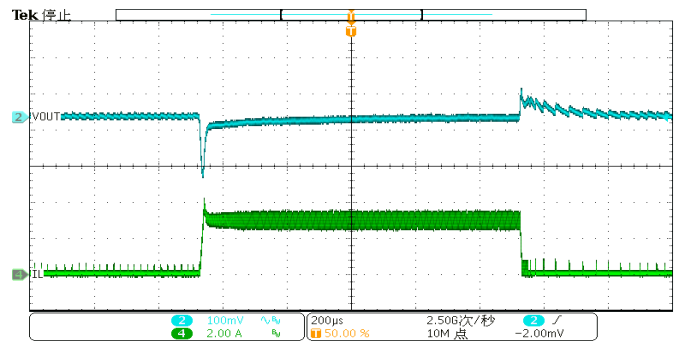
Short Recovery (PFM  $I_{OUT}=0A$ )



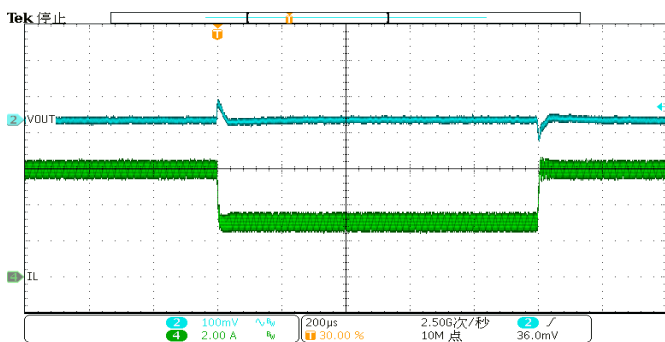
Short Recovery (FPWM  $I_{OUT}=0A$ )



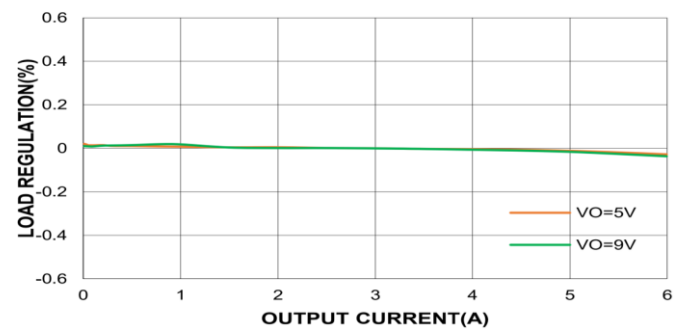
Short Recovery ( $I_{OUT}=6A$ )



Load Transient (0A to 3A,  $2.5A/\mu s$ )

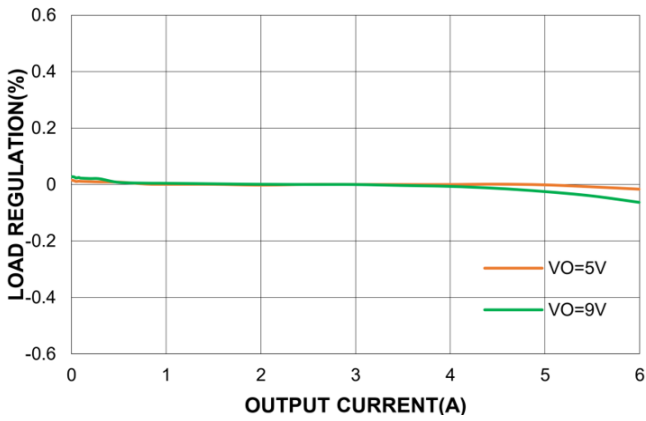


Load Transient (3A to 6A,  $2.5A/\mu s$ )

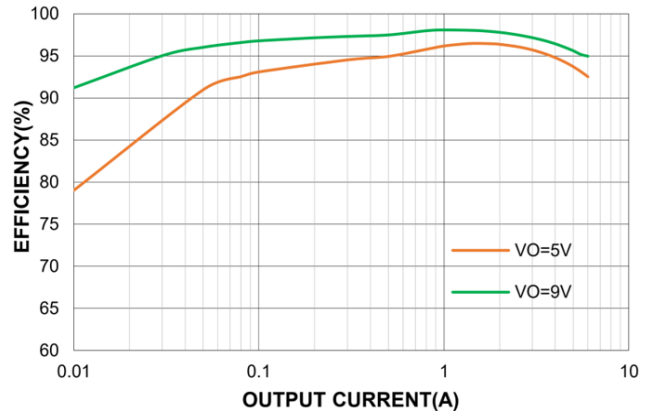


Load Regulation,  $V_{IN}=24V$

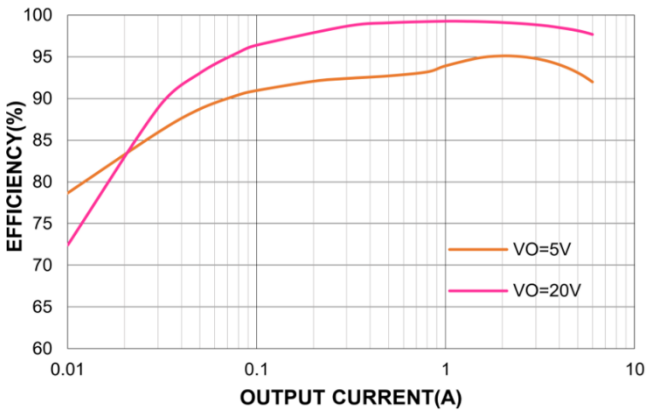
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 4 \times 22\mu F$ ,  $L1 = 10\mu H$ , and  $T_A = +25^\circ C$ , Frequency = 300kHz, unless otherwise noted.



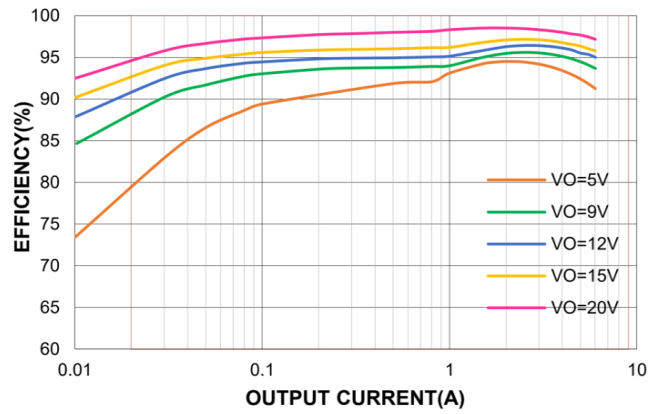
Load Regulation,  $V_{IN}=12V$



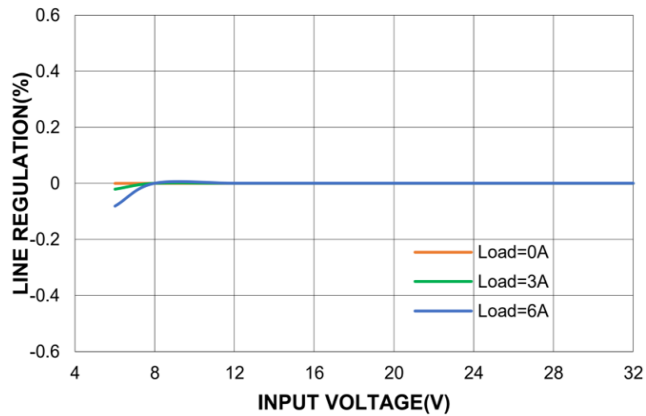
Efficiency vs. Load Current  
( $L=10\mu H, DCR= 30mohm V_{IN}=12V$ )



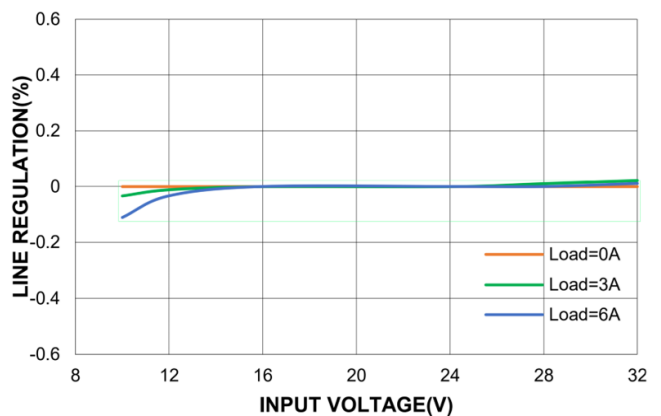
Efficiency vs. Load Current  
( $L=10\mu H, DCR= 30mohm V_{IN}=20.5V$ )



Efficiency vs. Load Current  
( $L=10\mu H, DCR= 30mohm V_{IN}=24V$ )



Line regulation,  $V_{OUT}=5V$



Line regulation,  $V_{OUT}=9V$

## 10 Layout

### 10.1 Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to the figure below and follow the guidelines below and take figures as the reference.

- The high current paths (GND, VIN and SW) should be placed very close to the device with short, direct and wide traces.
- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

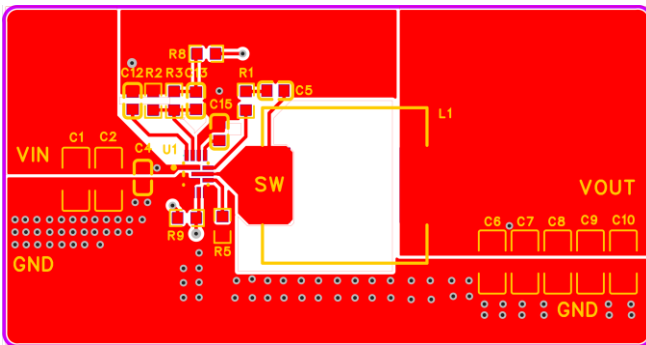


Figure 10-1 Top Layer

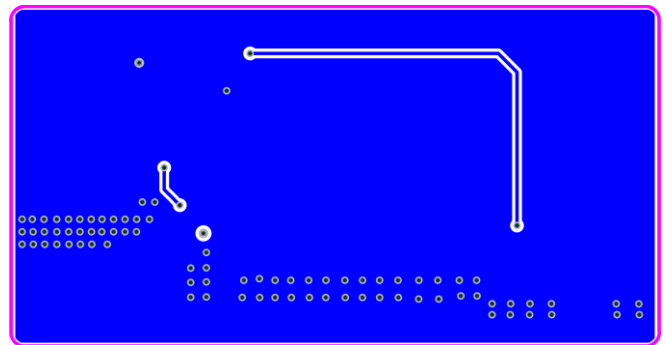


Figure 10-2 Bottom Layer

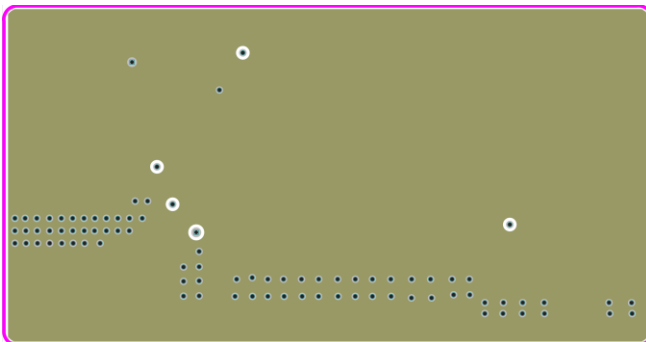


Figure 10-3 Inner1 Layer

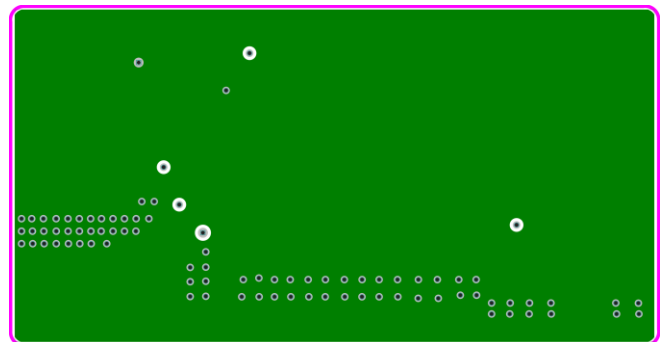
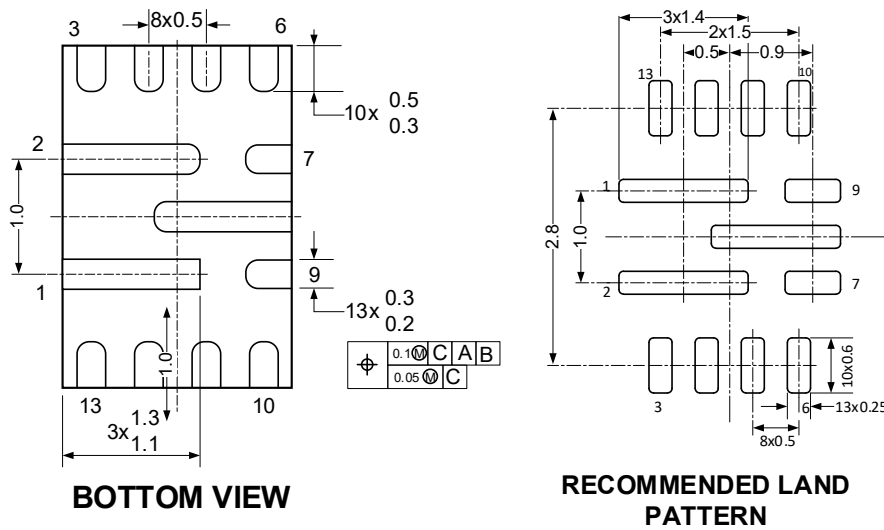
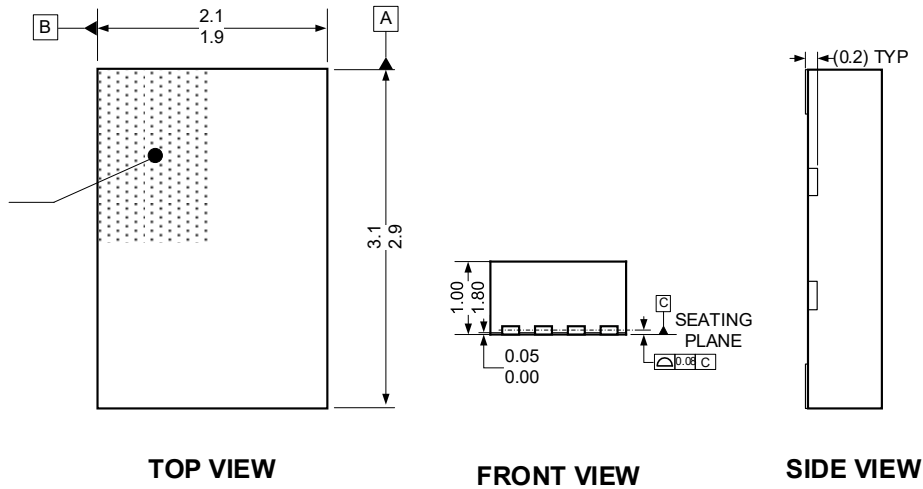


Figure 10-4 Inner2 Layer

11 Mechanical Information

11.1 FCQFN2x3-13 Mechanical Information

11.1.1 FCQFN2x3-13 Outline Dimensions



Note: All dimensions are in millimeters.

## 12 Notes and Revision History

### 12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

### 12.2 Notes

#### Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

### 12.3 Revision History

**August, 2025: rev - 1.1, Change the package name.**

**September, 2025: rev - 1.2, Change the Figure 8-1 Function Block Diagram.**

# DISCLAIMER

## IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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