70V, 3A, Asynchronous, DC-DC Step-down Converter

CJ92731 DC-DC

1 Introduction

The CJ92731 is a 70V, 3A step-down converter which is integrated with high-side power MOSFET. The CJ92731 can deliver 3A of output current efficiently with constant on time (COT) control for fast loop response.

The CJ92731 achieves high power conversion efficiency over a wide load range by scaling down its switching frequency under light-load conditions to reduce switching and gate driving losses.

The CJ92731 has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open protection and thermal shutdown.

The CJ92731 is available in a space-saving ESOP8 package.

2 Available Packages

PART NUMBER	PACKAGE
CJ92731	ESOP8

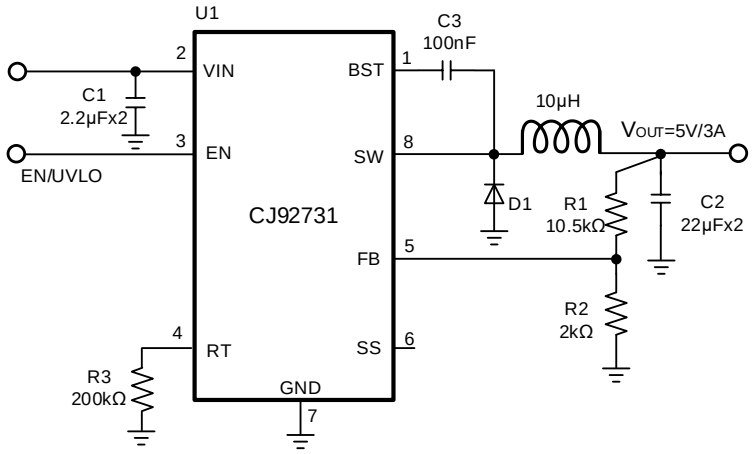
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- 4.5V to 70V Wide Input Range
- 3A Continuous Output Current
- Integrated 180mΩ low resistance high side power MOS
- Constant-On-Time Control scheme
- Soft Start Time Programmable
- Built-in Pull-up Current at EN Pin
- 150μA Low Quiescent Current
- 250kHz/500kHz Switching Frequency Selectable
- 3μA Low Input Current at Off-state
- Integrated BST refresh function
- Special Valley Current Limit for non-sync Buck Short Protection
- Low Drop Out Mode Support 97% Duty Cycle

4 Applications

- 12V, 24V and 48V Power Systems
- Surveillance Camera
- PoE Switch
- Industry applications



Typical Application Circuit

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ92731-EAN	ESOP8	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

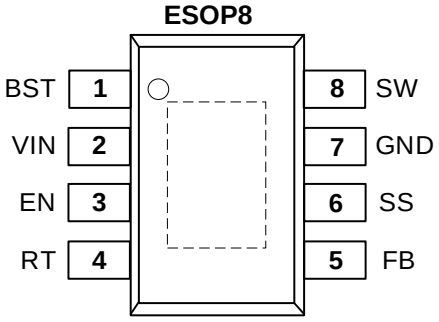


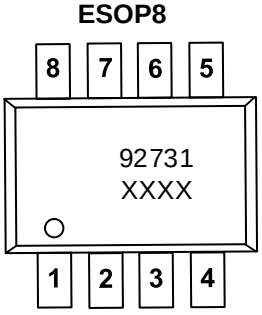
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I/O (1)	DESCRIPTION
No.	NAME		
1	BST	O	Bootstrap pin for high side power MOS driving. Connect a high-quality capacitor from this pin to the SW pin.
2	VIN	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
3	EN	I	Enable of the part. Pull down this pin to shut down the part. Internally pulled up by a current source.
4	RT	O	Frequency Set Pin. Place a resistor from RT (pin to GND) to select the switching frequency between 250kHz and 500kHz; two selections are available.
5	FB	I	Feedback. Connected to a resistor divider from VOUT to GND to set the output voltage.
6	SS	O	Soft Start Program Pin. Place a capacitor from SS pin to GND to set the soft start time. Float this pin to get 2ms (10% to 90%) fixed soft-start time.
7	GND	G	Ground of the chip. Connect to the ground of the system.
8	SW	O	Switching node of power stage. Connect to power inductor.
9	EP	G	Exposed Pad. Connect exposed pad to the PCB GND plane to achieve good thermal performance.

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



92731: Device number.

XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

T_{amb}=25°C, unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS	MIN.	MAX.	UNIT
V_{IN}	VIN to GND	-	-0.3	72	V
V_{EN}	EN to GND	-	-0.3	72	V
V_{SW}	SW to GND	-	-0.6	V_{IN}+0.3	V
V_{BST-SW}	BST to SW	-	-0.3	6	V
All Other Pins		-	-0.3	6	V
T_{STG}	Storage temperature	-	-55	150	°C
T_J	Junction temperature	-	-40	150	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	Typ.	MAX.	UNIT
V_{IN}	VIN to GND	-	4.5	-	70	V
V_{OUT}	VOUT to GND	-	0.8	-	40	V
I_{OUT}	Max Continuous Output Current	-	0	-	3	A
T_J	Junction temperature	-	-40	-	125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±2000	V
$V_{ESD-CDM}$	Electrostatic discharge	Charged Device model (CDM) (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information (2)

SYMBOL	THERMAL METRIC	ESOP8	UNIT
RΘJA	Junction-to-ambient thermal resistance	48	℃/W
RΘJC(top)	Junction to case (top) thermal resistance	52	℃/W

(2) Measured on JESD51-7, 4-Layer PCB, and the PCB has no copper for thermal dissipation. Normal PCB with copper thermal resistance will be smaller.

7.5 Electrical Characteristics

V_{IN}=48V, V_{EN}=2V, T_{amb}=25°C unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input UVLO and Quiescent Current						
VIN_{UV_R}	VIN UVLO rising threshold	-	-	4.25	-	V
VIN_{UV_F}	VIN UVLO falling voltage	-	-	4	-	V
VIN_{UV_HYS}	Hysteresis voltage of VIN UVLO	-	-	0.25	-	V
I_Q	Quiescent current	V_{FB} = 0.85V	-	150	-	μA
I_S	Shutdown current	V_{EN} = 0V	-	3	-	μA
Enable						
V_{EN_R}	EN rising threshold	-	-	1.2	-	V
V_{EN_F}	EN falling threshold	-	-	0.95	-	V
$I_{EN\_PULL\_UP}$	EN pulled up current	EN = L	-	1	-	μA
		EN = H	-	4	-	μA
I_{EN_HYS}	EN pulled up current hysteresis	-	-	3	-	μA
Feedback Voltage						
V_{FB}	Feedback voltage	-	0.788	0.8	0.812	V
V_{FB_UV}	FB UV threshold	-	-	0.1	-	V
Power Stage						
R_{HS_ON}	HS on resistance	V_{BST}-V_{SW} = 5V	-	180	-	mΩ
I_{LKG_HS}	HS leakage current	V_{EN} = 0V, V_{SW} = 0V	-	-	1	μA
Current Limit						
I_{LIMIT_HS}	High side current limit threshold	-	-	5.9	-	A
Soft Start						
T_{SS}	SS pin floating	V_{FB} from 10% to 90%	-	2	-	ms
I_{SS_CHARGE}	SS charge current			1.7		μA
I_{SS_DIS}	SS discharge current			3.5		mA
Switching Frequency function						
F_{SW}	Switching Frequency	RT Pin float	-	250	-	kHz
		R_{RT} = 200kΩ	-	500	-	kHz
T_{ON_MIN}(1)	Min On pulse	-	-	150	-	ns
T_{ON_MAX}(1)	Max On pulse	-	-	20	-	us
T_{OFF_MIN}(1)	Min Off time	-	-	350	-	ns
Thermal Protection						
T_{OTP_R}(1)	Over temperature protection rising threshold	-	-	160	-	°C
T_{OTP_F}(1)	Over temperature protection falling threshold	-	-	140	-	°C

(1) Guaranteed by design and engineering sample characterization.

8 Detailed Description

8.1 Overview

The CJ92731 is a 70V, 3A step-down converter which is integrated with high- side power MOSFET. The CJ92731 can deliver 3A of output current efficiently with constant on time (COT) control for fast loop response.

The CJ92731 achieves high power conversion efficiency over a wide load range by scaling down its switching frequency under light-load conditions to reduce switching and gate driving losses.

The CJ92731 has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open protection and thermal shutdown.

8.2 Functional Block Diagram

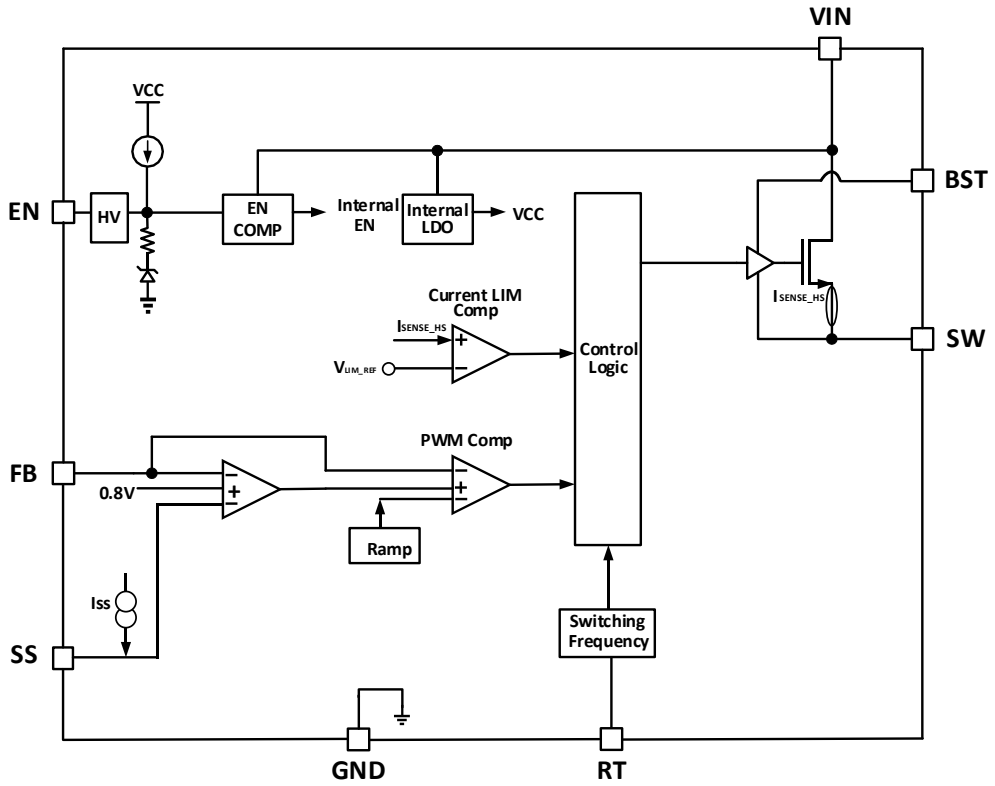


Figure 8-1 Function block diagram

8.3 Feature Description

8.3.1 Pulse-Width Modulation (PWM) Operation

The CJ92731 is a fully integrated, non-synchronous, step-down converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on-period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on-period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

8.3.2 Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 8-2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the external free-wheeling diode will handle the current.

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

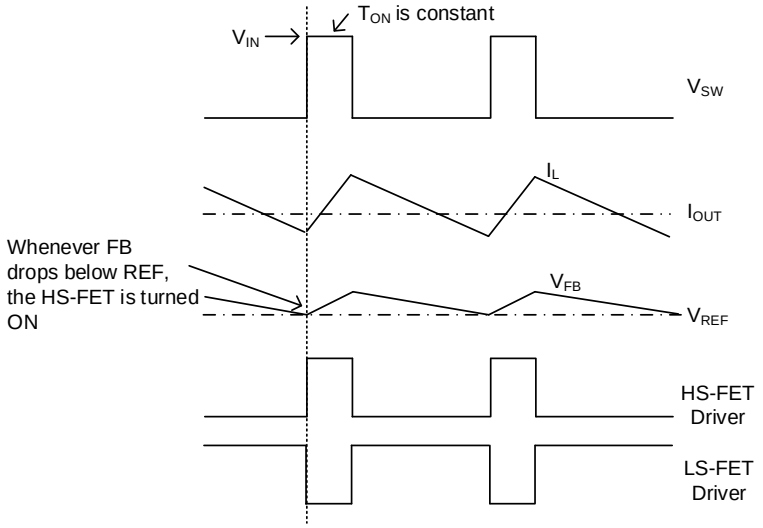


Figure 8-2 Heavy-Load Operation

8.3.3 Light-Load Operation

In non-synchronize application, the diode is used. When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 8-3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on- timer. When the HS-FET is turned off, the free- wheeling diode is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The free-wheeling diode will shut down the negative current and IC goes into tri-state. The output capacitors discharge to GND through the feedback resistor slowly. As a result, the efficiency in light- load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the CJ92731 reduces the switching frequency naturally. High efficiency is achieved at light load.

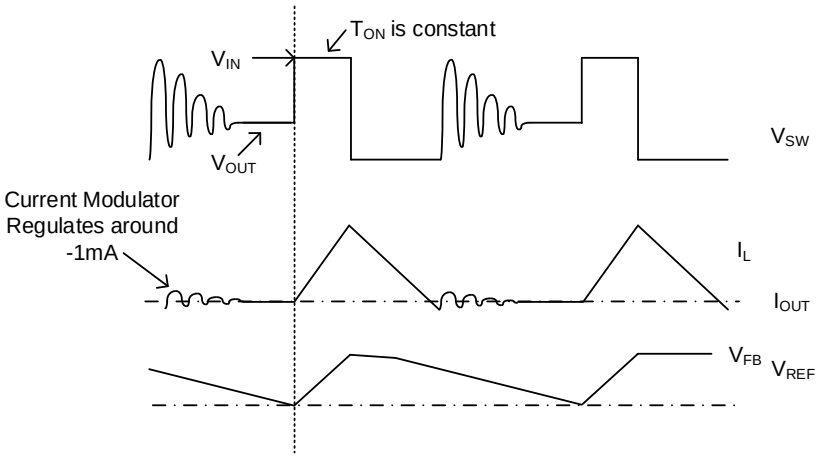


Figure 8-3 Light-Load Operation

As the output current increases from the light-load condition, the HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times 2 \times L \times f_{sw}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

8.3.4 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The CJ92731 UVLO comparator monitors the input voltage. The UVLO rising threshold is about 4.25V, while its falling threshold is consistently 4V.

8.3.5 Enable (EN) Control

The CJ92731 has a dedicated enable control pin with positive logic. Drive EN pin voltage higher than 1.2V(typical) to turn on the regulator, and drive EN pin voltage lower than 0.95V(typical) to turn it off. By using the two external resistor dividers, it is easy to optimize the start and stop voltage of the system via EN pin:

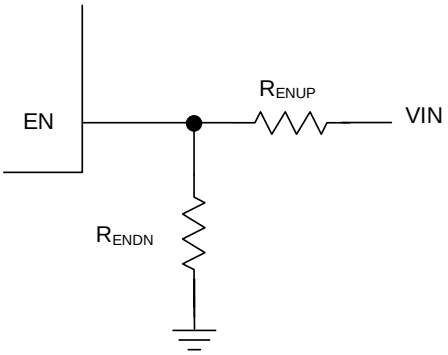


Figure 8-4 Enable network

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} - 4\mu A \times R_{ENUP} \quad (2)$$

Start voltage setting:

$$V_{STOP} = 0.95 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4\mu A \times R_{ENUP} \quad (3)$$

8.3.6 Internal Soft Start (SS)

The CJ92731 effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the power-supply's reference voltage and regulates the output accordingly. A capacitor on the SS pin to ground implements a soft start time. The CJ92731 has an internal pull-up current source of 1.7μA that charges the external soft start capacitor. The calculations for the soft start time (10% to 90%) are shown below equation. The voltage reference (VREF) is 0.8V and the soft start current (ISS) is 1.7μA. The soft start capacitor should remain lower than 100nF and greater than 4.7nF.

$$T_{SS}(ms) = \frac{0.8(V) + C_{SS}(nF)}{1.7(uA)} \quad (4)$$

8.3.7 Switching Frequency Set

The RT PIN can determine the switching frequency. CJ92731 has two options for switching frequency: 250kHz and 500kHz Selecting the switching frequency can be done by choosing the resistance value of the resistor connected between RT and GND. See below table:

Table 1 Switching frequency set resistor selection

RT resistor	Switching Frequency
Float	250 kHz
200 kΩ (±20%) to GND/ short to GND	500 kHz

8.3.8 High Duty Mode Operation

CJ92731 will automatically extend the on-time to support the application when VIN is close to VOUT. The on time extend circuit will be triggered when Toff min time is reached. The CJ92731 can support up to 97% maximum duty cycle at 250 kHz and 500 kHz.

8.3.9 Current Limit and Short Protection

The CJ92731 has a peak current limit and a special valley current. During HS-FET on, the inductor current is monitored. If the sensed inductor current reaches the peak current limit after blanking time, the HS-FET would be turn off. Due to the peak current limit's blanking time, the inductor current might runaway when output shorts to ground for a non-sync buck. The special valley current limit in CJ92731 can prevent this happening. When HS-FET is off and the inductor current is larger than the valley current limit, the HS-FET keeps off until the output current drops below the valley current limit threshold.

When the output is short to ground, CJ92731 will fold back the switching frequency automatically to prevent the current from running away. It will make the system more reliable.

8.3.10 Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 140°C), the chip is enabled again.

9 Application and Implementation

9.1 Typical Application Circuit

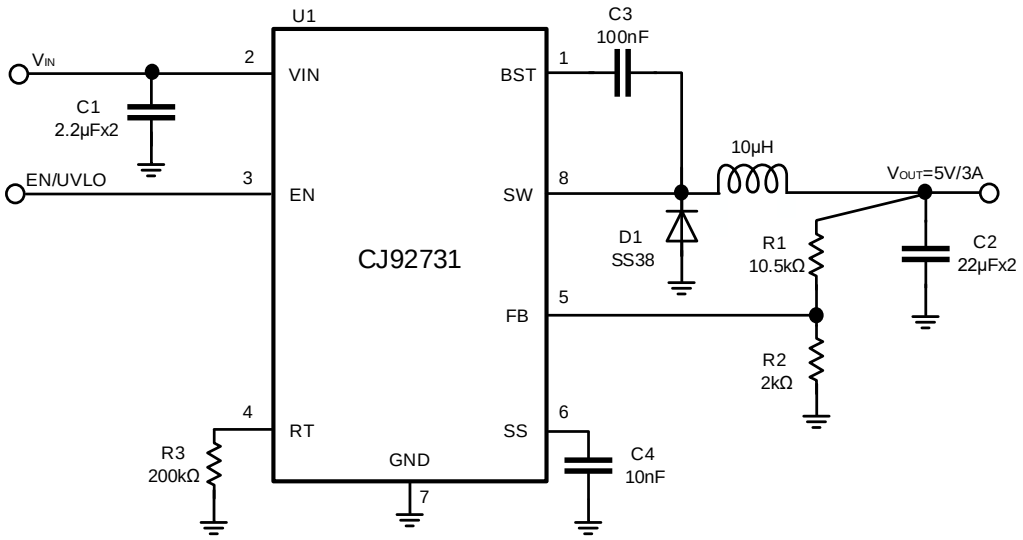


Figure 9-1 V_{IN}=48V, V_{OUT}=5V/3A, F_{SW}=500kHz

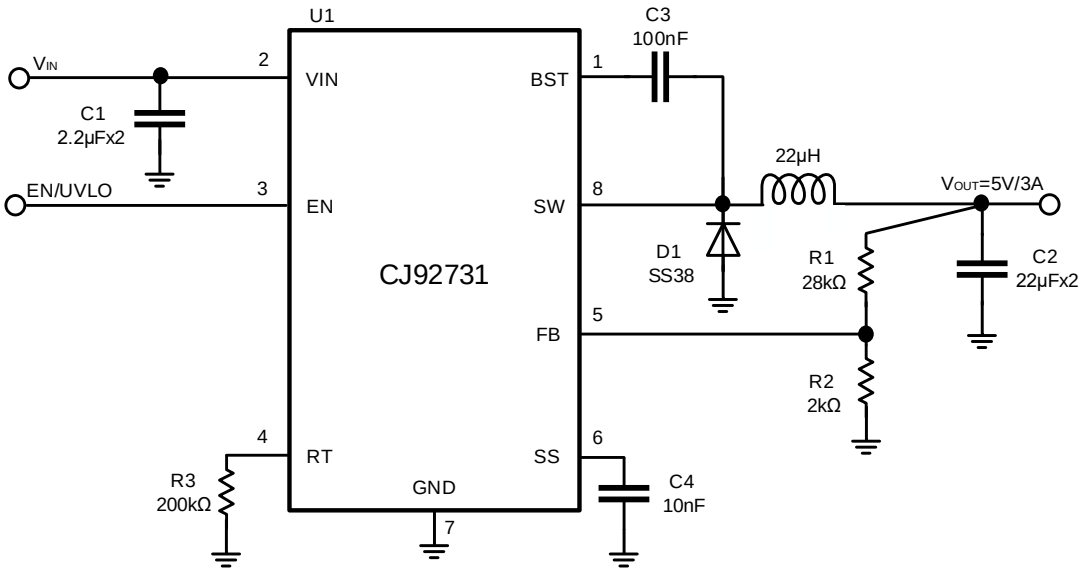


Figure 9-2 V_{IN}=48V, V_{OUT}=12V/3A, F_{SW}=500kHz

9.2 Application Selection

9.2.1 Setting the Output Voltage

The CJ92731 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.8V. The feedback network is shown below Figure.

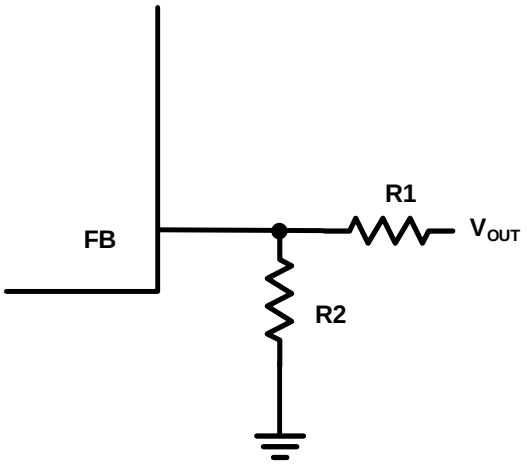


Figure 9-3 Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT} = V_{FB} \times \frac{(R_1 + R_2)}{R_2} \quad (4)$$

9.2.2 Setting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current.

For most designs, the inductance value can be derived from Equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection for Common Output Voltages (1)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{ff}(pF)	L (μH)	R_T (kΩ)	C_{OUT}(μF)
12	28	2	33 (optional)	22	200	44
5	10.5	2	100 (optional)	10	200	44

(1) For a detailed design circuit, please refer to the Typical Application Circuit

9.2.3 Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

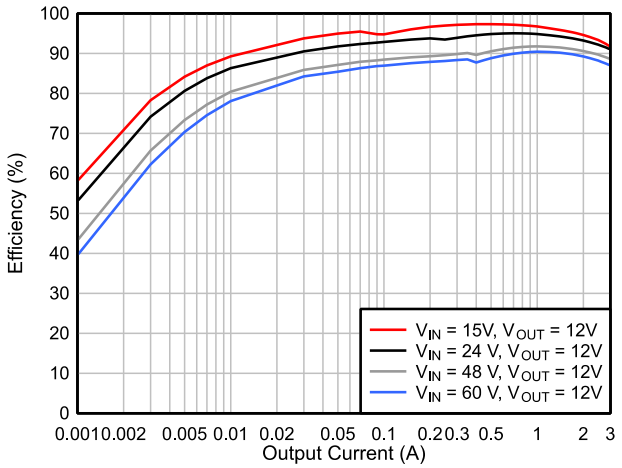
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

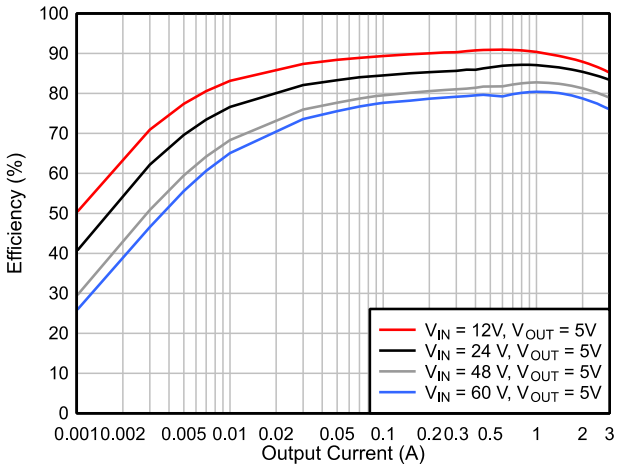
The characteristics of the output capacitor also affect the stability of the regulation system. The CJ92731 can be optimized for a wide range of capacitance and ESR values.

9.3 Typical Performance Characteristics

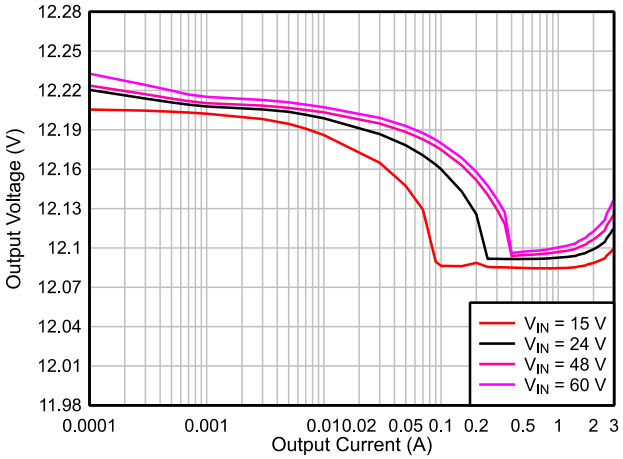
V_{IN} = 48V, V_{OUT} = 12V, F_{SW} = 500kHz, C_{IN} = 2x2.2μF, C_{OUT} = 2x22μF, L1 = 22μH, and T_A = +25°C, unless otherwise noted.



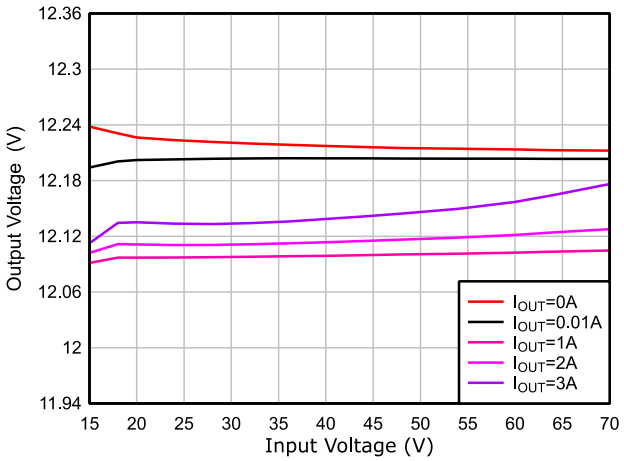
Efficiency vs. Load Current
(V_{OUT}=12V, L1=22μH, DCR=66mΩ)



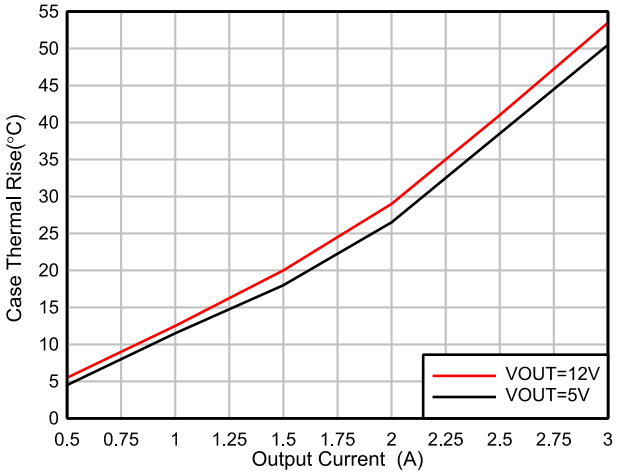
Efficiency vs. Load Current
(V_{OUT}=5V, L1=10μH, DCR=30mΩ)



Load Regulation
(V_{OUT}=12V, DCR=66mΩ)

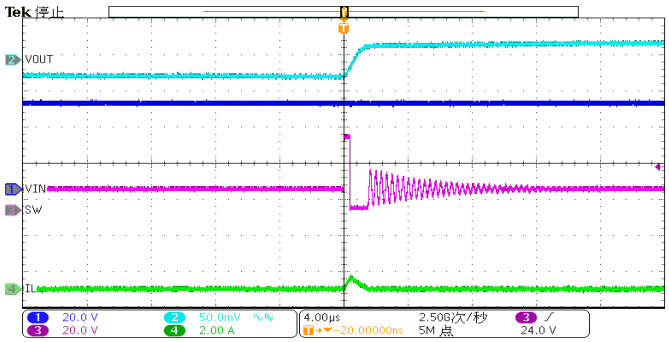


Line Regulation
(V_{OUT}=12V, DCR=66mΩ)

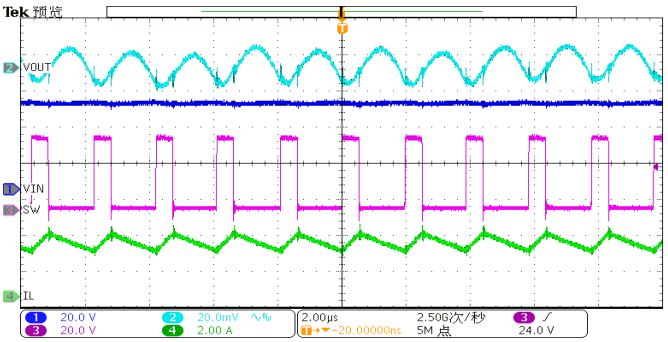


Thermal Rise (No air flow)

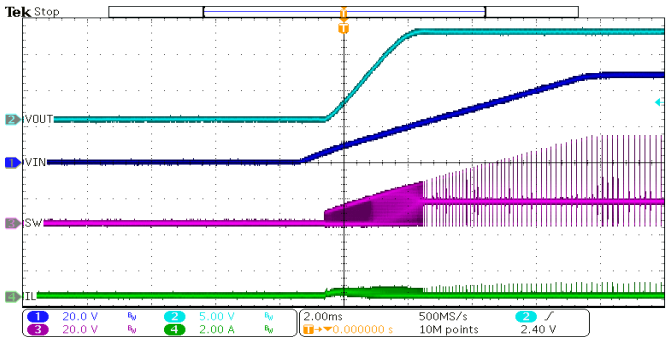
V_{IN} = 48V, V_{OUT} = 12V, F_{SW} = 500kHz, C_{IN} = 2x2.2μF, C_{OUT} = 22μFx2, L1 = 22μH, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



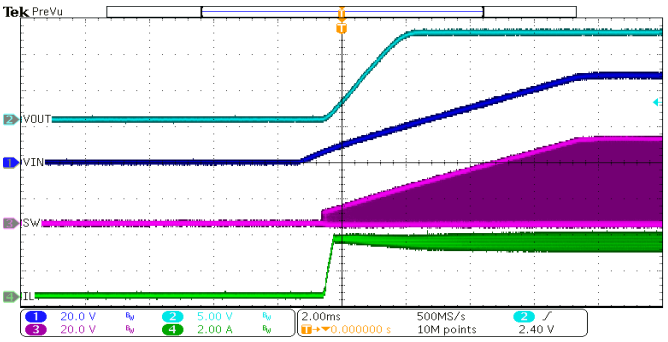
Output Voltage Ripple
(I_{OUT} =0A, PFM MODE)



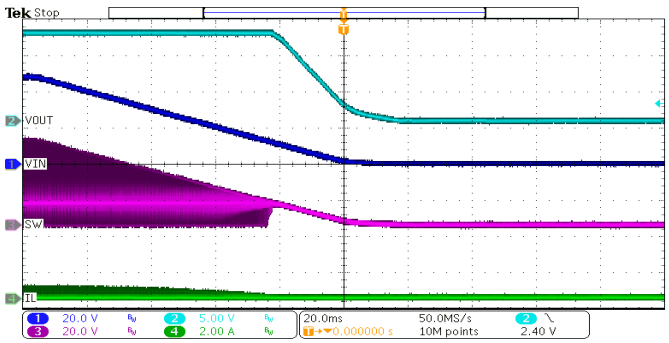
Output Voltage Ripple
(I_{OUT} =3A)



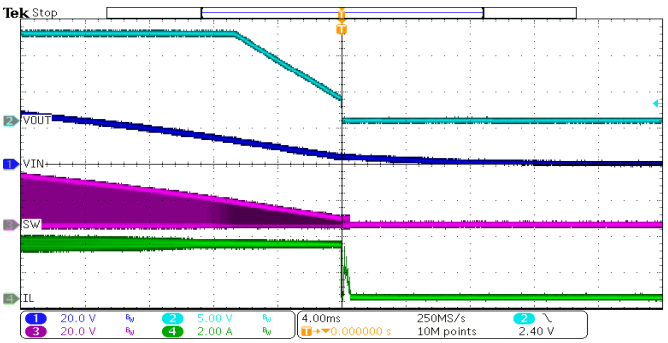
Start-Up through V_{IN}
(I_{OUT} =0A, PFM MODE)



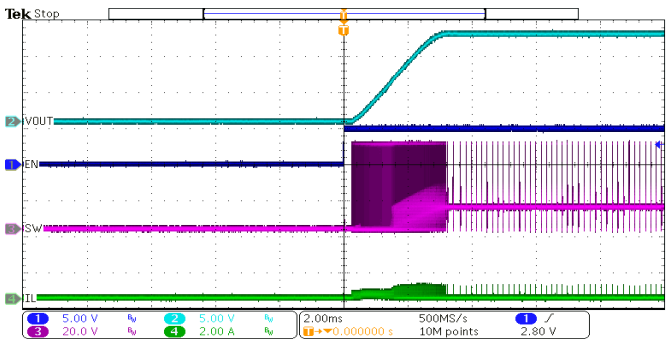
Start-Up through V_{IN}
(I_{OUT} =3A)



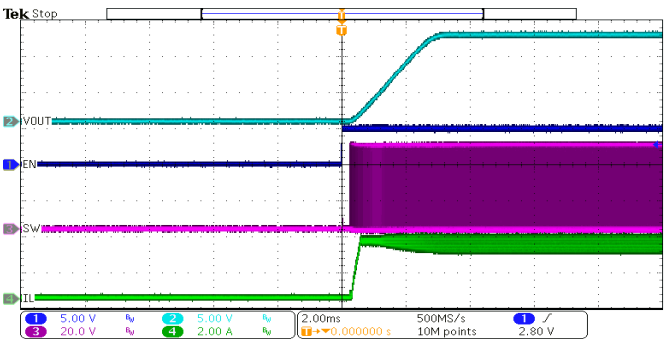
Shut-Down through V_{IN}
(I_{OUT} =0A, PFM MODE)



Shut-Down through V_{IN}
(I_{OUT} =3A)

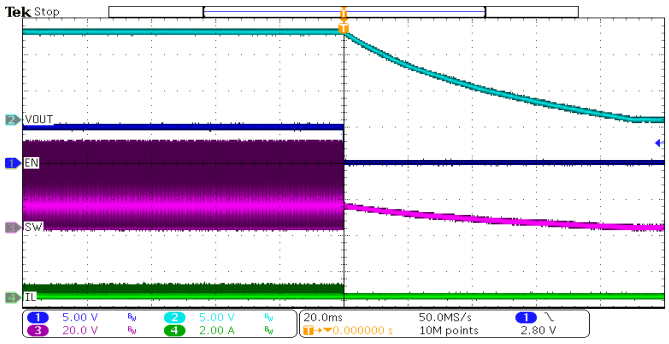


Start-Up through EN
(I_{OUT} =0A, PFM MODE)

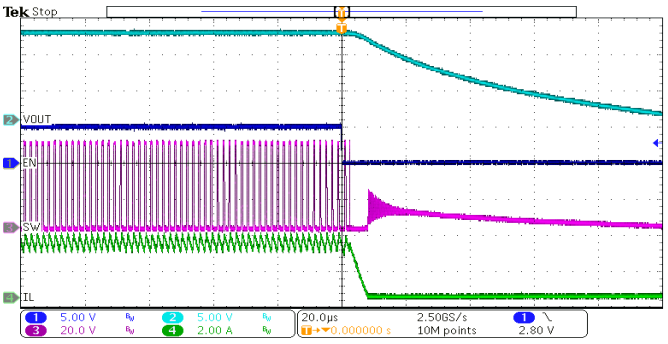


Start-Up through EN
(I_{OUT} =3A)

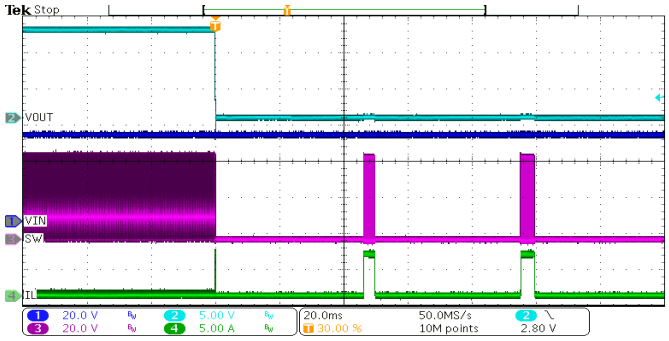
V_{IN} = 48V, V_{OUT} = 12V, F_{SW} = 500kHz, C_{IN} = 2x2.2μF, C_{OUT} = 22μFx2, L1 = 22μH, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



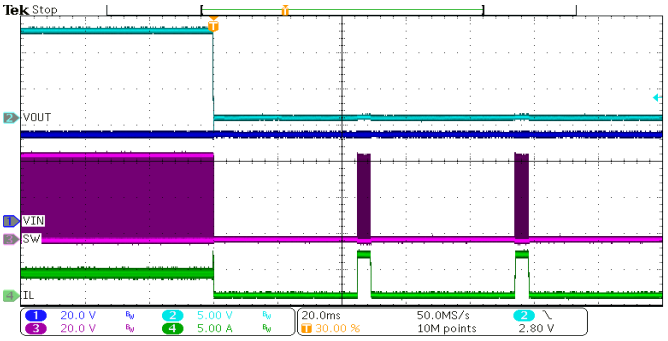
Shut-Down through EN
(I_{OUT} =0A, PFM MODE)



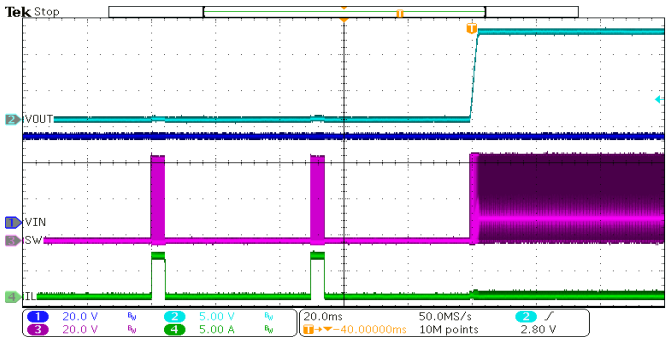
Shut-Down through EN
(I_{OUT} =3A)



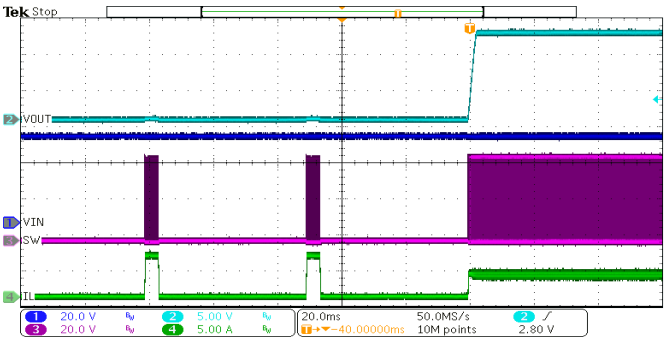
Short-Circuit Entry
(I_{OUT} =0A, PFM MODE)



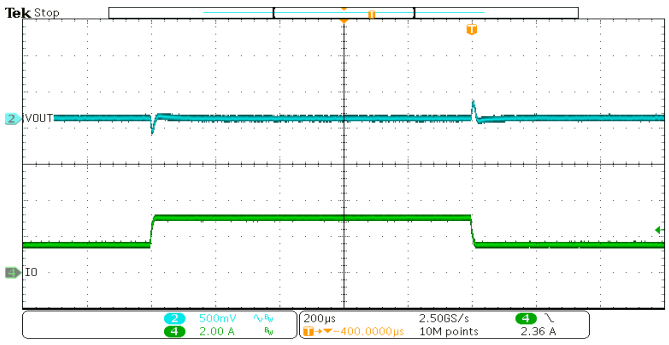
Short-Circuit Entry
(I_{OUT} =3A)



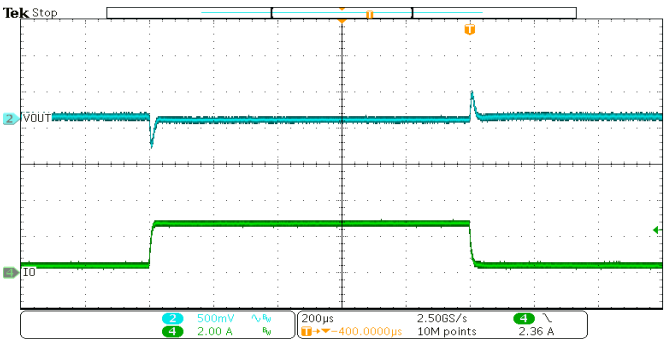
Short-Circuit Recovery
(I_{OUT} =0A, PFM MODE)



Short-Circuit Recovery
(I_{OUT} =3A)



Load Transient
(I_{OUT} = 1.5A to 3A, slew rate = 3A/μs)



Load Transient
(I_{OUT} = 0.3A to 2.7A, slew rate = 3A/μs)

10 Layout

10.1 Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

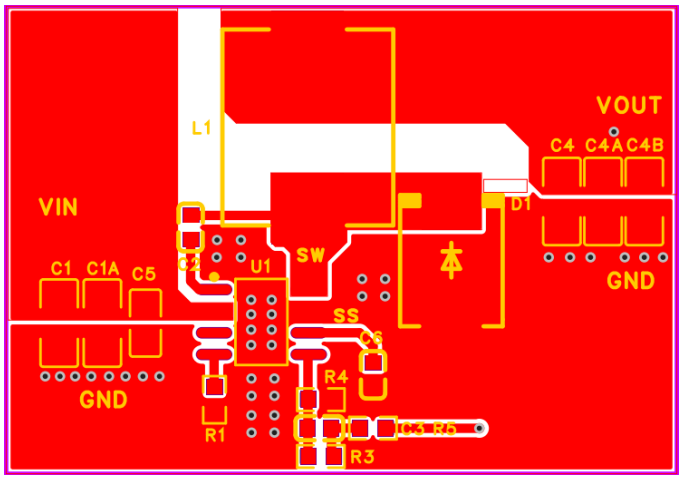


Figure 10-1 Recommend PCB Layout-Top Layer

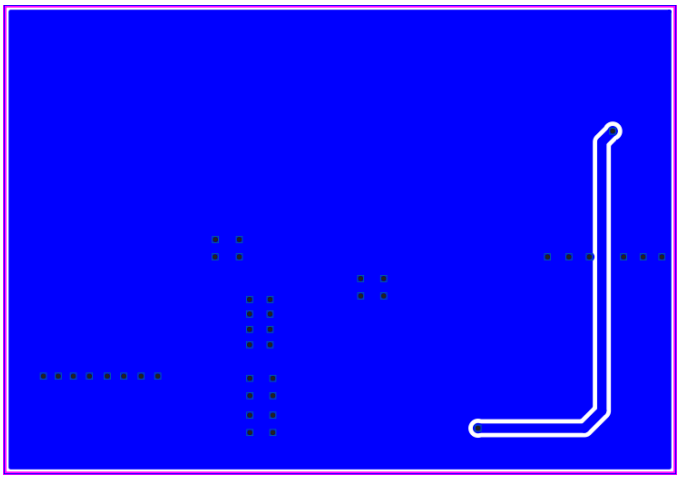
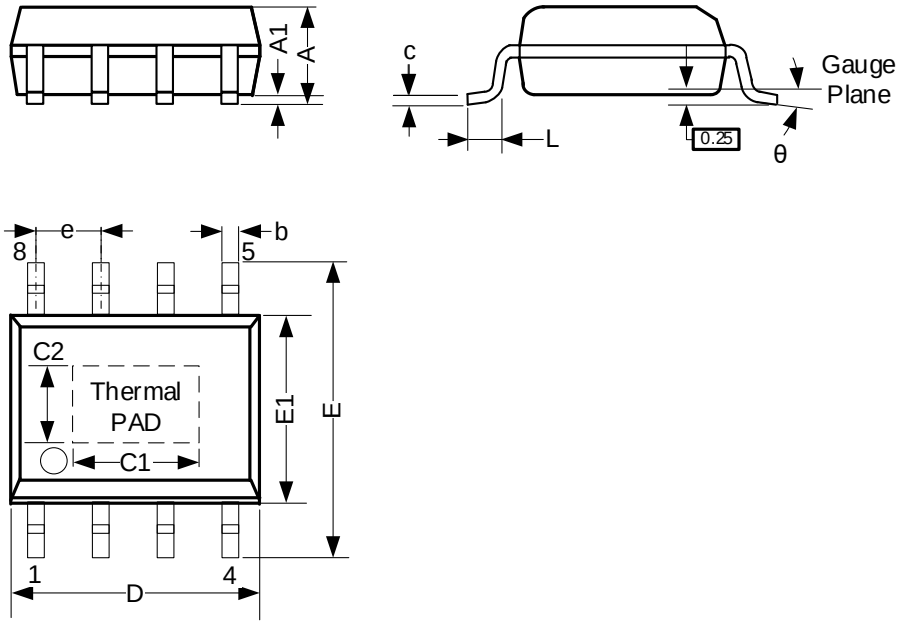


Figure 10-2 Recommend PCB Layout- Bottom Layer

11 Mechanical Information

11.1 ESOP8 Mechanical Information

11.1.1 ESOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.30	-	1.70
A1	0.00	-	0.15
b	0.33	-	0.51
c	0.19	-	0.25
C1	3.15	-	3.45
C2	2.26	-	2.56
D	4.80	-	5.00
E	5.80	-	6.20
E1	3.80	-	4.00
e	1.27 BSC		
L	0.41	-	1.27
Θ	0°	-	8°
Unit: mm			

12 Notes and Revision History

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

12.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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