



4.5V~100V, 550kHz, Asynchronous, DC-DC Step-Down Converter

CJ92900

DC-DC

1 Introduction

The CJ92900 is an easy-to-use, asynchronous buck converter. 4.5V to 100V input voltage range accommodates a variety of step-down applications.

The CJ92900 is integrated with 1.1Ω low R_{DS_ON} high-side power MOSFET. It can provide up to 500mA continuous output current with advanced COT control for fast response and ease loop compensation. The switching frequency is typically 550kHz, which will help to minimize the solution size and reduce BOM cost.

The CJ92900 has built-in full protection features, cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation.

The CJ92900 is available in a cost-effective SOT-23-6L package.

2 Available Packages

PART NUMBER	PACKAGE
CJ92900	SOT-23-6L

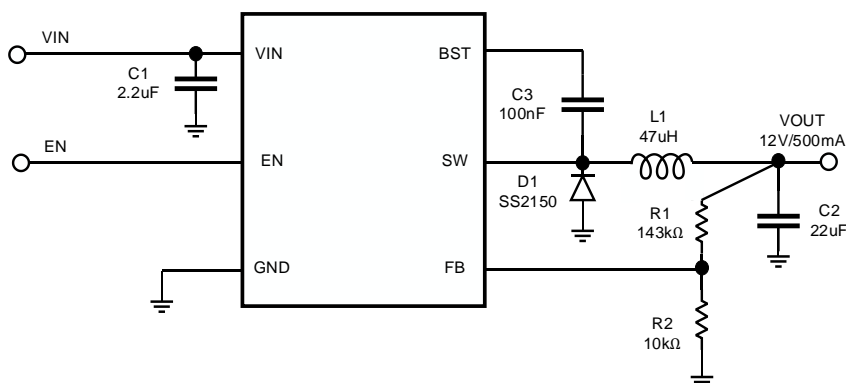
3 Features

- 4.5V to 100V Wide Input Range
- Integrated 1.1Ω low resistance high side power MOS
- Constant On Time Control for Fast Loop Response
- 180μA low Quiescent Current
- 550kHz Switching Frequency
- Special Valley Current Limit for asynchronous Buck Short Protection
- 3μA Low Current at Off-state
- Float EN pin for automatically start-up
- Low Drop Out Mode Supports 97% Duty Cycle
- 0.788V Reference Voltage
- Available in SOT-23-6L package
- Short Circuit Protection with Hiccup Mode
- Over Temperature Protection

4 Applications

- Battery powered tools
- E-bike powers, E-motors
- Industry applications

Typical Application



5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ92900-M6N	SOT-23-6L	-40 ~ 125°C	RoHS & Green	Level 1	Tape and Reel 3000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products.

Customized: Products manufactured to meet the specific needs of customers.

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available.

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers.

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

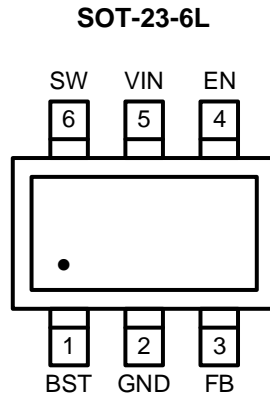


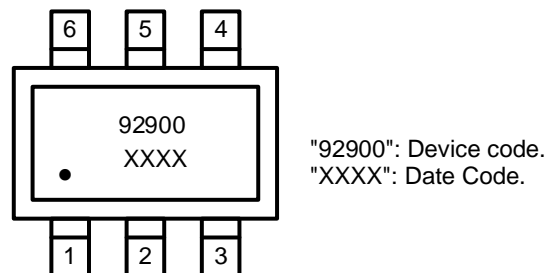
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I / O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	BST	P	Bootstrap capacitor connection pin for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
2	GND	G	Ground pin of IC. Connect to the ground of the system.
3	FB	I	Feedback. Connect a resistor divider to set the output voltage.
4	EN	I	Enable. Float this pin for automatically start-up, pull down this pin to shut down the IC.
5	VIN	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
6	SW	P	Switching node of power stage. Connect to power inductor.

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



7 Specifications

7.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified) ⁽¹⁾

SYMBOL	CHARACTERISTIC	VALUE	UNIT
V _{IN}	VIN to GND	-0.3 ~ 105	V
V _{SW}	SW to GND	-0.3 ~ 105	V
V _{BST} - V _{SW}	BST to SW	6	V
I _{EN}	Max Input current to EN pin	100	uA
All other pins		-0.3 ~ 6	V
T _J	Junction temperature	-40 ~ 150	°C
T _{stg}	Storage temperature	-55 ~ 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNIT
V _{IN}	VIN to GND	4.5		100	V
V _{OUT}	V _{OUT} to GND	0.8		V _{IN} *D _{MAX} ⁽¹⁾ Or V _{OUT} <24	V
I _{OUT}	Continuous Output Current	0		0.5	A

(1) D_{MAX} = T_{ON_MAX} / (T_{ON_MAX} + T_{OFF_MIN}). Typical value is 97%.

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
V _{ESD-HBM}	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	±2000	V
V _{ESD-CDM}		Charged-device model (CDM) ⁽²⁾	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

SYMBOL	THERMAL METRIC	SOT-23-6L	UNIT
R _{θJA} ⁽¹⁾	Junction-to-ambient thermal resistance	173	°C/W
R _{θJC(top)} ⁽¹⁾	Junction to case (top) thermal resistance	116	°C/W
R _{θJB} ⁽¹⁾	Junction-to-board thermal resistance	31	°C/W

(1) The value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were measured on JESD 51-7, 4-layer JEDEC PCB board.

7.5 Electrical Characteristics
V_{IN}=60V and T_A=25°C, unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{INUV_R}	VIN UVLO rising voltage			4.3		V
V _{INUV_F}	VIN UVLO falling voltage			4		V
V _{INUV_HYS}	Hysteresis voltage of VIN UVLO			0.3		V
I _S	Shut down current from VIN	V _{EN} =0V		3		μA
I _Q	Quiescent current from VIN	V _{FB} =0.85V		180		μA
V _{EN_R}	Enable rising voltage			1.2		V
V _{EN_F}	Enable falling voltage			1		V
I _{EN_PULL_UP}	Enable pull-up current	V _{EN} =Low		1		μA
		V _{EN} =High		4		μA
V _{FB}	Feedback voltage		0.776	0.788	0.8	V
V _{FB_UV}	Feedback UVLO threshold			0.1		V
R _{HS_ON}	High Side power MOS ON resistance	V _{BST} -V _{SW} =5V		1.1		Ω
I _{LIMIT_HS}	High side current limit threshold			1.45		A
T _{SS}	Soft-start time	V _{FB} from 10% to 90%		1.5		ms
F _{SW}	Switching frequency		400	550	640	kHz
T _{ON_MIN} ⁽¹⁾	Min on time			150		ns
T _{ON_MAX}	Max on time			10		μs
T _{OFF_MIN} ⁽¹⁾	Min off time			350		ns
T _{VALLEY_MAX} ⁽¹⁾	Max valley off time			100		μs
T _{OTP_R} ⁽¹⁾	Thermal shutdown entry threshold			160		°C
T _{OTP_F} ⁽¹⁾	Thermal shutdown recovery threshold			140		°C

(1) Guaranteed by design and engineering sample characterization

8 Detailed Description

8.1 Overview

The CJ92900 is an easy-to-use, asynchronous buck converter. 4.5V to 100V input voltage range accommodates a variety of step-down applications. It is integrated with 1.1Ω low R_{DS_ON} high-side power MOSFET and can provide up to 500mA continuous output current with advanced COT control for fast response and ease loop compensation. Typical 550kHz switching frequency will help to minimize the solution size and reduce BOM cost

The CJ92900 has built-in full protection features, cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation.

8.2 Functional Block Diagram

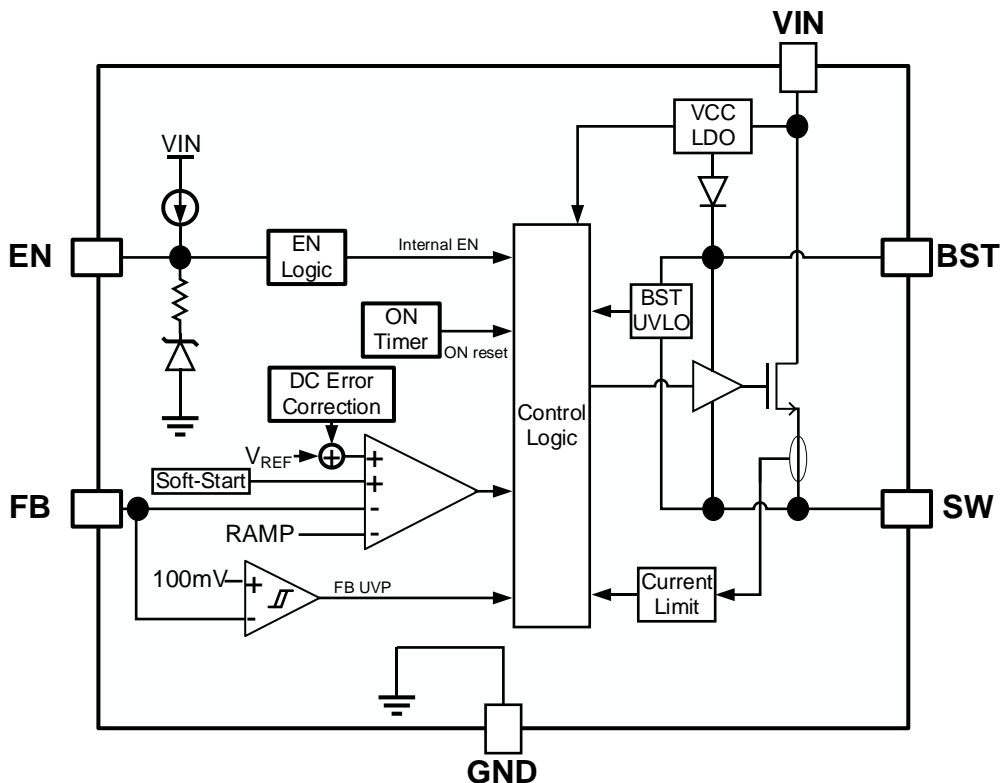


Figure 8-1 Function block diagram

8.3 Feature Description

8.3.1 Pulse-Width Modulation (PWM) Operation

The CJ92900 is a fully integrated, asynchronous, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on-period is determined by both the output voltage and input voltage to make the switching frequency relatively constant over the input voltage range.

After the On-time elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF} . By repeating operations this way, the converter regulates the output voltage.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

8.3.2 Heavy-Load Operation

When the output current is high and the inductor current is always above zero amps (see Figure 8-2), the converter works in Continuous conduction mode (CCM). The HS-FET is turned on for a fixed interval determined by the one-shot on-timer once the V_{FB} is below V_{REF} . Then the HS-FET is turned off and the external free-wheeling diode will handle the current.

In CCM operation mode, the switching frequency is relatively constant, which is called pulse-width modulation (PWM) mode.

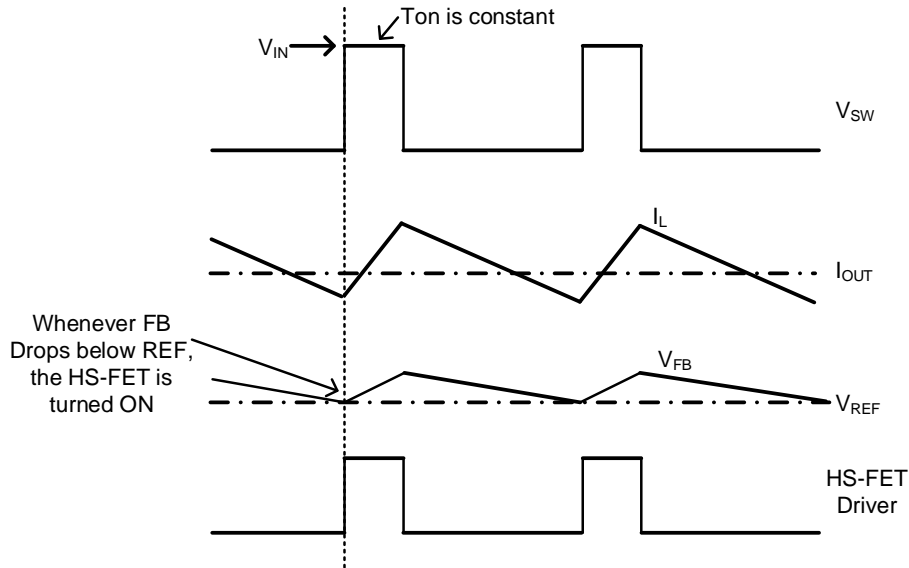


Figure 8-2 Heavy-Load Operation

8.3.3 Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 8-3. When V_{FB} is below V_{REF} , the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. Then the HS-FET is turned off and the free-wheeling diode is turned on until the inductor current drops to zero. In DCM operation, V_{FB} cannot reach V_{REF} when the inductor current is approaching zero. When the free-wheeling diode current arrives at zero, it will shut down the negative current and SW goes into tri-state. The output capacitors are only discharged to GND through the feedback resistor slowly. As a result, the efficiency in light-load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

Regarding light-load or no-load condition, the output drops very slowly, and the CJ92900 reduces the switching frequency naturally. High efficiency is achieved at light load.

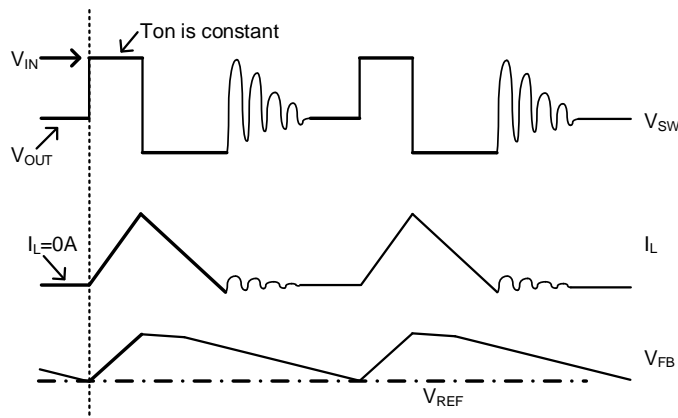


Figure 8-3 Light-Load Operation

As the output current increases from the light-load condition, the HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT_Critical} = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains relatively constant over the output current range.

8.3.4 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The CJ92900’s UVLO comparator will monitor the input voltage with 4.3V rising threshold and 4V falling threshold.

8.3.5 Enable (EN) Control

The CJ92900 has a dedicated enable control pin with positive logic. To turn on the regulator, drive the EN pin voltage higher than 1.2V(typical). To turn it off, drive the EN pin voltage lower than 1V (typical).

The EN pin includes an internal pull-up current source, allowing the CJ92900 to automatically start-up when the EN pin is floating. More than 4µA pulldown current is required to shut down the regulator via EN pin. Once the EN pin is pulled low, its internal pull-up current will decrease to 1µA to reduce the shutdown current.

By using the two external resistor dividers, it is easy to optimize the system’s start and stop voltage via EN pin:

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} - 1\mu A \times R_{ENUP} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 1 \times \frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} - 4\mu A \times R_{ENUP} \quad (3)$$

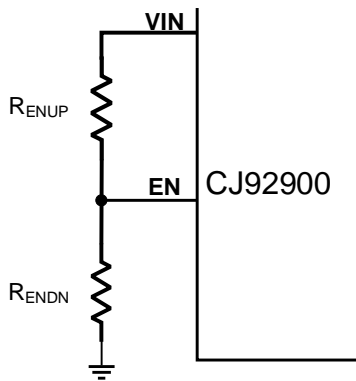


Figure 8-4 EN divider for adjustable UVLO

8.3.6 Internal Soft Start (SS)

Soft start (SS) prevents the output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V. When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF}, the error amplifier uses V_{SS} as the reference. Once V_{SS} exceeds V_{REF}, the error amplifier switches to using V_{REF} as the reference. The SS time is set to 1.5ms internally.

8.3.7 High Duty Mode Operation

The CJ92900 will automatically extend the on-time to support the application when V_{IN} is close to V_{OUT}. The on time extend circuit will be triggered when T_{OFF_MIN} time is reached. The CJ92900 can support up to 97% maximum duty cycle.

8.3.8 Current Limit and Short Protection

The CJ92900 has a peak current limit and a special valley current-limit circuit. During HS-FET on phase, the inductor current is monitored. If the sensed inductor current reaches the peak current limit after the blanking time, the HS-FET will be turned off. Due to the peak current limit's blanking time, the inductor current might run away when output shorts to ground for an asynchronous buck. The special valley current limit in CJ92900 can prevent this failure. When HS-FET is off and the inductor current is larger than the valley current limit, the HS-FET remains off until the output current drops below the valley current limit threshold. As a result, CJ92900 will automatically fold back the switching frequency to prevent the current from running away, making the system more reliable.

8.3.9 Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. The chip recovers when the temperature falls below its lower threshold (typically 140°C).

9 Application and Implementation

9.1 Typical Application Circuit

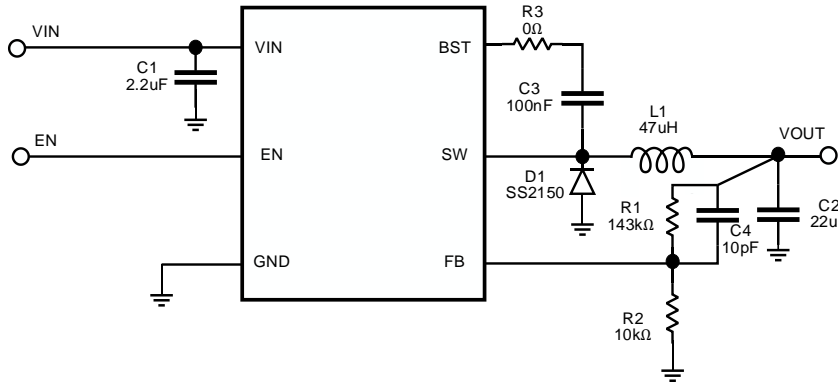


Figure 9-1 VIN=48V, VOUT=12V/500mA

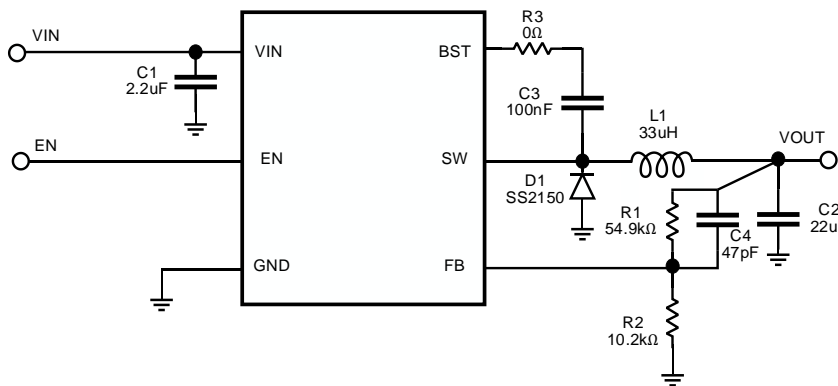


Figure 9-2 VIN=48V, VOUT=5V/500mA

9.2 Component Selection

9.2.1 Setting the Output Voltage

The CJ92900 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.788V. The feedback network is shown below Figure.

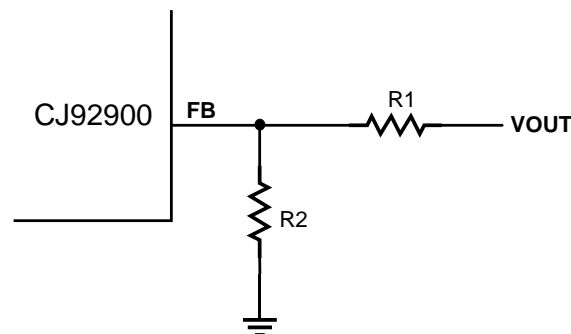


Figure 9-3 Feedback Network

Choose R1 and R2 using the Equation:

$$V_{OUT} = V_{FB} \times \frac{(R1+R2)}{R2} \quad (4)$$

9.2.2 Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current.

For most designs, the inductance value can be derived from Equation:

$$L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times f_{SW} \times V_{IN}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages ⁽¹⁾

VOUT (V)	R1 (kΩ)	R2 (kΩ)	Cff(pF)	L (μH)	COUT(μF)
12	143	10	10	47	22
5	54.9	10.2	47	33	22

(1) For a detailed design circuit, please refer to the Typical Application Circuit

9.2.3 Selecting the Output Capacitor

The output capacitor maintains the DC output voltage ripple. Ceramic, tantalum, or low-ESR electrolytic capacitors can be used. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

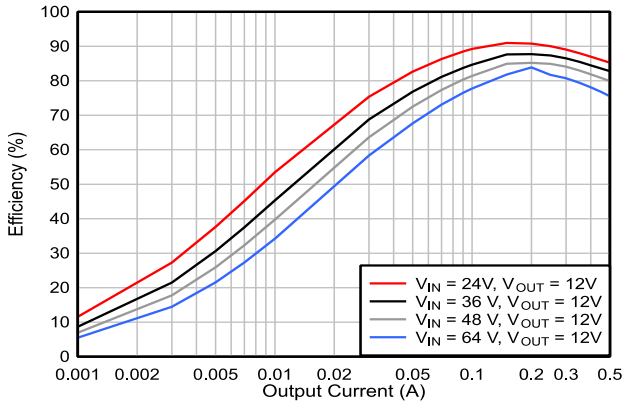
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

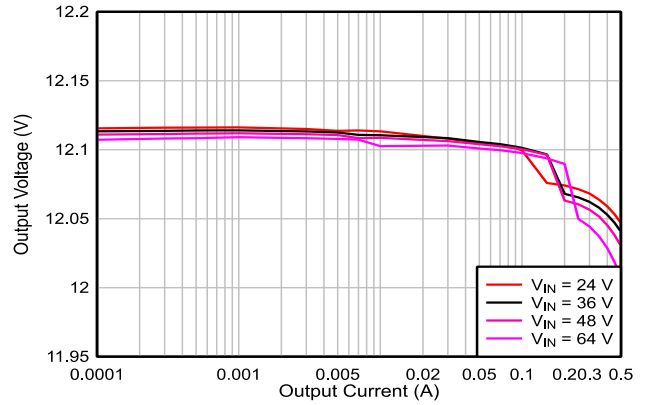
The characteristics of the output capacitor also affect the stability of the regulation system. The CJ92900 can be optimized for a wide range of capacitance and ESR values.

9.3 Application Curve

$V_{IN} = 48V$, $V_{OUT} = 12V$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 22\mu F$, $L1 = 47\mu H$, and $T_A = +25^\circ C$, unless otherwise noted.

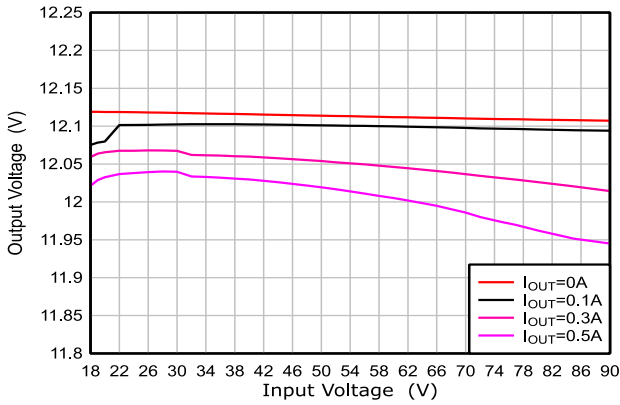


Efficiency vs. Output Current (DCR=135mΩ)

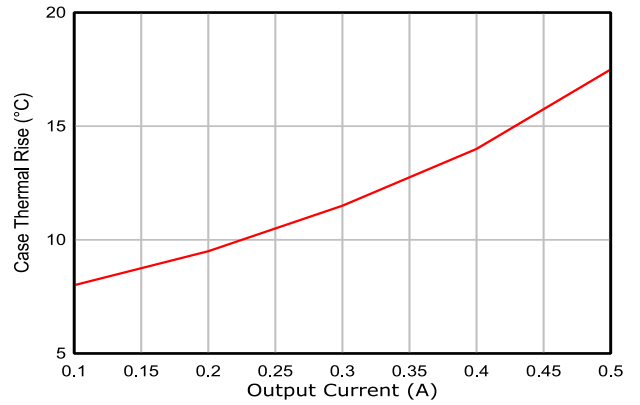


Load Regulation

DATA.xlsx7

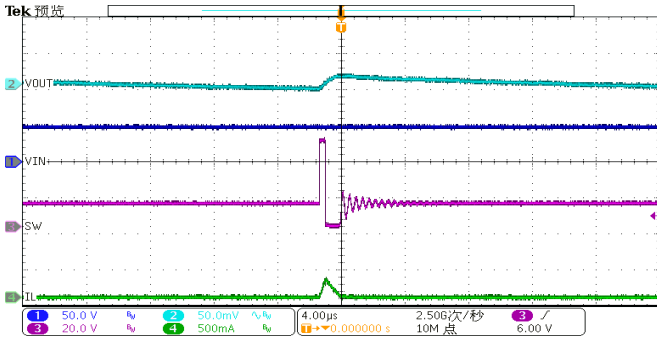


Line Regulation

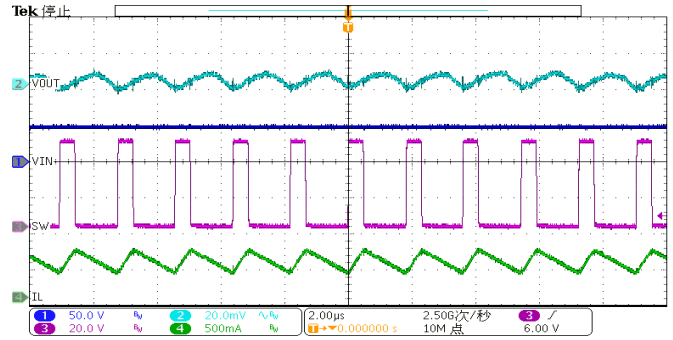


Thermal Rise (no air flow)

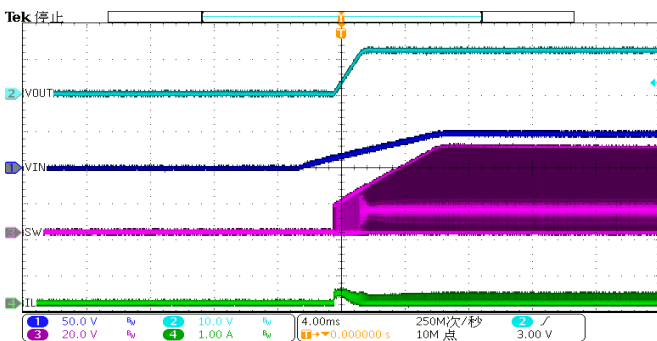
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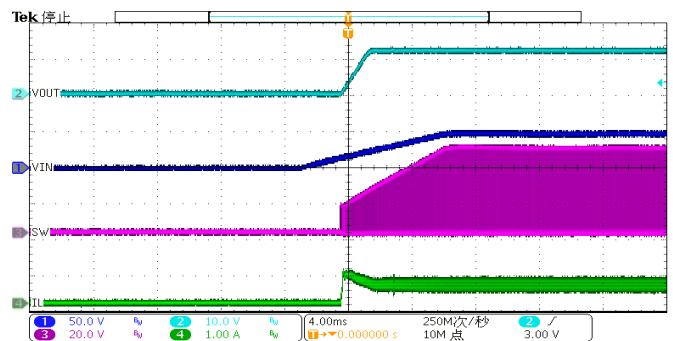
Output Voltage Ripple ($I_{OUT}=0A$)



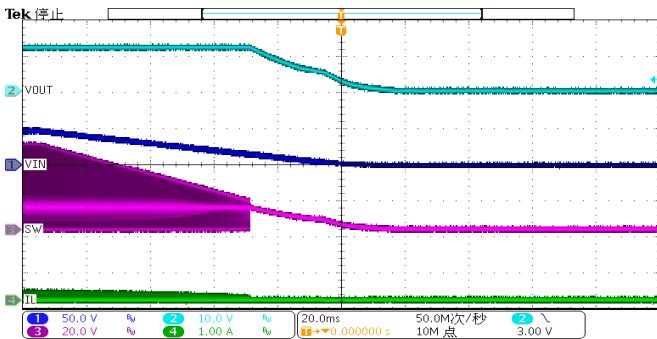
Output Voltage Ripple ($I_{OUT}=500mA$)



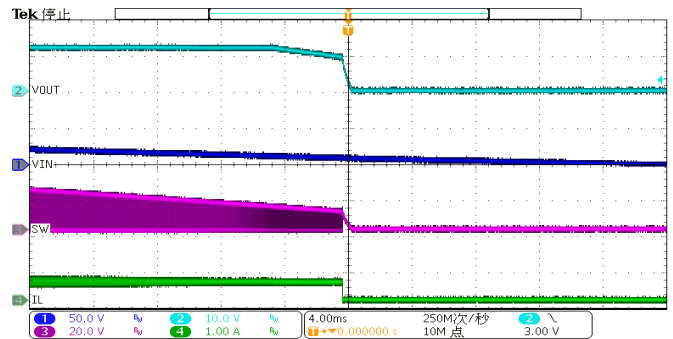
Start-Up through V_{IN} ($I_{OUT}=0A$)



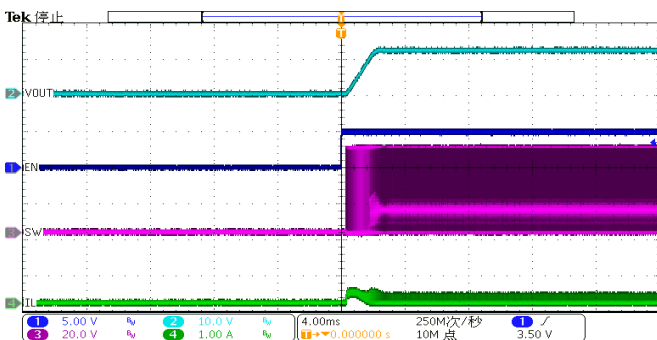
Start-Up through V_{IN} ($I_{OUT}=500mA$)



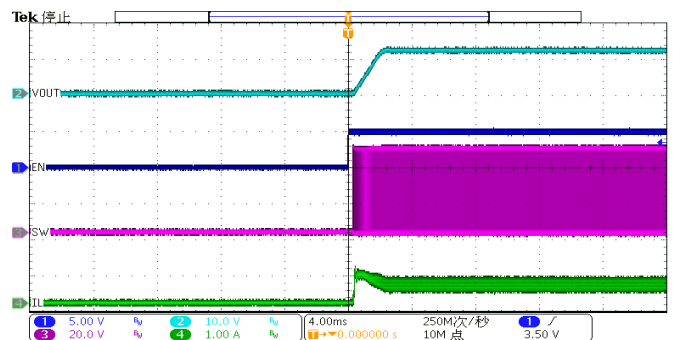
Start-Down through V_{IN} ($I_{OUT}=0A$)



Start-Down through V_{IN} ($I_{OUT}=500mA$)

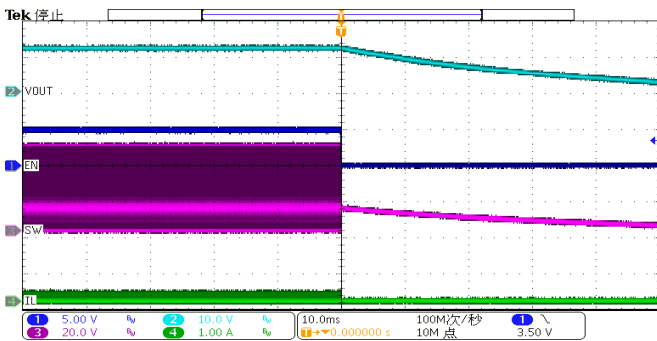


Start-Up through EN ($I_{OUT}=0A$)

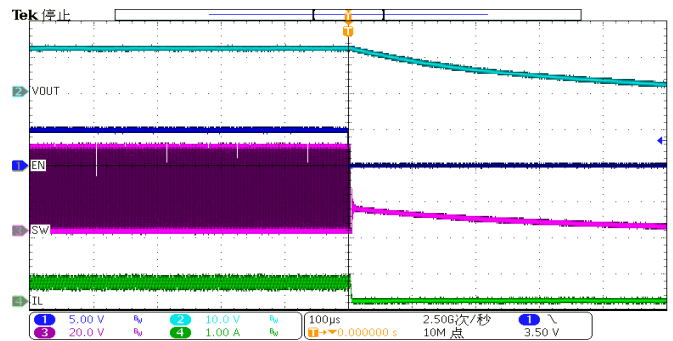


Start-Up through EN ($I_{OUT}=500mA$)

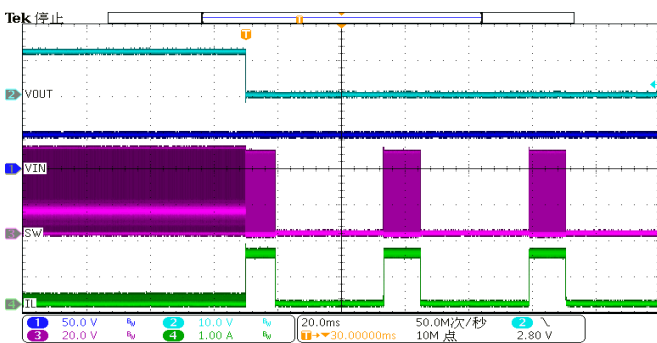
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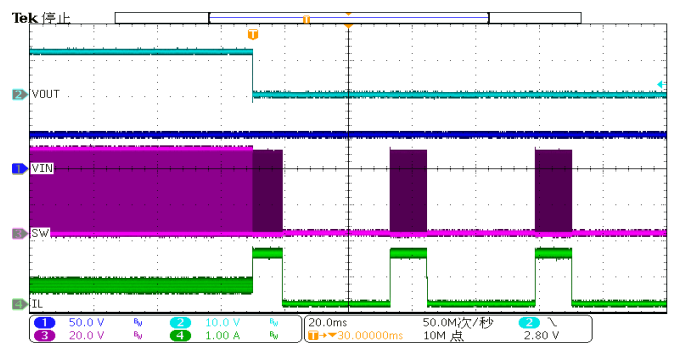
Start-Down through EN ($I_{OUT}=0A$)



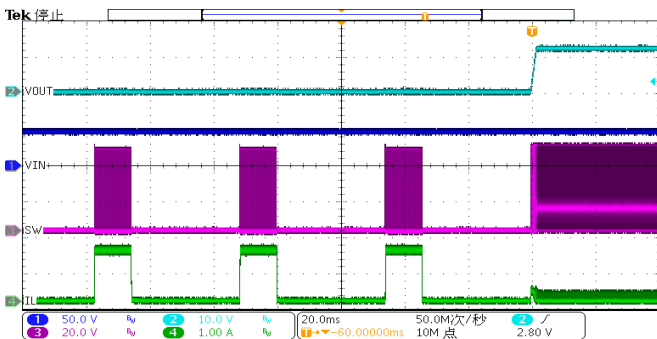
Start-Down through EN ($I_{OUT}=500mA$)



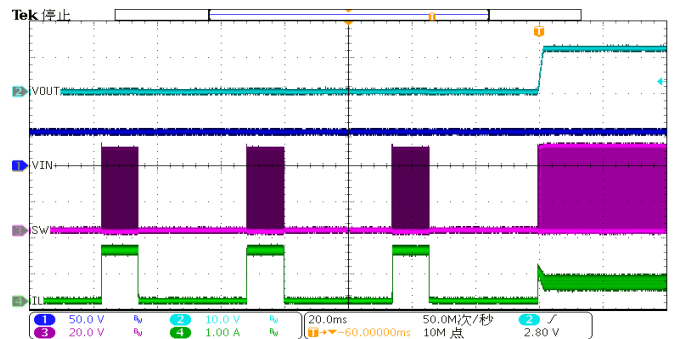
Short-Circuit Entry ($I_{OUT}=0A$)



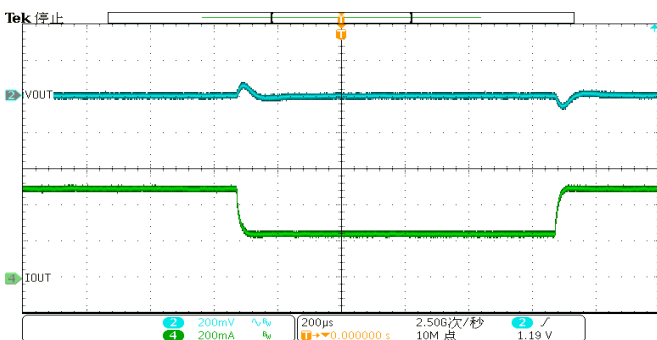
Short-Circuit Entry ($I_{OUT}=500mA$)



Short-Circuit Recovery ($I_{OUT}=0A$)



Short-Circuit Recovery ($I_{OUT}=500mA$)



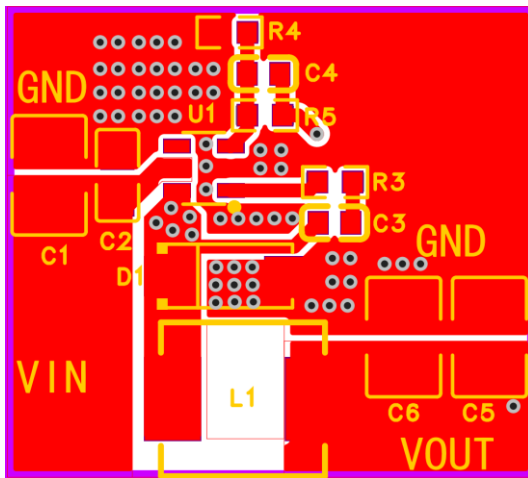
Load Transient
($I_{OUT} = 0.25A$ to $0.5A$, $2.5A/\mu s$ slew rate)

10 Layout

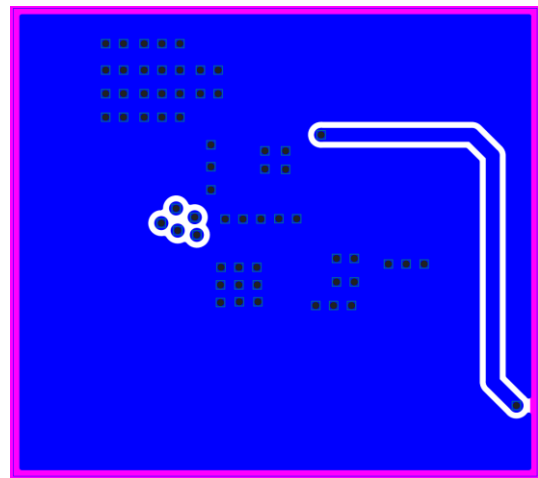
10.1 Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to the figure below and follow the guidelines below.

- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.



Top Layer



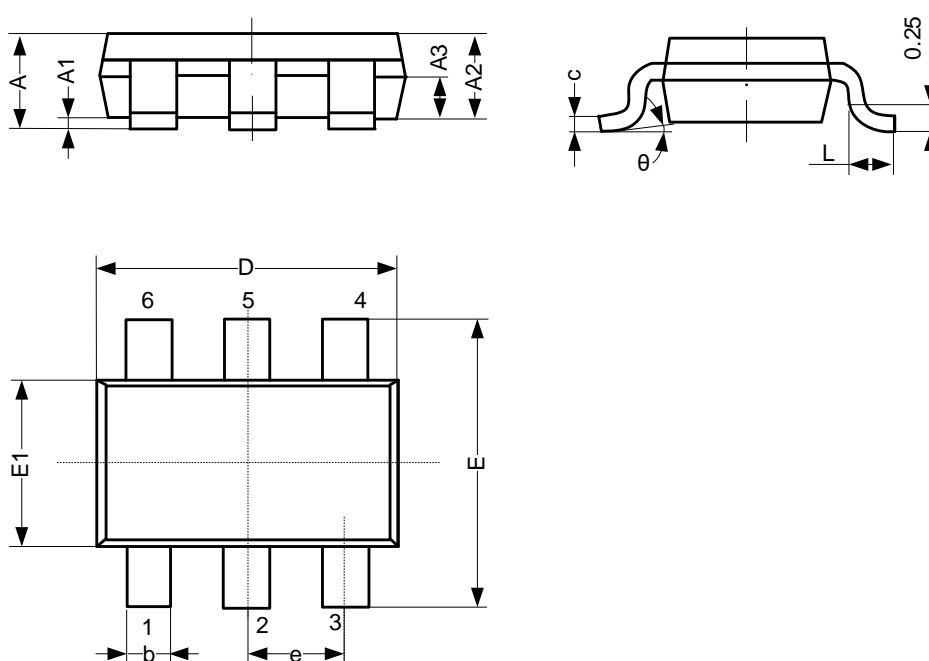
Bottom Layer

Figure 10-1 Recommend PCB Layout

11 Mechanical Information

11.1 SOT-23-6L Mechanical Information

SOT-23-6L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	–	–	1.45
A1	0.00	–	0.15
A2	0.90	–	1.30
b	0.30	–	0.50
c	0.09	–	0.20
D	2.80	–	3.00
E	2.60	–	3.00
E1	1.50	–	1.70
e	0.95 BSC		
L	0.30	–	0.60
θ	0°	–	8°

12 Notes

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

12.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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