4.5V~100V, 460kHz, Asynchronous, Step-Down Converter

CJ92911 DC-DC

1 Introduction

The CJ92911 is an easy-to-use, non-sync buck converter, which is integrated with 900mΩ low R_{DS_ON} high-side power MOSFET. The CJ92911 can provide up to 1A continues output current with advanced COT control for fast response and ease loop compensation.

The switching frequency of CJ92911 is typically 460kHz, which will help to minimize the solution size and reduce BOM cost. The CJ92911 has 4.5V to 100V input voltage range, which accommodates a variety of step-down applications.

The CJ92911 has built-in full protection features, cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation.

The CJ92911 is available in a cost-effective SOT-23-6L package.

2 Available Packages

PART NUMBER	PACKAGE
CJ92911	SOT-23-6L

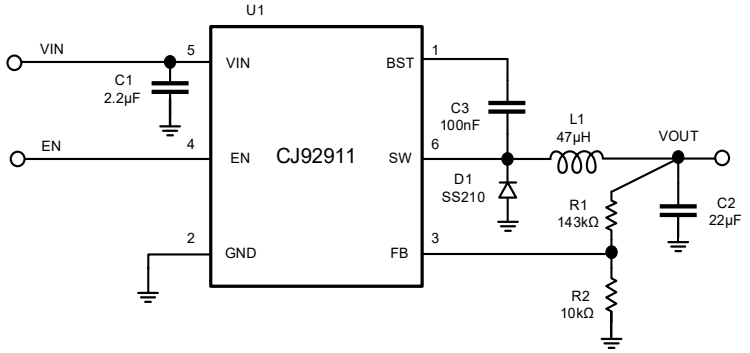
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- 4.5V to 100V Wide Input Range
- Integrated 900mΩ low resistance high side power MOS
- Constant On Time Control for Fast Loop Response
- 180μA low Quiescent Current
- 460kHz Switching Frequency
- Special Valley Current Limit for non- sync Buck Short Protection
- 3μA Low Current at Off-state
- Float EN pin for automatically start-up
- Low Drop Out Mode Support 97% Duty Cycle
- Reference Voltage 0.78V
- Available in SOT-23-6L package
- Short Circuit Protection with Hiccup Mode
- Over Temperature Protection

4 Applications

- Battery powered tools
- E-bike powers, E-motors
- Industry applications



Typical Application Circuit

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ92911-M6N	SOT-23-6L	-40~125°C	RoHS & Green	Level 1 Unlimited	Tape and Reel 3000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

SOT-23-6L

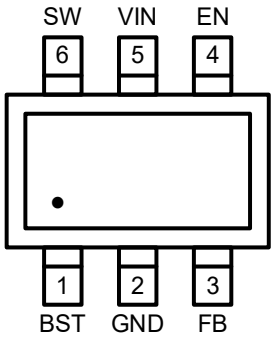


Figure 6-1 Pin Configuration

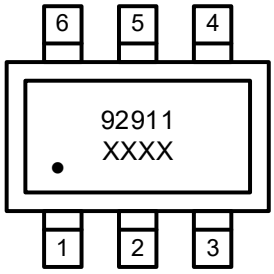
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	BST	P	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
2	GND	G	Ground pin of IC. Connect to the ground of the system.
3	FB	I	Feedback. Connect a resistor divider to set the output voltage.
4	EN	I	Enable. Float this pin for automatically start-up, pull down this pin to shut down the IC.
5	VIN	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors C_{IN}. Input bypass capacitors must be directly connected to this pin and GND.
6	SW	P	Switching node of power stage. Connect to power inductor.

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information

SOT-23-6L



92911: Device number.

XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

T_{amb} = 25°C, unless otherwise specified

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{IN}	VIN to GND	-0.3	105	V
V_{SW}	SW to GND	-0.3	105	V
V_{BST} - V_{SW}	BST to SW	-	6	V
I_{EN}	Max Input current to EN pin	-	100	μA
All other pins		-0.3	6	V
T_{STG}	Storage temperature	55	150	°C
T_J	Junction temperature	40	150	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{IN}	VIN to GND	4.5	100	V
V_{OUT}	VOUT to GND	0.8~V_{IN}*D_{MAX} (1) or V_{OUT}<24V		V
I_{OUT}	Continuous Output Current	0	1	A

(1) D_{MAX} = T_{ON_MAX} / (T_{ON_MAX} + T_{OFF_MIN}). Typical value is 97%.

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±2000	V
$V_{ESD-CDM}$	Electrostatic discharge	Charged device model	±500	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

SYMBOL	THERMAL METRIC	SOT-23-6L	UNIT
$R_{\Theta JC}$ (1)	Junction to case thermal resistance	21	°C/W
$R_{\Theta JA}$ (1)	Junction to ambient thermal resistance	40	°C/W

(1) Measured on 2-Layer PCB.

7.5 Electrical Characteristics

V_{IN}=60V and T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIN_{UV_R}	VIN UVLO rising voltage	-	4.15	4.3	4.45	V
VIN_{UV_F}	VIN UVLO falling voltage	-	3.9	4.05	4.2	V
VIN_{UV_HYS}	Hysteresis voltage of VIN UVLO	-	-	0.25	-	V
I_S	Shut down current from VIN	V_{EN}=0V	-	3	6	μA
I_Q	Quiescent current from VIN	V_{FB}=0.85V	-	180	-	μA
V_{EN_R}	Enable rising voltage	-	1.1	1.2	1.3	V
V_{EN_F}	Enable falling voltage	-	0.85	0.95	1.05	V
$I_{EN\_PULL\_UP}$	Enable pull-up current	V_{EN}=Low	-	1	-	μA
		V_{EN}=High	-	4	-	μA
V_{EN_CLAMP}	Enable clamp voltage	EN voltage at 100uA current	-	5.7	-	V
V_{FB}	Feedback voltage	-	0.768	0.78	0.792	V
V_{FB_UV}	Feedback UVLO threshold	-	-	0.1	-	V
R_{HS_ON}	High Side power MOS ON resistance	V_{BST}-V_{SW}=5V	-	900	-	mΩ
I_{LIMIT_HS}	High side current limit threshold	-	1.4	1.8	2.2	A
T_{SS}	Soft-start time	V_{FB} from 10% to 90%	-	1.8	-	ms
F_{SW}	Switching frequency	-	400	460	557	kHz
T_{ON_MIN} (1)	Min on time	-	-	150	-	ns
T_{ON_MAX}	Max on time	-	-	10	-	μs
T_{OFF_MIN} (1)	Min off time	-	-	350	-	ns
T_{VALLEY_MAX} (1)	Max valley off time	-	-	100	-	μs
T_{OTP_R} (1)	Thermal shutdown entry threshold	-	-	160	-	°C
T_{OTP_F} (1)	Thermal shutdown recovery threshold	-	-	140	-	°C

(1) Guaranteed by design and engineering sample characterization.

8 Detailed Description

8.1 Overview

The CJ92911 is an easy-to-use, non-sync buck converter, which is integrated with 900mΩ low RDS_ON high-side power MOSFET. The CJ92911 can provide up to 1A continues output current with advanced COT control for fast response and ease loop compensation. The switching frequency of CJ92911 is typically 460kHz, which will help to minimize the solution size and reduce BOM cost.

The CJ92911 has 4.5V to 100V input voltage range, which accommodates a variety of step-down applications. The CJ92911 has built-in full protection features, cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation. The CJ92911 is available in a cost-effective SOT-23-6L package.

8.2 Functional Block Diagram

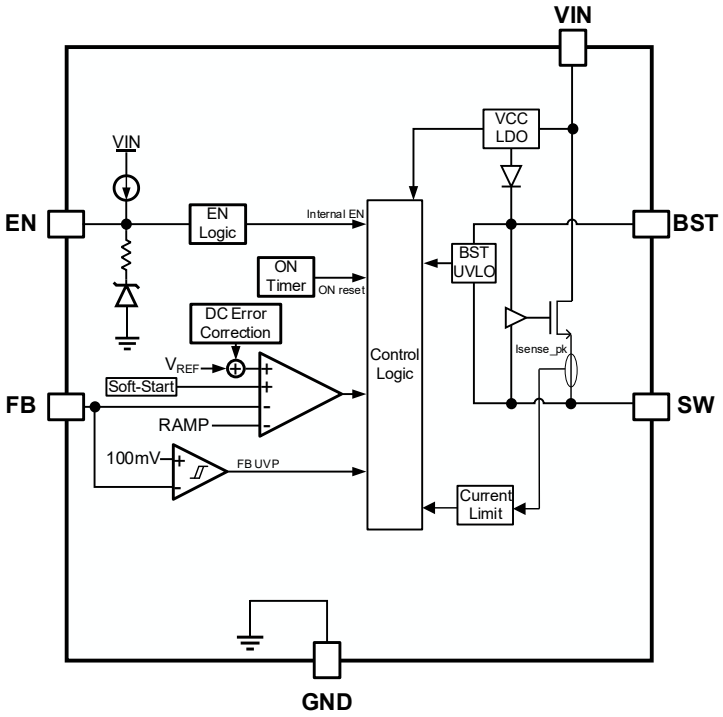


Figure 8-1 Function Block Diagram

8.3 Feature Description

8.3.1 Pulse-Width Modulation (PWM) Operation

The CJ92911 is a fully integrated, non-synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS- FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the On-period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

8.3.2 Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 8-2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the external free-wheeling diode will handle the current.

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

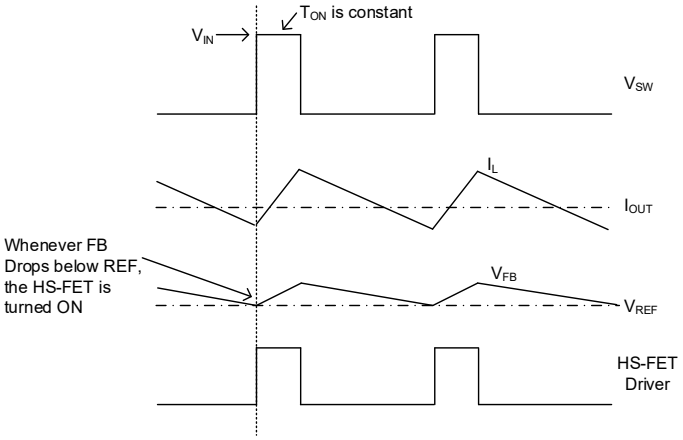


Figure 8-2 Heavy-Load Operation

8.3.3 Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 8-3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on- timer. When the HS-FET is turned off, the free-wheeling diode is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The free-wheeling diode will shut down the negative current and IC goes into tri-state. The output capacitors discharge to GND through the feedback resistor slowly. As a result, the efficiency in light-load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the CJ92911 reduces the switching frequency naturally. High efficiency is achieved at light load.

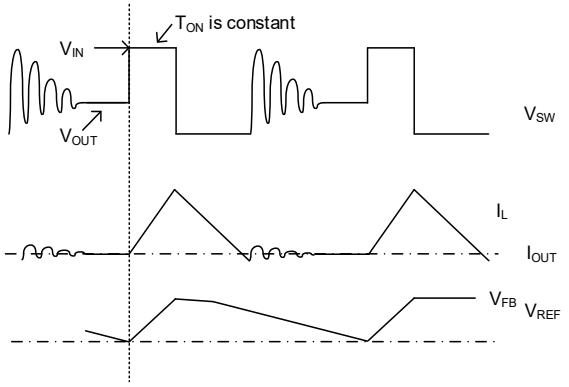


Figure 8-3 Light-Load Operation

As the output current increases from the light-load condition, the HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times 2 \times L \times f_{sw}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

8.3.4 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The CJ92911's UVLO comparator will monitor the input voltage. its UVLO rising threshold is 4.3V, while its falling threshold is consistently 4.05V.

8.3.5 Enable (EN) Control

The CJ92911 has a dedicated enable control pin with positive logic. Drive EN pin voltage higher than 1.2V(typical) to turn on the regulator, and drive EN pin voltage lower than 0.95V(typical) to turn it off.

The EN pin has an internal 4μA pull-up current source, thus the CJ92911 can automatically startup under EN pin floating conditions.

More than 4μA pulldown current is required to shut down the regulator via EN pin, after EN pin is pulled low, its internal pull-up current will be decreased to 1μA to reduce the shutdown current.

By using the two external resistor dividers, it is easy to optimize the start and stop voltage of the system via EN pin:

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} - 4\mu A \times R_{ENUP} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 0.95 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4\mu A \times R_{ENUP} \quad (3)$$

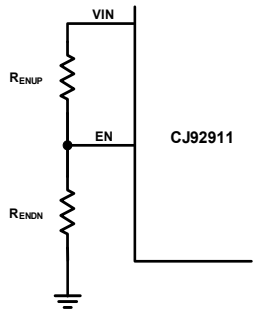


Figure 8-4 EN divider for adjustable UVLO

8.3.6 Internal Soft Start (SS)

Soft start (SS) prevents the output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V. When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set to 1.8ms internally.

8.3.7 High Duty Mode Operation

The CJ92911 will automatically extend the on time to support the application when V_{IN} is close to V_{OUT}. The on time extend circuit will be triggered when T_{OFF_MIN} time is reached. The CJ92911 can support up to 97% maximum duty cycle.

8.3.8 Current Limit and Short Protection

The CJ92911 has a peak current limit and a special valley current. During HS-FET on, the inductor current is monitored. If the sensed inductor current reaches the peak current limit after blanking time, the HS-FET would be turn off. Due to the peak current limit's blanking time, the inductor current might runaway when output shorts to ground for a non-sync buck. The special valley current limit in CJ92911 can prevent this happen. When HS-FET is off and the inductor current is larger than the valley current limit, the HS-FET keeps off until the output current drops below the valley current limit threshold.

When the output is short to ground, CJ92911 will fold back the switching frequency automatically to prevent the current from runaway. It will make the system more reliable.

8.3.9 Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 140°C), the chip is enabled again.

9 Application and Implementation

9.1 Typical Application Circuit

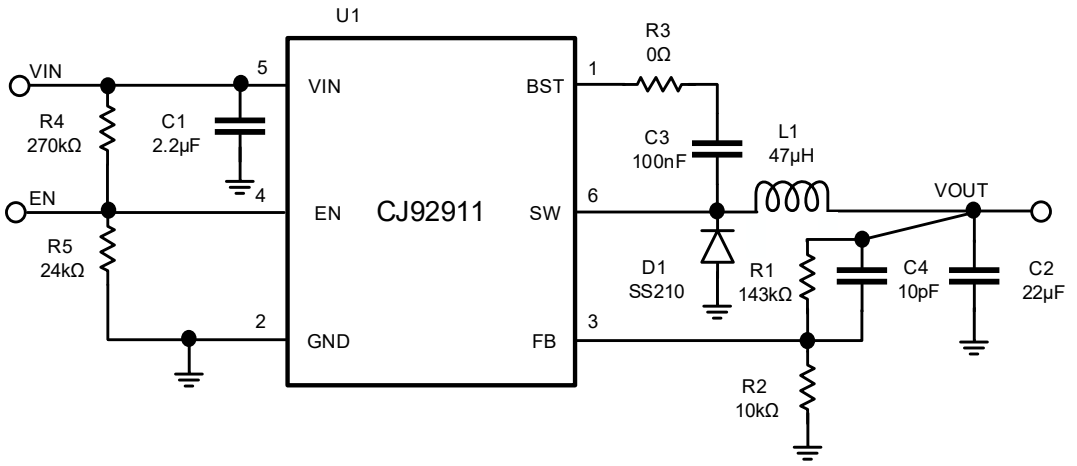


Figure 9-1 V_{IN}=48V, V_{OUT}=12V/1A

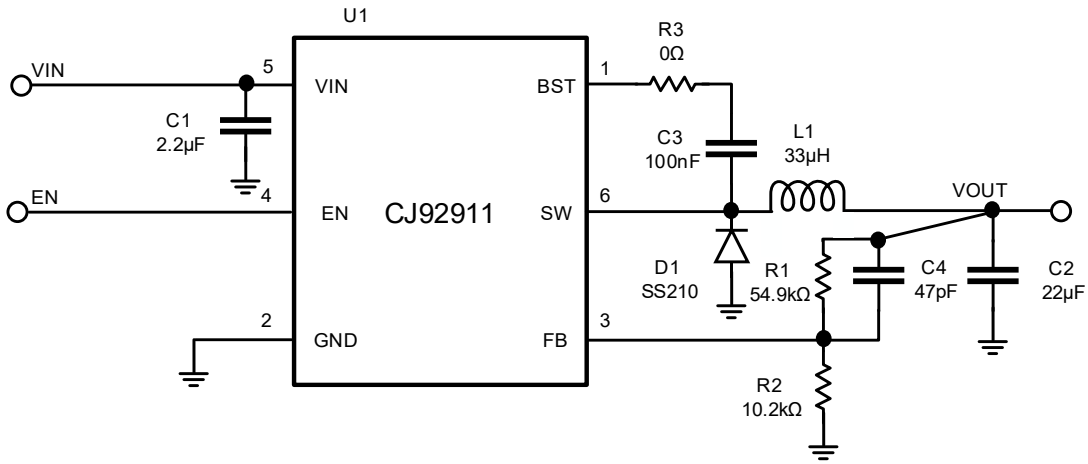


Figure 9-2 V_{IN}=48V, V_{OUT}=5V/1A

9.2 Application Selection

9.2.1 Setting the Output Voltage

The CJ92911 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.78V. The feedback network is shown below Figure.

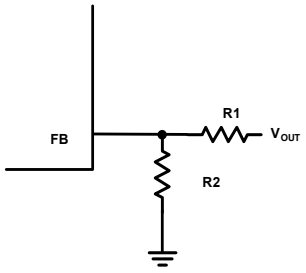


Figure 9-3 Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT} = V_{FB} \times \frac{(R_1 + R_2)}{R_2} \quad (4)$$

9.2.2 Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current.

For most designs, the inductance value can be derived from Equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (5)$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (1)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{ff}(pF)	L (μH)	C_{OUT}(μF)
12	143	10	10	47	22
5	54.9	10.2	47	33	22

(1) For a detailed design circuit, please refer to the Typical Application Circuit

9.2.3 Selecting the Output Capacitor

The output capacitor (C2, C3) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

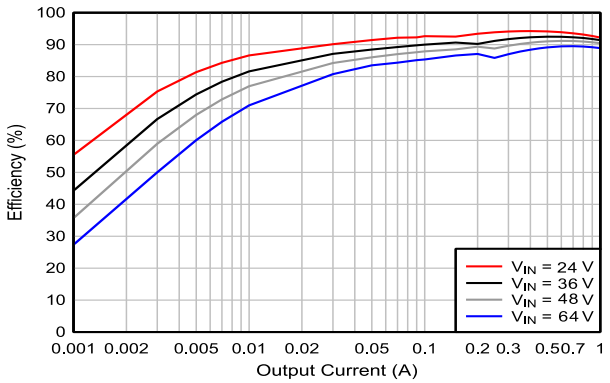
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

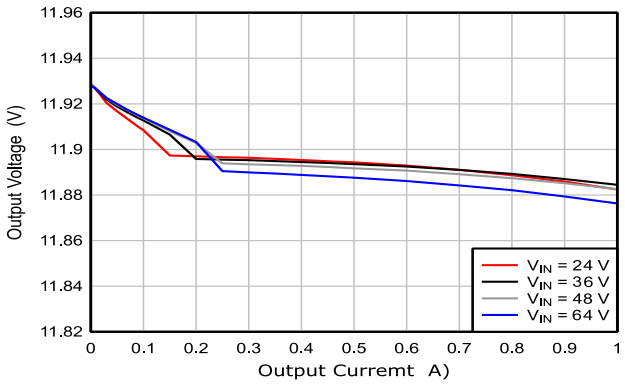
The characteristics of the output capacitor also affect the stability of the regulation system. The CJ92911 can be optimized for a wide range of capacitance and ESR values.

9.3 Typical Performance Characteristics

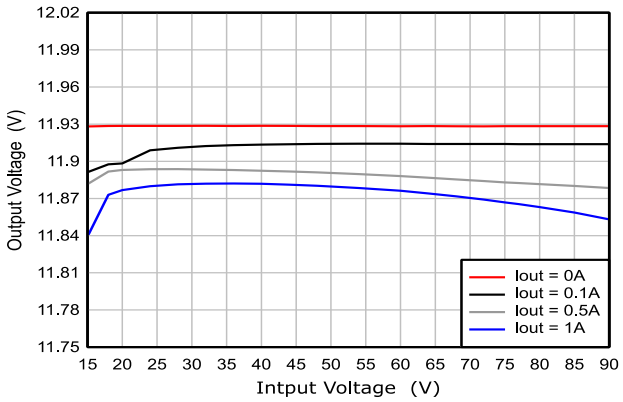
V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.



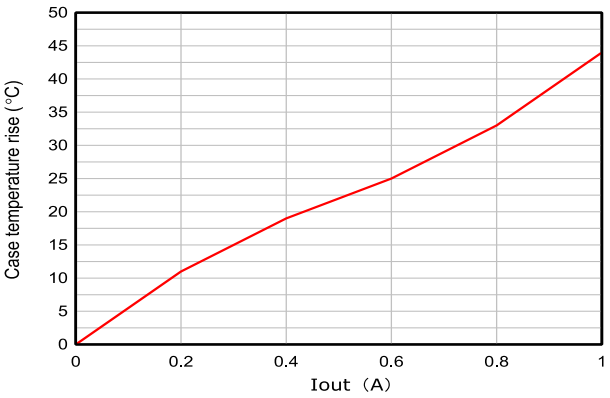
Efficiency vs. Load Current
(V_{OUT}=12V, L=47μH, DCR=135mΩ)



Load Regulation

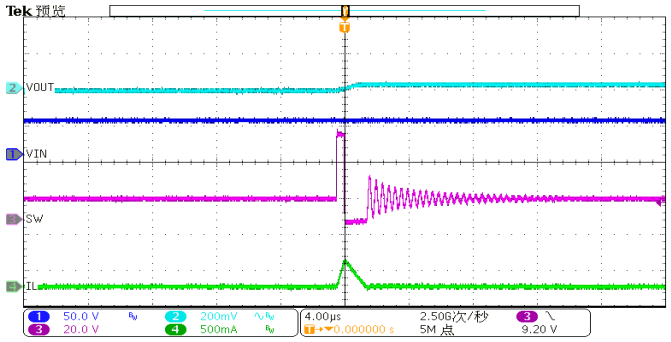


Line Regulation

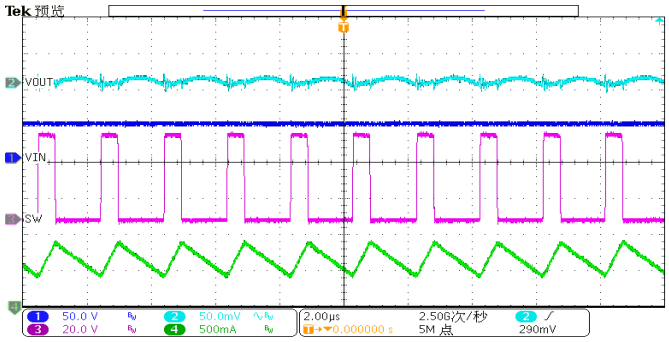


Thermal Rise
(V_{OUT}=12V, no air flow)

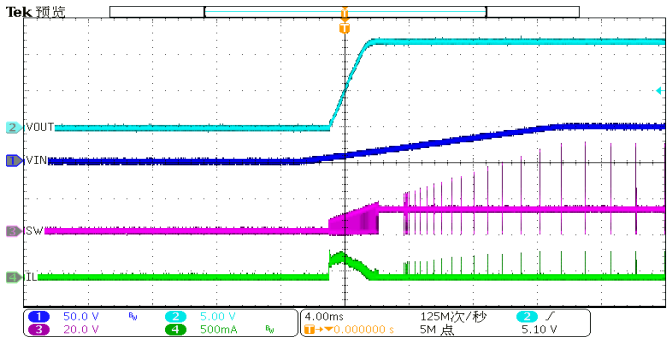
V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.



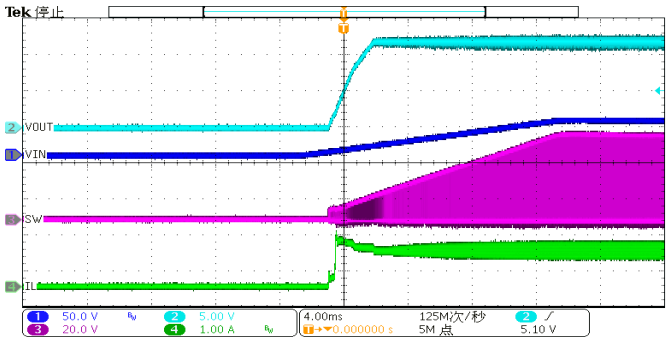
Output Voltage Ripple (I_{OUT} =0A)



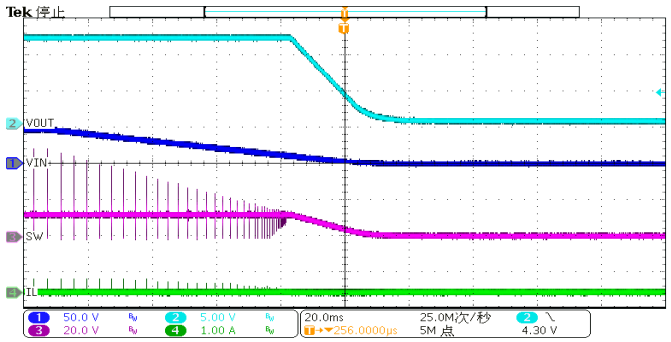
Output Voltage Ripple (I_{OUT} =1A)



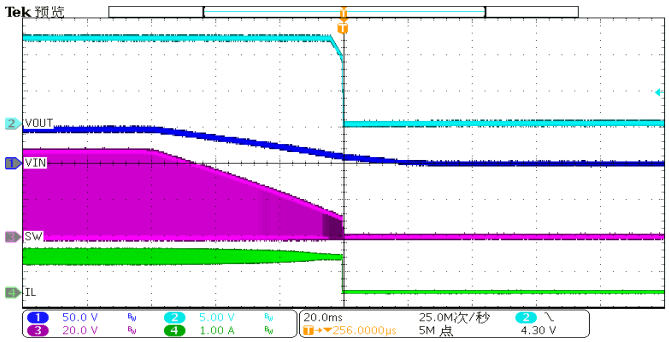
Start-Up through V_{IN} (I_{OUT} =0A)



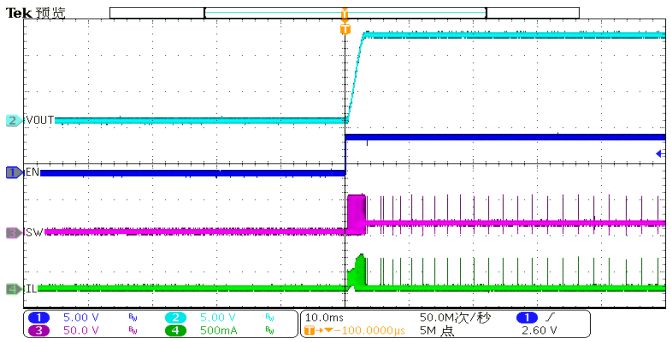
Start-Up through V_{IN} (I_{OUT} =1A)



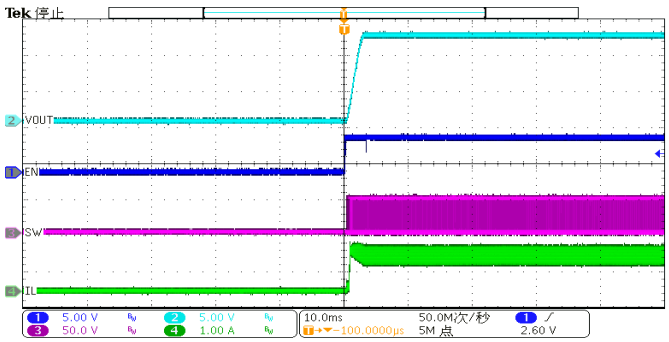
Shut-Down through V_{IN} (I_{OUT} =0A)



Shut-Down through V_{IN} (I_{OUT} =1A)

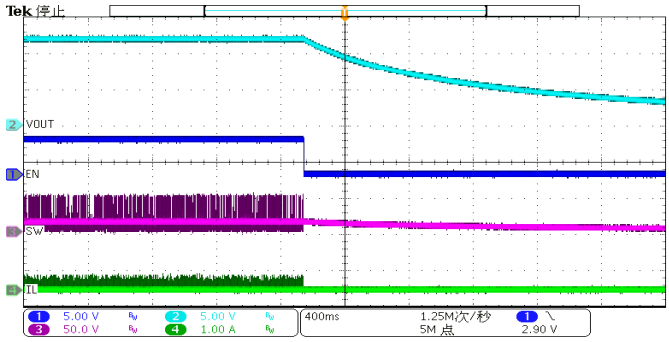


Start-Up through EN (I_{OUT} =0A)

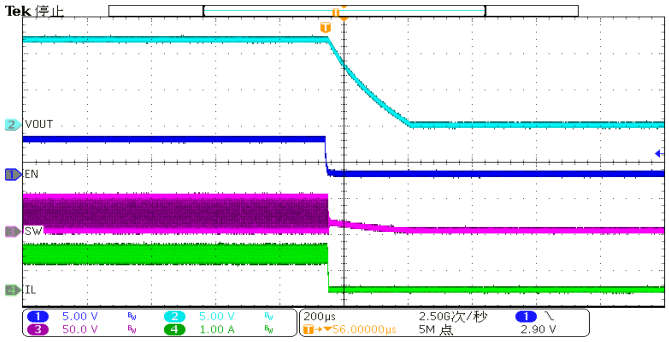


Start-Up through EN (I_{OUT} =1A)

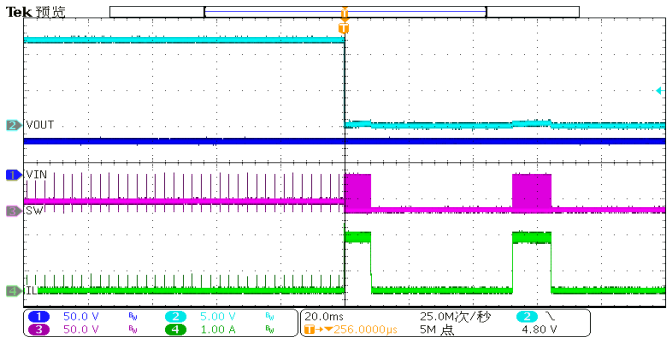
V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.



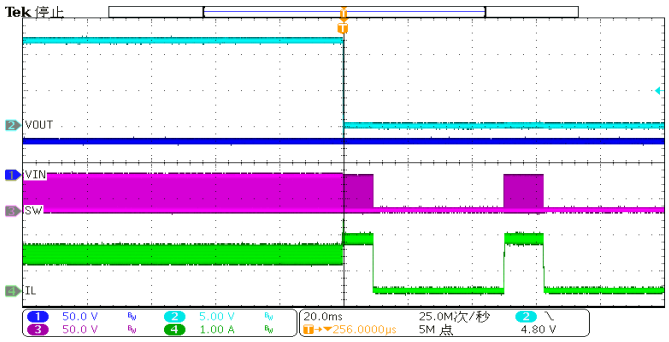
Shut-Down through EN (I_{OUT} =0A)



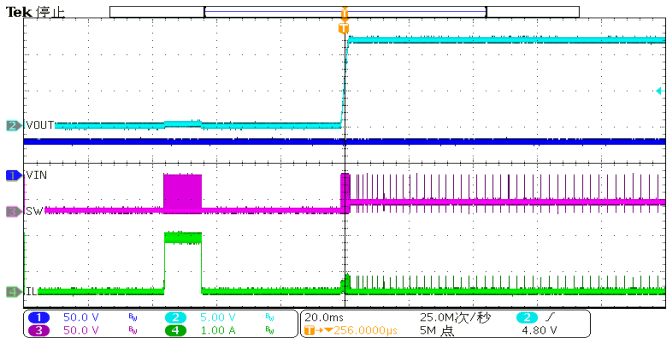
Shut-Down through EN (I_{OUT} =1A)



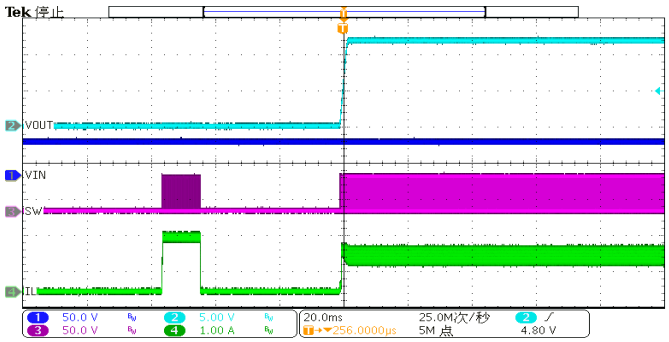
Short-Circuit Entry (I_{OUT} =0A)



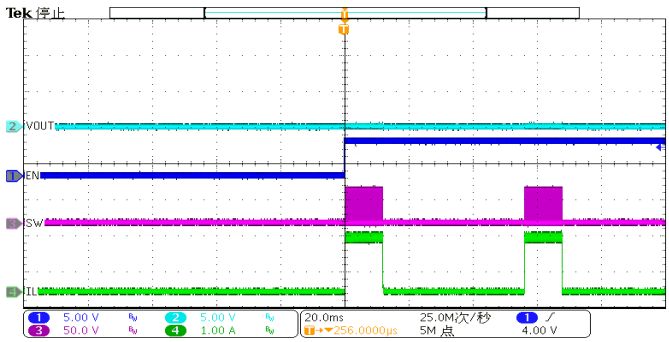
Short-Circuit Entry (I_{OUT} =1A)



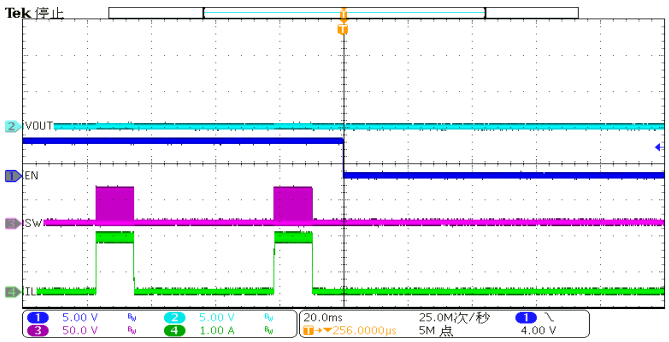
Short-Circuit Recovery (I_{OUT} =0A)



Short-Circuit Recovery (I_{OUT} =1A)

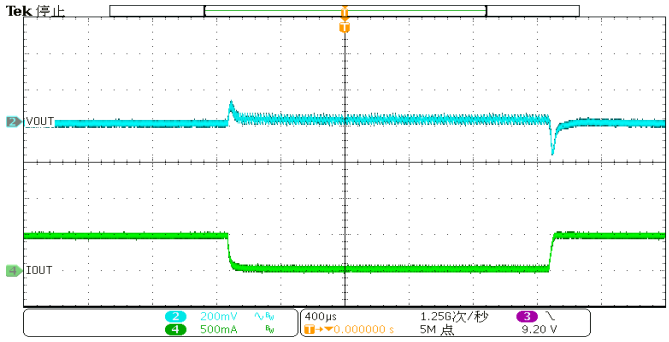


Short-circuit EN power on



Short-circuit EN power off

V_{IN}= 48V, V_{OUT}= 12V, C_{IN} =2.2μF, C_{OUT} =22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.



Load Transient
(I_{OUT} = 0.01A to 0.5A, 2.5A/μs slew rate)

10 Layout

10.1 Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.

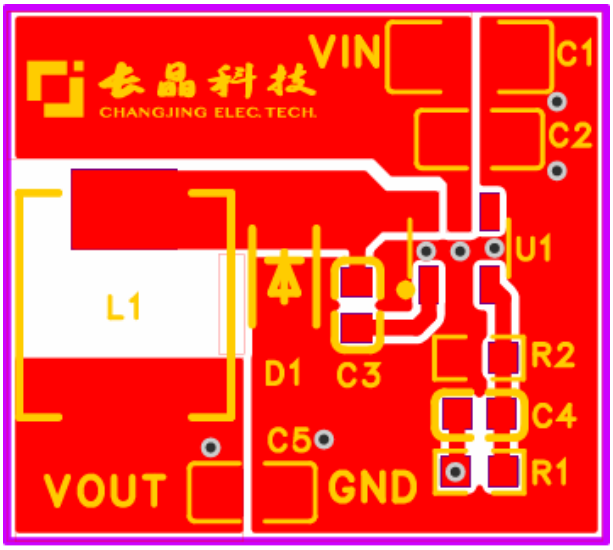


Figure 10-1 Recommend PCB Layout-Top Layer

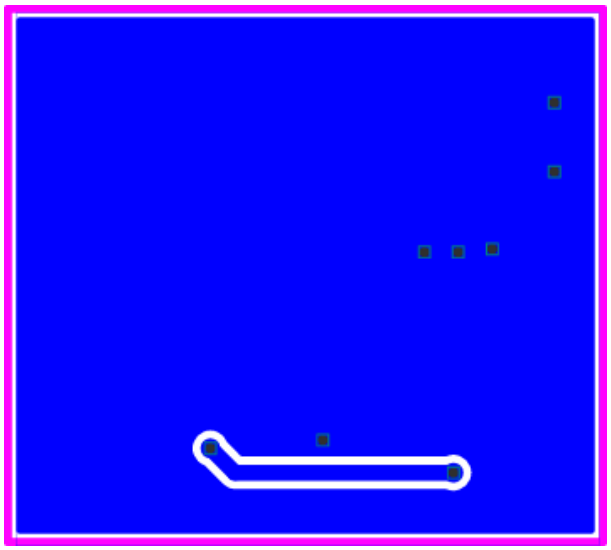
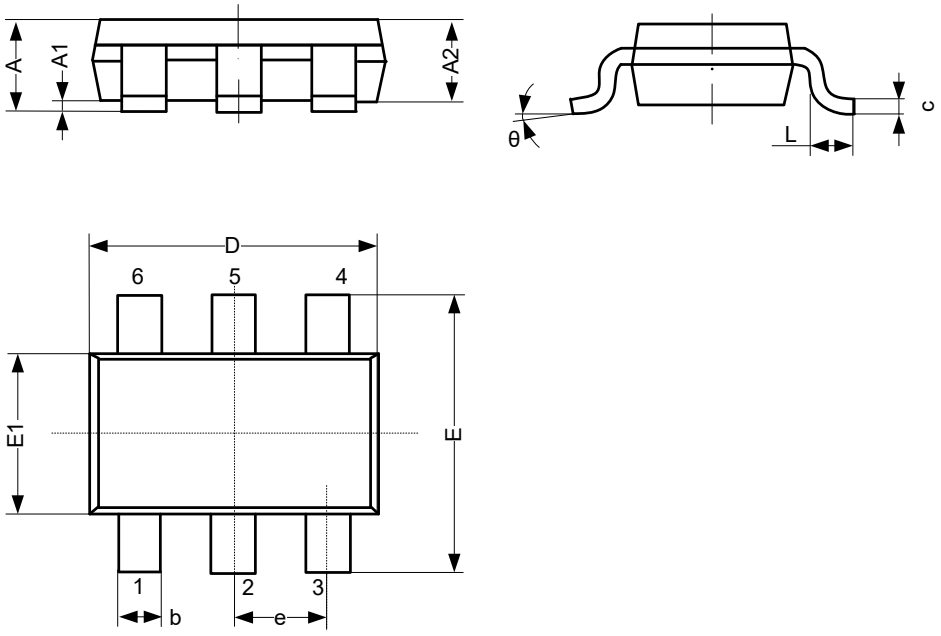


Figure 10-2 Recommend PCB Layout-Bottom Layer

11 Mechanical Information

11.1 SOT-23-6L Mechanical Information

11.1.1 SOT-23-6L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.45
A1	0.00	-	0.15
A2	0.90	-	1.30
b	0.30	-	0.50
c	0.09	-	0.20
D	2.80	-	3.00
E	2.60	-	3.00
E1	1.50	-	1.70
e	0.95 BSC		
L	0.30	-	0.60
Θ	0°	-	8°
Unit：mm			

12 Notes and Revision History

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

12.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

12.3 Revision History

September, 2025: rev - 1.1, Updated the 9.3 Typical Performance Characteristics.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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