JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

Single-phase Full-wave Fan Motor Pre-driver

CJDR1267 / CJDR1267R Motor Pre-drivers

1 Introduction

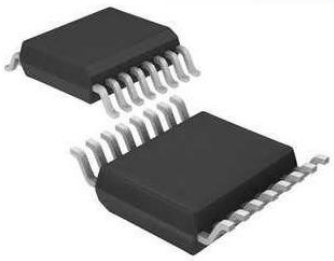
The CJDR1267 and the CJDR1267R are the single-phase bipolar driving motor pre-drivers with the variable speed function compatible with external PWM signal. With a few external parts, a highly-efficient and highly-silent variable drive fan motor with low power consumption can be achieved. This product is best suited for driving of the server requiring large air flow and large current and the fan motor of consumer appliances.

2 Applications

- CPU Cooler / VGA Fan
- Computing & Peripherals
- Industrial
- Server
- Vending Machine

3 Available Package

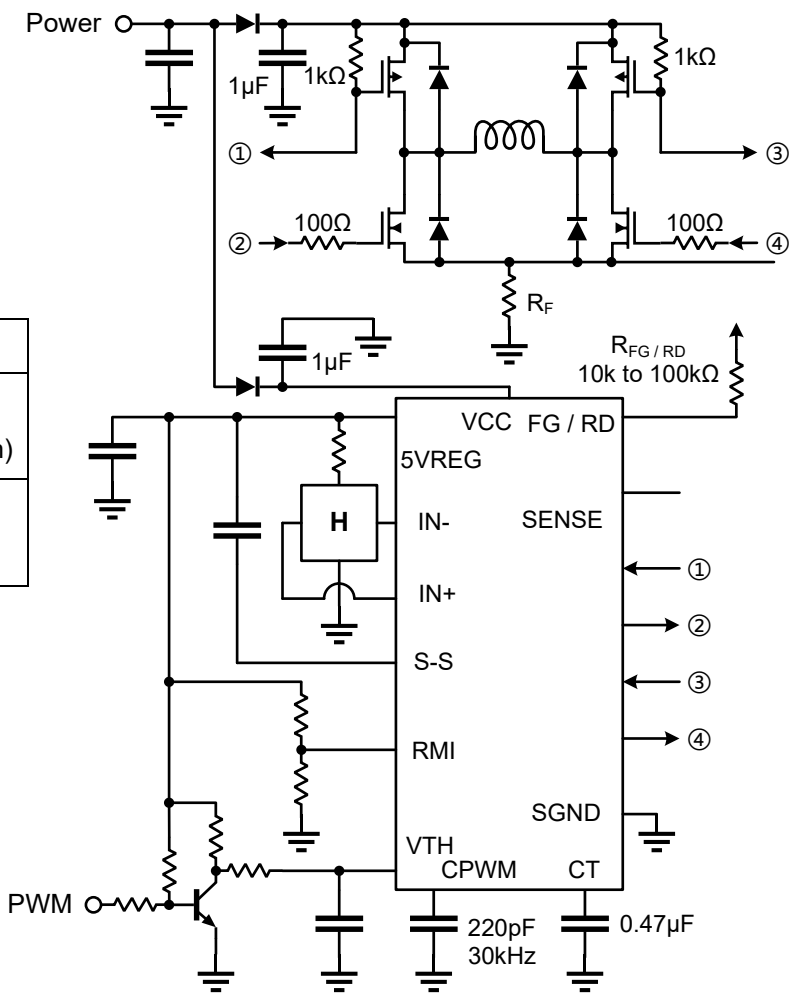
PART NUMBER	PACKAGE
CJDR1267	SSOP16 with FG pin (Rotation speed detection function)
CJDR1267R	SSOP16 with RD pin (Lock detection function)



SSOP16 Package

4 Features

- Single-phase full-wave driving predriver
- Variable speed control possible with external PWM input
- Current limiting circuit incorporated
- Reactive current cut circuit incorporated
- Minimum speed setting pin
- Soft start setting pin
- Lock protection and automatic reset circuits incorporated
- FG output for CJDR1267
- RD output for CJDR1267R
- Thermal shutdown circuit incorporated



12V Typical Application Circuit

5 Pin Configuration and Marking Information

5.1 Pin Configuration and Function

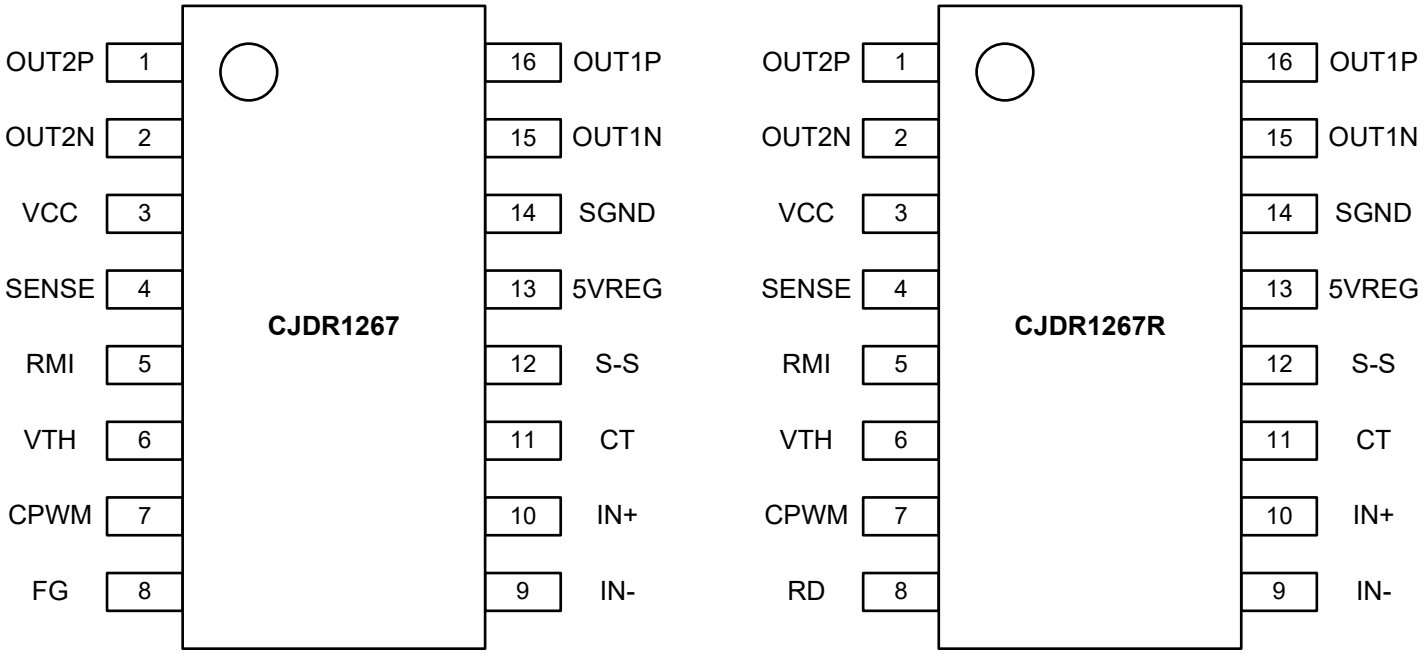


Figure 5-1. SSOP16 Package Pin Map

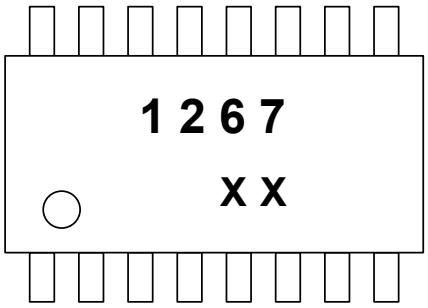
PIN NAME	CJDR1267 SSOP16	CJDR1267R SSOP16	I / O	DESCRIPTION
OUT2P	1	1	O	High side output 2.
OUT2N	2	2	O	Low side output 2.
VCC	3	3	Power	Power input pin. Use a capacitor of 1μF or greater between VCC and ground to achieve power stabilization on the signal side. The position of the capacitor should be placed as close as possible to the VCC pin and ensure that the input trace has a short length and a large width.
SENSE	4	4	I / O	Current limiting detection pin. When the pin voltage exceeds 0.2V, the current is limited, and the operation enters the lower regeneration mode. Connect this pin to GND when it is not to be used.
RMI	5	5	I	Minimum speed setting pin. Perform pull-up with 5VREG when this pin is not to be used. If the IC power supply is likely to be turned OFF first when the pin is used with external power supply, be sure to insert the current limiting resistor to prevent inflow of large current (the same applies to the VTH pin).
VTH	6	6	I	Speed control pin. Connect this pin to GND when it is not used (at full speed). For the control method, refer to the timing chart. For control with pulse input, insert the current limiting resistor and use the pin with the frequency of 20k to 100kHz (20k to 50kHz recommended).

5 Pin Configuration and Marking Information

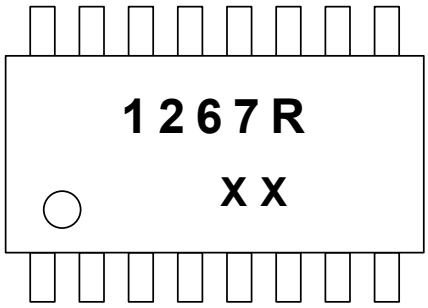
5.1 Pin Configuration and Function (continued)

PIN NAME	CJDR1267 SSOP16	CJDR1267R SSOP16	I / O	DESCRIPTION
CPWM	7	7	I / O	Pin to connect the capacitor for generation of the PWM basic frequency. The use of CP = 220pF causes oscillation at f = 30kHz, which is the basic frequency of PWM. As this is used also for the current limiting canceling signal, be sure to connect the capacitor even when the speed control is not made.
FG	8	-	O	Rotation speed detection pin. This is an open collector output, which can detect the rotation speed from the FG output according to the phase changeover. Keep this pin open when it is not to be used.
RD	-	8	O	Lock the detection pin. This is an open collector output, which can detect the current rotation state. When rotating, it outputs a low level, and when locked, it outputs a high level. Keep this pin open when it is not to be used.
IN-	9	9	I	Hall signal input -.
IN+	10	10	I	Hall signal input +.
CT	11	11	I / O	Pin to connect the lock detection capacitor. The constant-current charge and discharge circuits incorporated cause locking when the pin voltage becomes 3.0V and unlocking when it is 1.1V. Connect the pin to GND when it is not to be used (locking not necessary).
S-S	12	12	I / O	Pin to connect the soft-start setting capacitor. Connect the capacitor between 5VREG and S-S pin. This pin enables setting of the soft start time according to the capacity of the capacitor. See the timing char. Connect the pin to GND when it is not to be used.
5VREG	13	13	I / O	Internal 5V VREF output pin.
SGND	14	14	Ground	Ground pin. SGND is connected to the control circuit power supply system.
OUT1N	15	15	O	Low side output 1.
OUT1P	16	16	O	High side output 1.

5.2 Marking Information



CJDR1267



CJDR1267R

"1267" & "1267R": Device code.

"XX": Code, indicates weekly record information of production.

6 Specifications

6.1 Absolute Maximum Ratings

(over operating free-air temperature range, unless otherwise specified)(1)

CHARACTERISTIC		SYMBOL	VALUE	UNIT
VCC pin maximum supply voltage		$V_{CC\ MAX}$	18	V
OUTN pin maximum output current		$I_{OUTN\ MAX}$	20	mA
OUTP pin maximum sink current		$I_{OUTP\ MAX}$	20	mA
OUT pin output withstand voltage		$V_{OUT\ MAX}$	18	V
VTH pin withstand voltage		$V_{VTH\ MAX}$	7	V
RMI pin withstand voltage		$V_{FG\ MAX}$	7	V
S-S pin withstand voltage		$V_{S\text{-}S\ MAX}$	7	V
FG output pin withstand voltage		$V_{FG\ MAX}$	19	V
FG pin maximum output current		$I_{FG\ MAX}$	10	mA
RD output pin withstand voltage		$V_{RD\ MAX}$	19	V
RD pin maximum output current		$I_{RD\ MAX}$	10	mA
5VREG pin maximum output current		$I_{5VREG\ MAX}$	20	mA
Maximum power dissipation	SSOP16	$P_{D\ Max}$	0.8	W
Maximum junction temperature		$T_{J\ Max}$	150	°C
Storage temperature		T_{stg}	-55 ~ 150	°C
Soldering temperature & time		T_{solder}	260°C, 10s	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

6.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN.	NOM.	MAX.	UNIT
VCC supply voltage	V_{CC}	5.5	-	16	V
VTH input voltage	V_{VTH}	0	-	5.0	V
RMI input voltage	V_{RMI}	0	-	5.0	V
Hall input common-phase input voltage	V_{ICM}	0.2	-	3.0	V
Operating ambient temperature(2)	T_A	-40	-	100	°C

(2) It is necessary to ensure that the operating junction temperature of the device does not exceed the rated value of the recommended operating conditions when using the device for design.

6 Specifications

6.3 Electrical Characteristics

CJDR1267 (V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCC and 5VREG Pins						
Supply current	$I_{CC\ 1}$	During drive	5.5	7.5	9.5	mA
	$I_{CC\ 2}$	During lock protection	5.5	7.5	9.5	
5VREG voltage	V_{5VREG}	I_{5VREG} = 5mA	4.80	4.95	5.1	V
Current limiting voltage	V_{Limit}	-	185	200	215	mV
CPWM Pin						
High level	$V_{CPWM\ H}$	-	2.8	3.0	3.2	V
Low level	$V_{CPWM\ L}$	-	0.9	1.1	1.3	V
Charge current	$I_{CPWM\ 1}$	V_{CPWM} = 0.5V	24	30	36	μA
Discharge current	$I_{CPWM\ 2}$	V_{CPWM} = 3.5V	21	27	33	μA
Oscillation frequency	f_{PWM}	C = 220pF	-	30	-	kHz
CT Pin						
High level	$V_{CT\ H}$	-	2.8	3.0	3.2	V
How level	$V_{CT\ L}$	-	0.9	1.1	1.3	V
Charge current	$I_{CT\ 1}$	V_{CT} = 0.5V	1.6	2.0	2.5	μA
Discharge current	$I_{CT\ 2}$	V_{CT} = 3.5V	0.16	0.20	0.25	μA
Charge / discharge ratio	R_{CT}	I_{CT1} / I_{CT2}	8	10	12	times
S-S Pin						
Discharge current	$I_{S\text{-}S}$	$V_{S\text{-}S}$ = 1.0V	0.4	0.5	0.6	μA
OUTN & OUTP Pins						
OUTN output high level	$V_{OUTN\ H}$	I_{OUT} = 10mA	-	V_{CC} - 0.85	V_{CC} - 1.00	V
OUTN output low level	$V_{OUTN\ L}$	I_{OUT} = 10mA	-	0.90	1.00	V
OUTP output low level	$V_{OUTP\ L}$	I_{OUT} = 10mA	-	0.50	0.65	V
Hall						
Hall input sensitivity	V_{HN}	IN+, IN- different voltage, including offset and hysteresis	-	±10	±20	mV
FG Pin						
FG output low level	$V_{FG\ L}$	I_{FG} = 5mA	-	0.15	0.30	V
FG leakage current	$I_{FG\ L}$	V_{FG} = 19V	-	-	20	μA
VTH and RMI Pins						
VTH bias current	I_{VTH}	CPWM = VTH = 2V	-	-	0.1	μA
RMI bias current	I_{RMI}	CPWM = RMI = 2V	-	-	0.1	μA

6 Specifications

6.3 Electrical Characteristics (continued)

CJDR1267R (V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

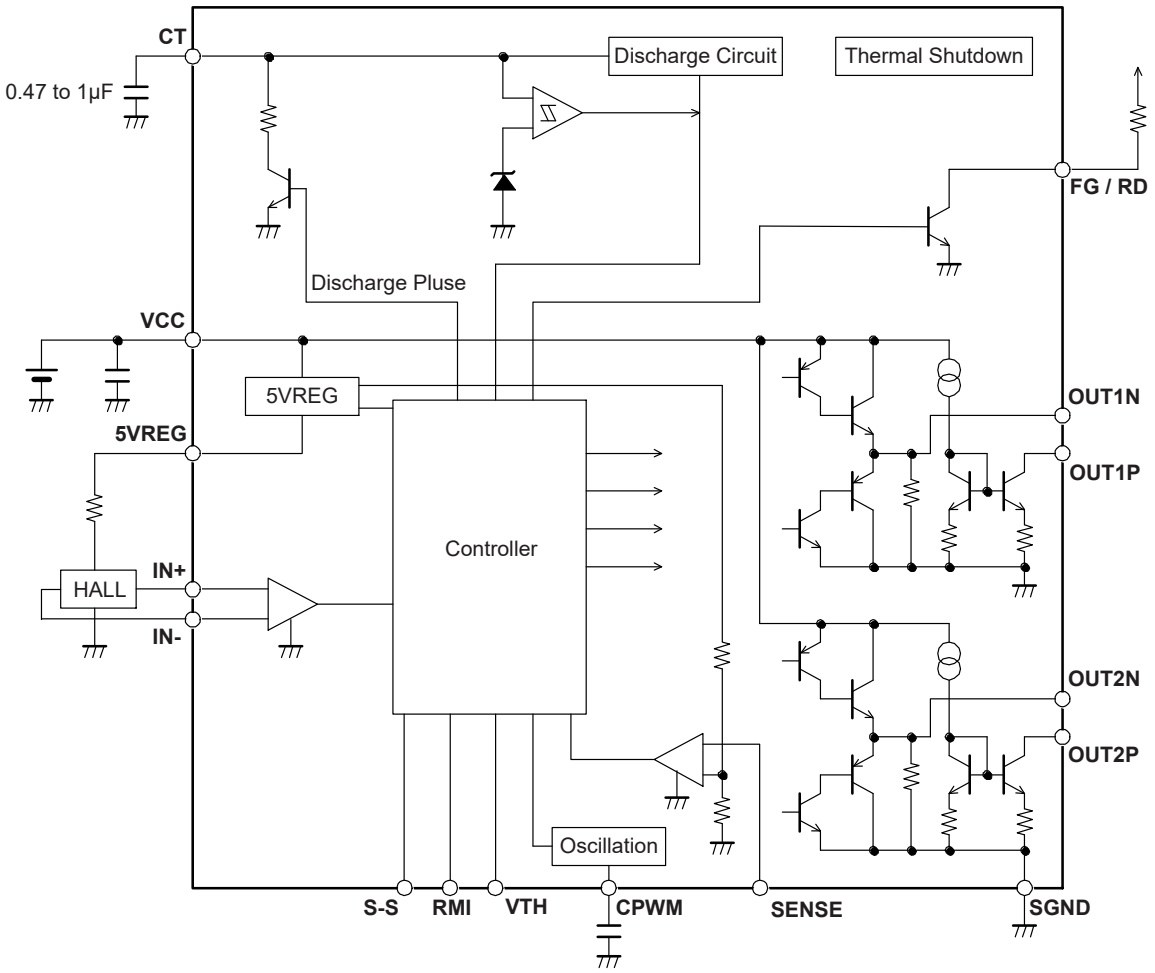
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCC and 5VREG Pins						
Supply current	$I_{CC\ 1}$	During drive	5.5	7.5	9.5	mA
	$I_{CC\ 2}$	During lock protection	5.5	7.5	9.5	
5VREG voltage	V_{5VREG}	I_{5VREG} = 5mA	4.80	4.95	5.1	V
Current limiting voltage	V_{Limit}	-	185	200	215	mV
CPWM Pin						
High level	$V_{CPWM\ H}$	-	2.8	3.0	3.2	V
Low level	$V_{CPWM\ L}$	-	0.9	1.1	1.3	V
Charge current	$I_{CPWM\ 1}$	V_{CPWM} = 0.5V	24	30	36	μA
Discharge current	$I_{CPWM\ 2}$	V_{CPWM} = 3.5V	21	27	33	μA
Oscillation frequency	f_{PWM}	C = 220pF	-	30	-	kHz
CT Pin						
High level	$V_{CT\ H}$	-	2.8	3.0	3.2	V
How level	$V_{CT\ L}$	-	0.9	1.1	1.3	V
Charge current	$I_{CT\ 1}$	V_{CT} = 0.5V	1.6	2.0	2.5	μA
Discharge current	$I_{CT\ 2}$	V_{CT} = 3.5V	0.16	0.20	0.25	μA
Charge / discharge ratio	R_{CT}	I_{CT1} / I_{CT2}	8	10	12	times
S-S Pin						
Discharge current	$I_{S\text{-}S}$	$V_{S\text{-}S}$ = 1.0V	0.4	0.5	0.6	μA
OUTN & OUTP Pins						
OUTN output high level	$V_{OUTN\ H}$	I_{OUT} = 10mA	-	V_{CC} - 0.85	V_{CC} - 1.00	V
OUTN output low level	$V_{OUTN\ L}$	I_{OUT} = 10mA	-	0.90	1.00	V
OUTP output low level	$V_{OUTP\ L}$	I_{OUT} = 10mA	-	0.50	0.65	V
Hall						
Hall input sensitivity	V_{HN}	IN+, IN- different voltage, including offset and hysteresis	-	±10	±20	mV
RD Pin						
RD output low level	$V_{FG\ L}$	I_{FG} = 5mA	-	0.15	0.30	V
RD leakage current	$I_{FG\ L}$	V_{FG} = 19V	-	-	20	μA
VTH and RMI Pins						
VTH bias current	I_{VTH}	CPWM = VTH = 2V	-	-	0.1	μA
RMI bias current	I_{RMI}	CPWM = RMI = 2V	-	-	0.1	μA

7 Detailed Description

7.1 Description

The CJDR1267 and CJDR1267R are the single-phase bipolar driving motor pre-drivers with the variable speed function compatible with external PWM signal. With a few external parts, a highly-efficient and highly-silent variable drive fan motor with low power consumption can be achieved. This product is best suited for driving of the server requiring large air flow and large current and the fan motor of consumer appliances.

7.2 Functional Block Diagram



7.3 Truth Table

(1) Drive lock CPWM = H, VTH = L, RMI = L, S-S = L

CJDR1267

IN-	IN+	CT	OUT1P	OUT1N	OUT2P	OUT2N	FG	MODE
H	L	L	L	L	OFF	H	L	OUT1 → OUT2 Drive
L	H		OFF	H	L	L	OFF	OUT2 → OUT1 Drive
H	L	H	OFF	L	OFF	H	L	Lock Protection
L	H		OFF	H	OFF	L	OFF	

7 Detailed Description

7.3 Truth Table (continued)

CJDR1267R

IN-	IN+	CT	OUT1P	OUT1N	OUT2P	OUT2N	RD	MODE
H	L	L	L	L	OFF	H	L	OUT1 → OUT2 Drive
L	H		OFF	H	L	L	L	OUT2 → OUT1 Drive
H	L	H	OFF	L	OFF	H	OFF	Lock Protection
L	H		OFF	H	OFF	L	OFF	

(2) Speed control CT = L, S-S = L

VTH, RMI	CPWM	IN-	IN+	OUT1P	OUT1N	OUT2P	OUT2N	MODE
L	H	H	L	L	L	OFF	H	OUT1 → OUT2 Drive
		L	H	OFF	H	L	L	OUT2 → OUT1 Drive
H	L	H	L	OFF	L	OFF	H	Regeneration Mode
		L	H	OFF	H	OFF	L	

7.4 Control Timing Chart (Speed Control)

Minimum Speed Setting (Stop) Mode

The low-speed fan rotation occurs at the minimum speed set with the RMI pin. When the minimum speed is not set (RMI pin pulled up to 5VREG), the motor stops.

Low Speed ⇔ High Speed

PMW control is made by comparing the CPWM oscillation voltage (1.1V ⇔ 3.0V) and VTH voltage. Both upper and lower output TRs are turned on when the VTH voltage is low. The upper output TR is turned off when the VTH voltage is high, regenerating the coil current in the lower TR. Therefore, as the VTH voltage decreases, the output on-duty increases, causing increase in the coil current, raising the moor rotation speed.

For CJDR1267, the rotation speed can be monitored with the FG output. For CJDR1267R, the current rotation state can be monitored with the RD output.

Full Speed Mode

The full speed mode becomes effective when the VTH voltage is 1.1V or less (set VTH = GND when the speed control is not to be made).

7 Detailed Description

7.4 Control Timing Chart (Speed Control)

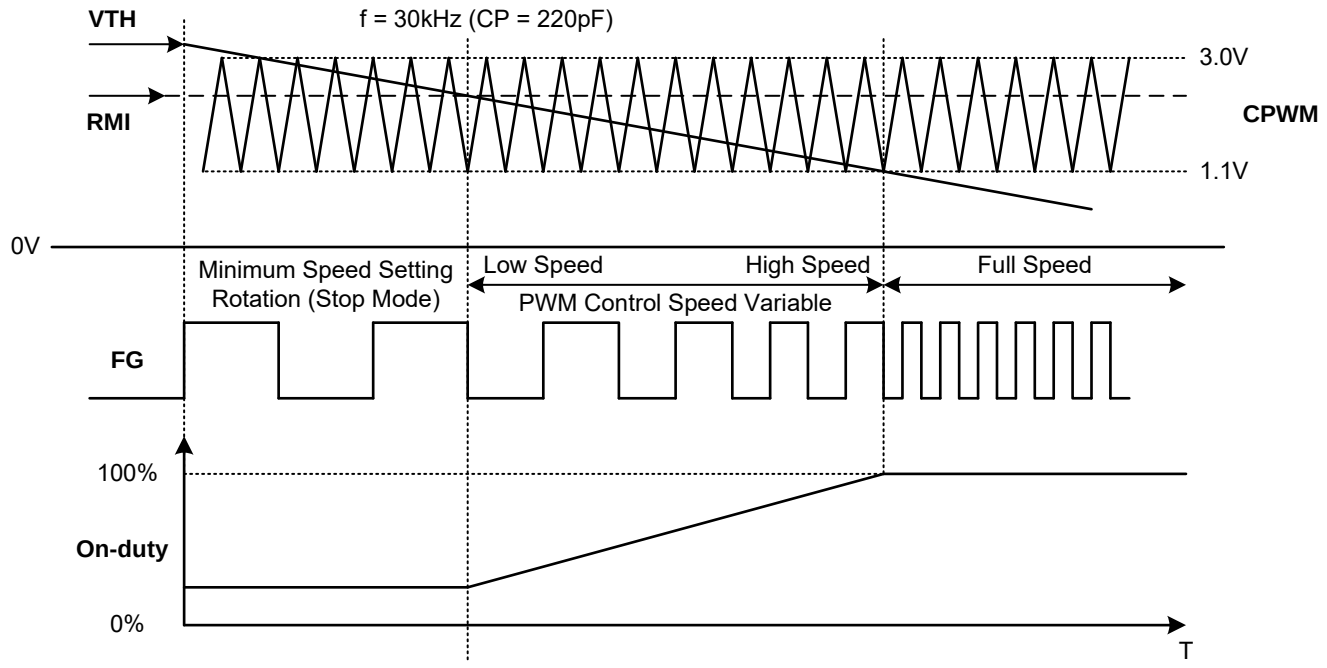


Figure 7-1. Control Timing Chart - Speed Control fro CJDR1267

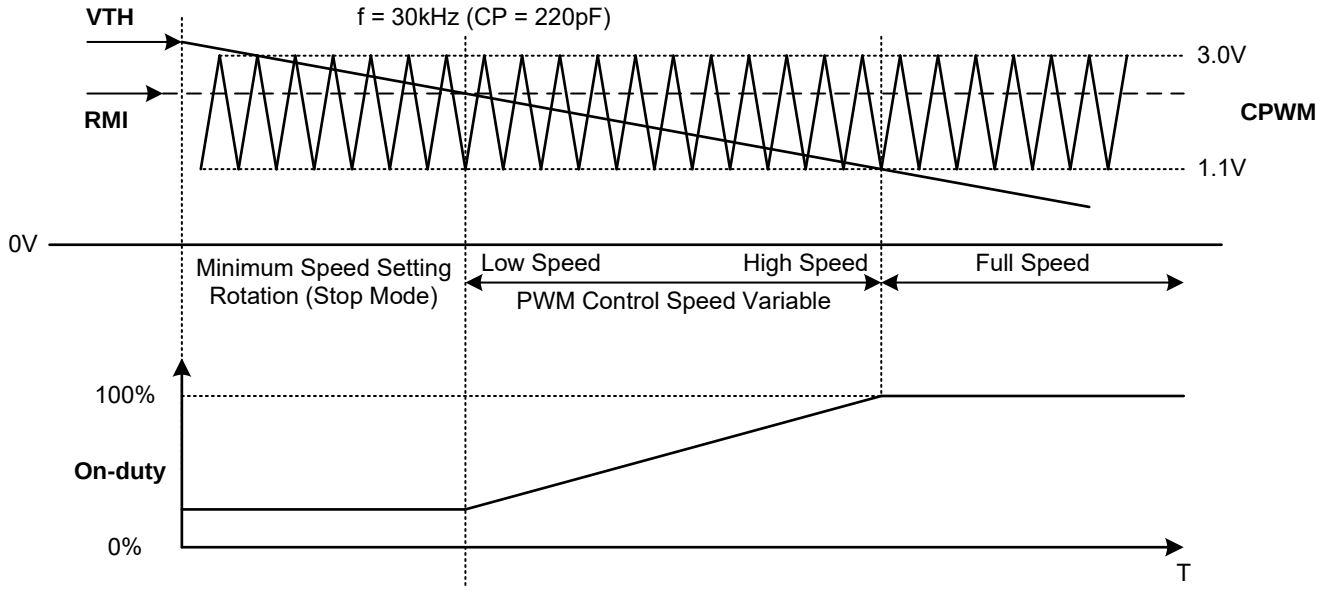


Figure 7-2 Control Timing Chart - Speed Control fro CJDR1267R

7 Detailed Description

7.5 Control Timing Chart (Soft Start)

(1) At VTH < RMI Voltage

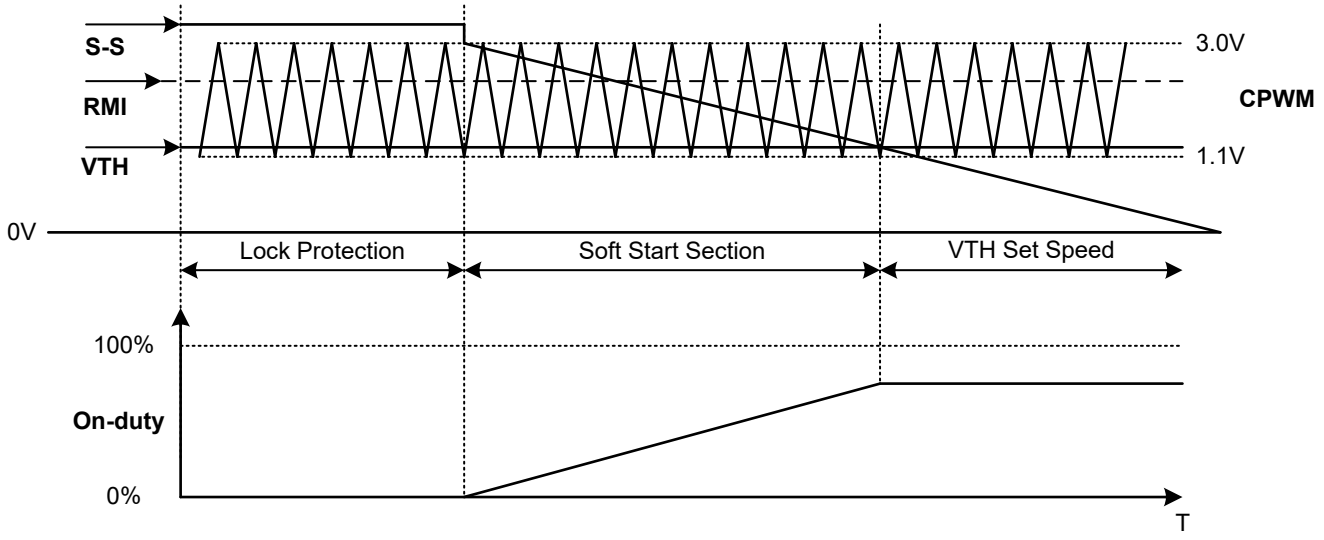


Figure 7-2. At VTH < RMI Voltage

(2) At VTH > RMI Voltage

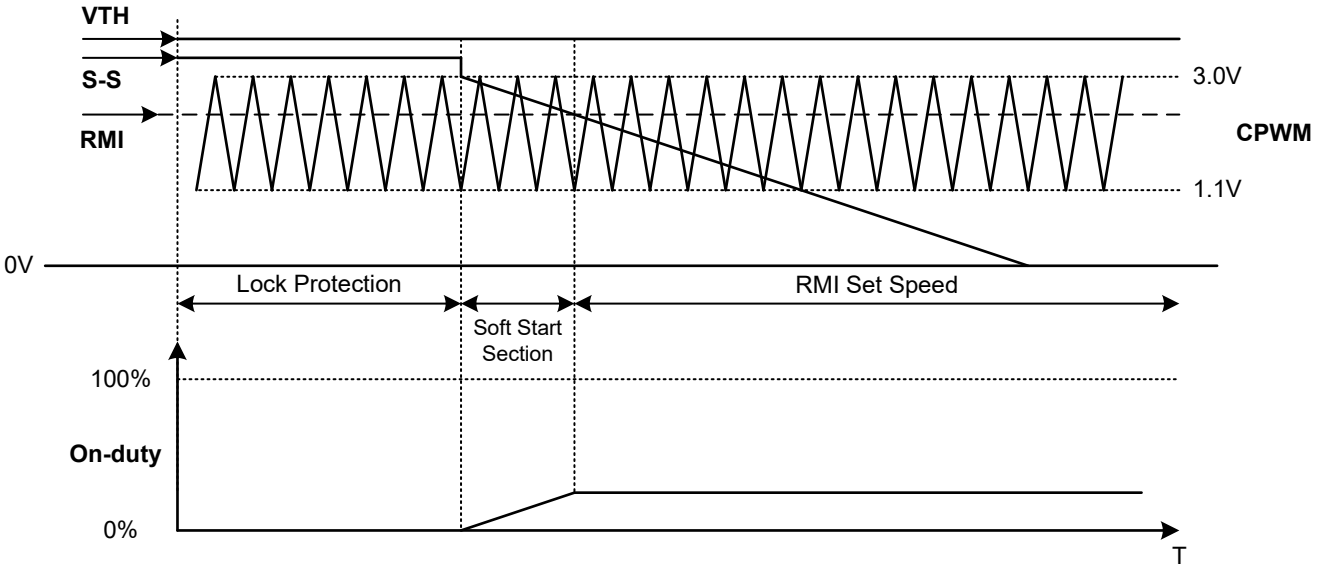
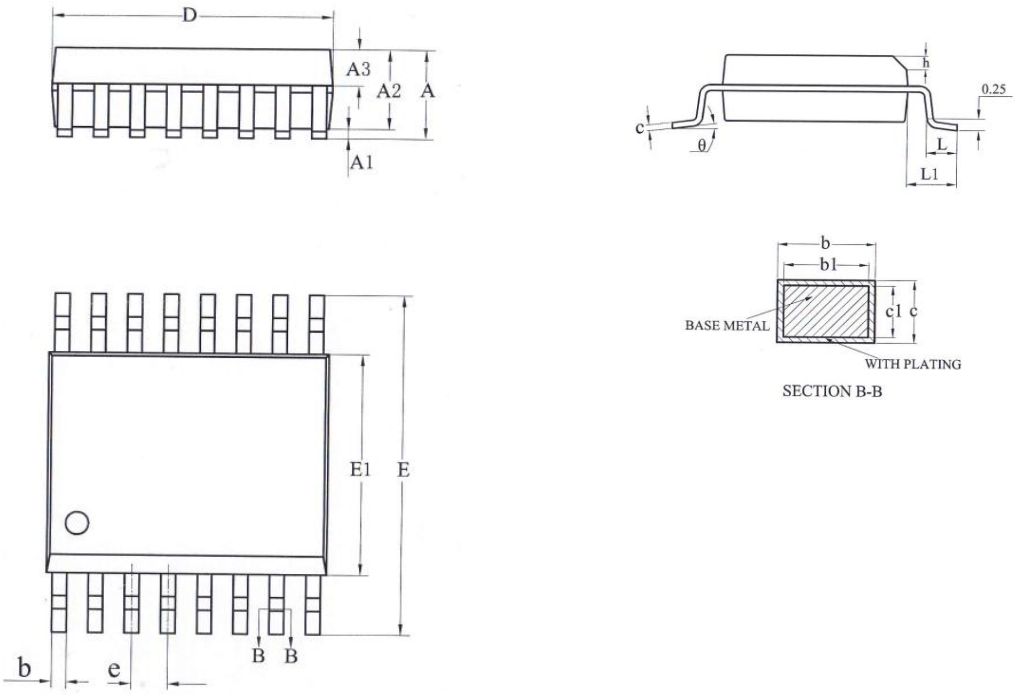


Figure 7-3. At VTH > RMI Voltage

Adjust the S-S pin voltage gradient by means of the capacitance of the capacitor between the S-S pin and 5VREG. Recommended capacitor: 0.1μF to 1μF.

8 Mechanical Information

SSOP16 Outlines Dimensions



SYMBOL	DISMENSIONS IN MILLIMETERS			DISMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.750	-	-	0.069
A1	0.100	-	0.225	0.004	-	0.009
A2	1.300	1.400	1.500	0.051	0.055	0.059
A3	0.600	0.650	0.700	0.024	0.026	0.028
b	0.230	-	0.310	0.009	-	0.012
b1	0.220	0.250	0.280	0.009	0.010	0.011
c	0.200	-	0.240	0.008	-	0.009
c1	0.190	0.200	0.210	0.007	0.008	0.008
D	4.800	4.900	5.000	0.189	0.193	0.197
E	5.800	6.000	6.200	0.228	0.236	0.244
E1	3.800	3.900	4.000	0.150	0.154	0.157
e	0.635BSC			0.025		
h	0.250	-	0.500	0.010	-	0.020
L	0.500	0.650	0.800	0.020	0.026	0.031
L1	1.05REF			0.041REF		
θ	0°	-	8°	0°	-	8°

9 Notes and Revision History

9.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- https: ***www.jscj-elec.com*** for more details.

9.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

9.3 Revision History

October, 2023: changed from rev - 1.0 to rev - 1.1:

- Added new device CJDR1267R.

September, 2023: released CJDR1267 rev - 1.0.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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