CJDR4938, CJDR4939 Motor Pre-Drivers

1 Introduction

The CJDR4938 and the CJDR4939 are a complete set of three-phase brushless DC motor pre-drivers. They can control the operation of three-phase brushless motor by driving 6 N-channel power MOSFETs, and can support the input of up to 36V power supply voltage. When the device works normally, the commutation logic can be determined by three Hall elements with 120° phase difference.

When the CJDR4938 and the CJDR4939 provide drive for the three-phase bridge composed of 6 MOSFETs, their output current will be determined by the ability of external MOSFETs. They are internally integrated with synchronous rectification controlled by pulse width modulation with fixed decay time to limit the possible surge current. During current attenuation, the MOSFET at the appropriate position inside will be turned on to reduce power consumption. When overvoltage occurs, synchronous rectification will be turned off to reduce power supply voltage fluctuation caused by changing current.

The CJDR4938 and the CJDR4939 also have other functions, including locked-rotor protection function that can set rotor detection delay time through external capacitor, thermal shutdown protection, over-voltage protection and under-voltage locking. The logic input mode includes enable control (ENABLE), direction control (DIR), brake control (BRAKEZ) and noise control (SYN). The logic output is Hall signal and FGx pin (CJDR4938 is FG1, CJDR4939 is FG2) output signal, which can be used to detect the rotation speed.

2 Applications

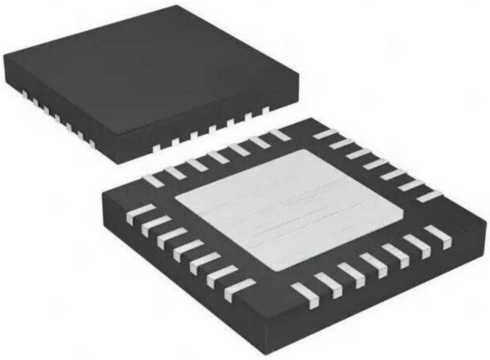
- Electric Tool and Household Appliances
- Mechatronic Products
- Pump

3 Features

- Drives 6 N-channel MOSFETs
- Input Voltage up to 36V
- Synchronous Rectification for Low Power Dissipation
- Internal UVLO and Thermal Shutdown Circuitry
- Hall Element Inputs
- PWM Current Limiting
- Dead Time Protection
- FG Outputs
- Standby Mode
- Lock Detect Protection
- Overvoltage Protection

4 Available Package

PART NUMBER	PACKAGE
CJDR4938	QFNWB5×5-28L
CJDR4939	



QFNWB5×5-28L Package

5 Pin Configuration and Function

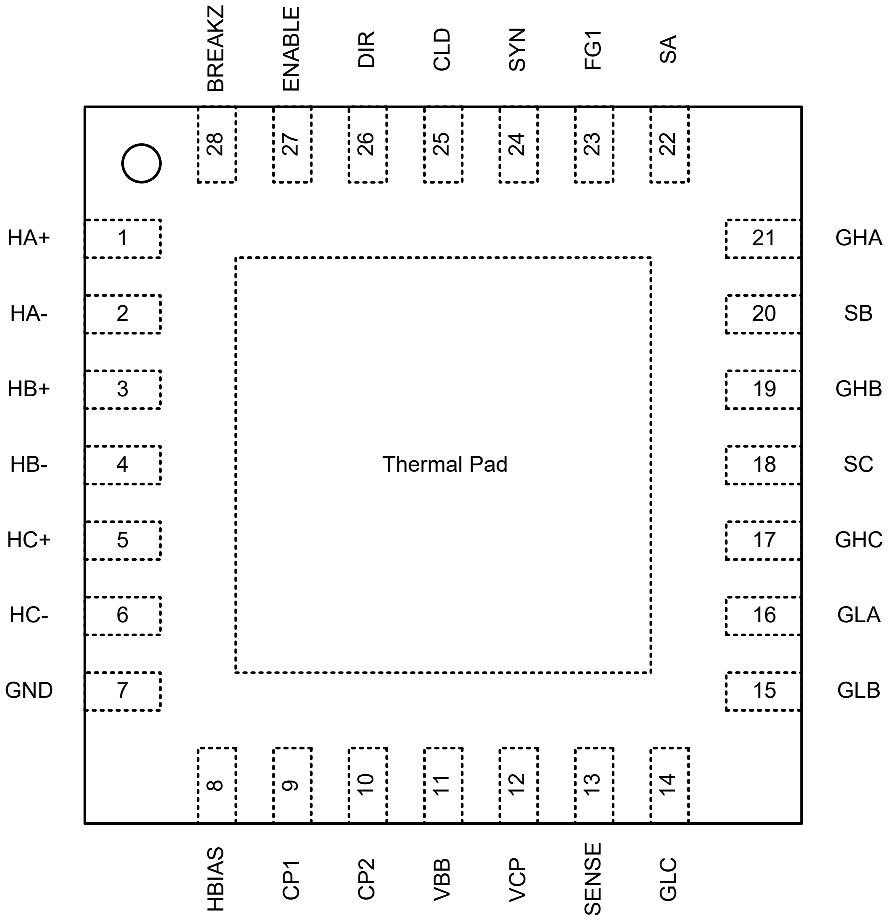


Figure 5-1. CJDR4938 Pin Map

5 Pin Configuration and Function

PIN NAME	CJDR4938	I / O	DESCRIPTION
	QFNWB5×5-28L		
1	HA+	I	HALL A-phase positive terminal input.
2	HA-	I	HALL A-phase negative terminal input.
3	HB+	I	HALL B-phase positive terminal input.
4	HB-	I	HALL B-phase negative terminal input.
5	HC+	I	HALL C-phase positive terminal input.
6	HC-	I	HALL C-phase negative terminal input.
7	GND	Ground	Connect to system ground.
8	HBIAS	I / O	5V power output for HALL element.
9	CP1	I / O	Charge pump capacitor pin 1.
10	CP2	I / O	Charge pump capacitor pin 2.
11	VBB	Power	Power supply.
12	VCP	I / O	Charge pump capacitor pin.
13	SENSE	I / O	Current monitoring pin
14	GLC	I / O	C-phase lower arm bridge grid drive.
15	GLB	I / O	B-phase lower arm bridge grid drive.
16	GLA	I / O	A-phase lower arm bridge grid drive.
17	GHC	I / O	C-phase upper arm bridge grid drive.
18	SC	I / O	C-phase output.
19	GHB	I / O	B-phase upper arm bridge grid drive.
20	SB	I / O	B-phase output.
21	GHA	I / O	A-phase upper arm bridge grid drive.
22	SA	I / O	A-phase output.
23	FG1	O	Speed output pin (3Φ).
24	SYN	O	Noise reduction function pin (active at low level).
25	CLD	I / O	External regulating capacitor pin for locked rotor protection.
26	DIR	I	Motor direction pin.
27	ENABLE	I	External PWM control pin (active at low level).
28	BREAKZ	I	Brake (active at low level).
-	Thermal Pad	-	Connect to system ground.

5 Pin Configuration and Function

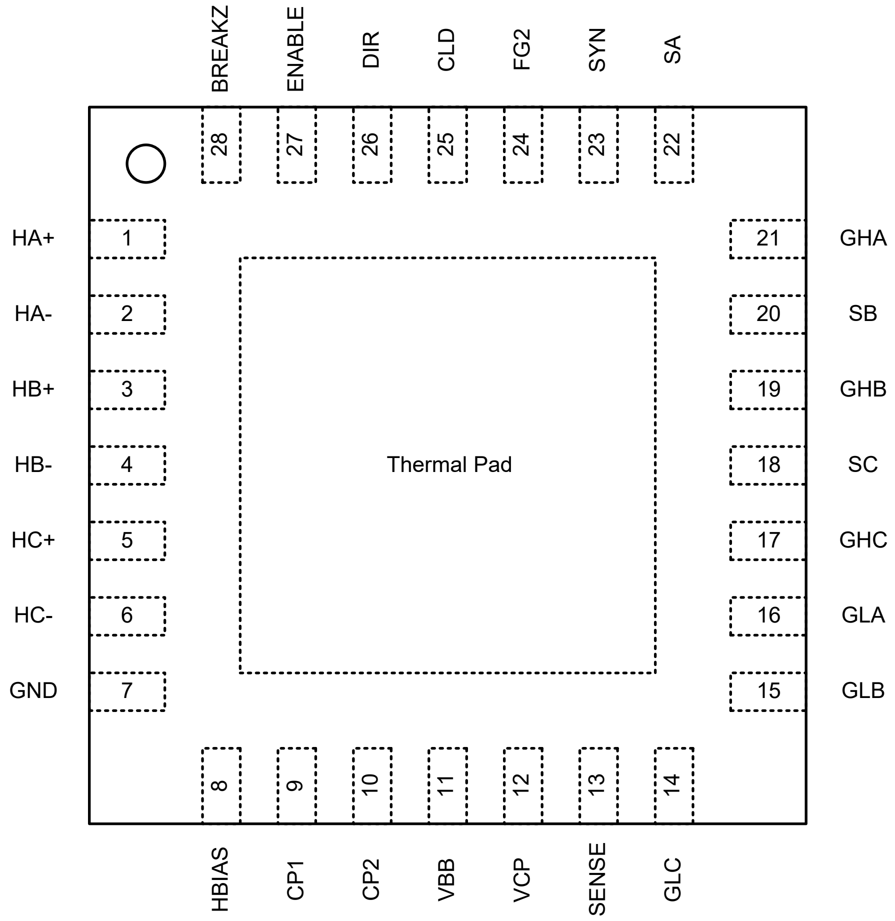


Figure 5-2. CJDR4939 Pin Map

5 Pin Configuration and Function

PIN NAME	CJDR4939	I / O	DESCRIPTION
	QFNWB5×5-28L		
1	HA+	I	HALL A-phase positive terminal input.
2	HA-	I	HALL A-phase negative terminal input.
3	HB+	I	HALL B-phase positive terminal input.
4	HB-	I	HALL B-phase negative terminal input.
5	HC+	I	HALL C-phase positive terminal input.
6	HC-	I	HALL C-phase negative terminal input.
7	GND	Ground	Connect to system ground.
8	HBIAS	I / O	5V power output for HALL element.
9	CP1	I / O	Charge pump capacitor pin 1.
10	CP2	I / O	Charge pump capacitor pin 2.
11	VBB	Power	Power supply.
12	VCP	I / O	Charge pump capacitor pin.
13	SENSE	I / O	Current monitoring pin
14	GLC	I / O	C-phase lower arm bridge grid drive.
15	GLB	I / O	B-phase lower arm bridge grid drive.
16	GLA	I / O	A-phase lower arm bridge grid drive.
17	GHC	I / O	C-phase upper arm bridge grid drive.
18	SC	I / O	C-phase output.
19	GHB	I / O	B-phase upper arm bridge grid drive.
20	SB	I / O	B-phase output.
21	GHA	I / O	A-phase upper arm bridge grid drive.
22	SA	I / O	A-phase output.
23	SYN	O	Noise reduction function pin (active at low level).
24	FG2	O	Speed output pin (3Φ).
25	CLD	I / O	External regulating capacitor pin for locked rotor protection.
26	DIR	I	Motor direction pin.
27	ENABLE	I	External PWM control pin (active at low level).
28	BREAKZ	I	Brake (active at low level).
-	Thermal Pad	-	Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)(1)

CHARACTERISTIC			SYMBOL	VALUE	UNIT
Maximum load supply voltage(2)			V_{BB}	38	V
Hall input voltage range(2)			V_{HX}	-0.3 ~ 7.0	
Logic input voltage range(2)			V_{IN}	-0.3 ~ 7.0	
Maximum power dissipation	CJDR4938	QFNWB5×5-28L	$P_{D\ MAX}$	Internally limited(3)	W
	CJDR4939				
Maximum junction temperature			$T_{J\ Max}$	150	°C
Storage temperature			T_{stg}	-65 ~ 150	°C
Soldering temperature & time			T_{solder}	260°C, 10s	-

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Refer to *Thermal Information* for details.

6.2 Recommend Operating Conditions

PARAMETER(4)	SYMBOL	MIN.	NOM.	MAX.	UNIT
Load supply voltage	V_{BB}	7.5	-	36	V
Operating junction temperature	T_J	-60	-	150	°C
Operating ambient temperature(5)	T_A	-40	-	110	°C

(4) JSCJ recommends that users should not exceed the rated value in the *Recommended Operating Conditions* for the application conditions of the device, so as to ensure the stability of normal operation and reliability of long-term operation. Operation beyond the recommended rated conditions does not mean that the product will fail. The consumers need to evaluate the risks that may be caused by the operation of the product beyond the recommended rated conditions.
(5) It is necessary to ensure that the operating junction temperature of the device does not exceed the rated value of the recommended operating conditions when using the device for design.

6.3 ESD Ratings

ESD RATINGS		SYMBOL	VALUE	UNIT
Electrostatic discharge(6)	Human body model	$V_{ESD\text{-}HBM}$	4000	V

(6) ESD testing is conducted in accordance with the relevant specifications formulated by the Joint Electronic Equipment Engineering Commission (JEDEC). The human body model (HBM) electrostatic discharge test is based on the JESD22-114D test standard, using a 100pF capacitor and discharging to each pin of the device through a resistance of 1.5kΩ.

6 Specifications

6.4 Thermal Information

THERMAL METRIC(7)	SYMBOL	CJDR4938	CJDR4939	UNIT
Junction-to-ambient thermal resistance	$R_{\Theta JA}$	QFNWB5×5-28L		°C/W
		40.0		
Reference maximum power dissipation for continuous operation	$P_{D\ Ref}$	QFNWB5×5-28L		W
		3.1		

(7) T_A = 25°C, tested on the 4-layer PCB based on JEDEC standard.

6.5 Electrical Characteristics

CJDR4938, CJDR4939 (V_{BB} = 24V, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage range	V_{BB}	Operating	7.5	-	36	V
Motor supply current	I_{BB}	f_{PWM} < 30kHz, C_{LOAD} = 1nF	-	4.0	6.0	mA
		Charge pump on, outputs disabled, standby mode	-	3.3	3.6	
HBIAS pin voltage	V_{HBIAS}	I_{HBIAS} = 0 to 24mA	5.1	5.2	5.3	V
HBIAS current limit	$I_{HBIAS\ Limit}$	-	35	-	-	mA
Control Logic						
Logic input voltage	$V_{IN\ (1)}$	-	2.0	-	-	V
	$V_{IN\ (0)}$	-	-	-	0.8	
Logic input pull-up	$R_{IN\ (PU)}$	ENABLE, BRAKEZ, DIR, SYN pins pull-up to independent 5V inside (not HBIAS)	-	50	-	kΩ
Input pin glitch reject	t_{GLITCH}	ENABLE pin	900	1200	1350	ns
		DIR, BRAKEZ pins	700	1000	1300	
ENABLE standby pulse propagation delay	$t_{dENABLE}$	From ENABLE high to outputs off	2.1	3.0	3.9	ms
HBIAS wake-up delay, standby mode	t_{dHBIAS}	C_{HBIAS} = 0.1μF	-	15	25	μs

6 Specifications

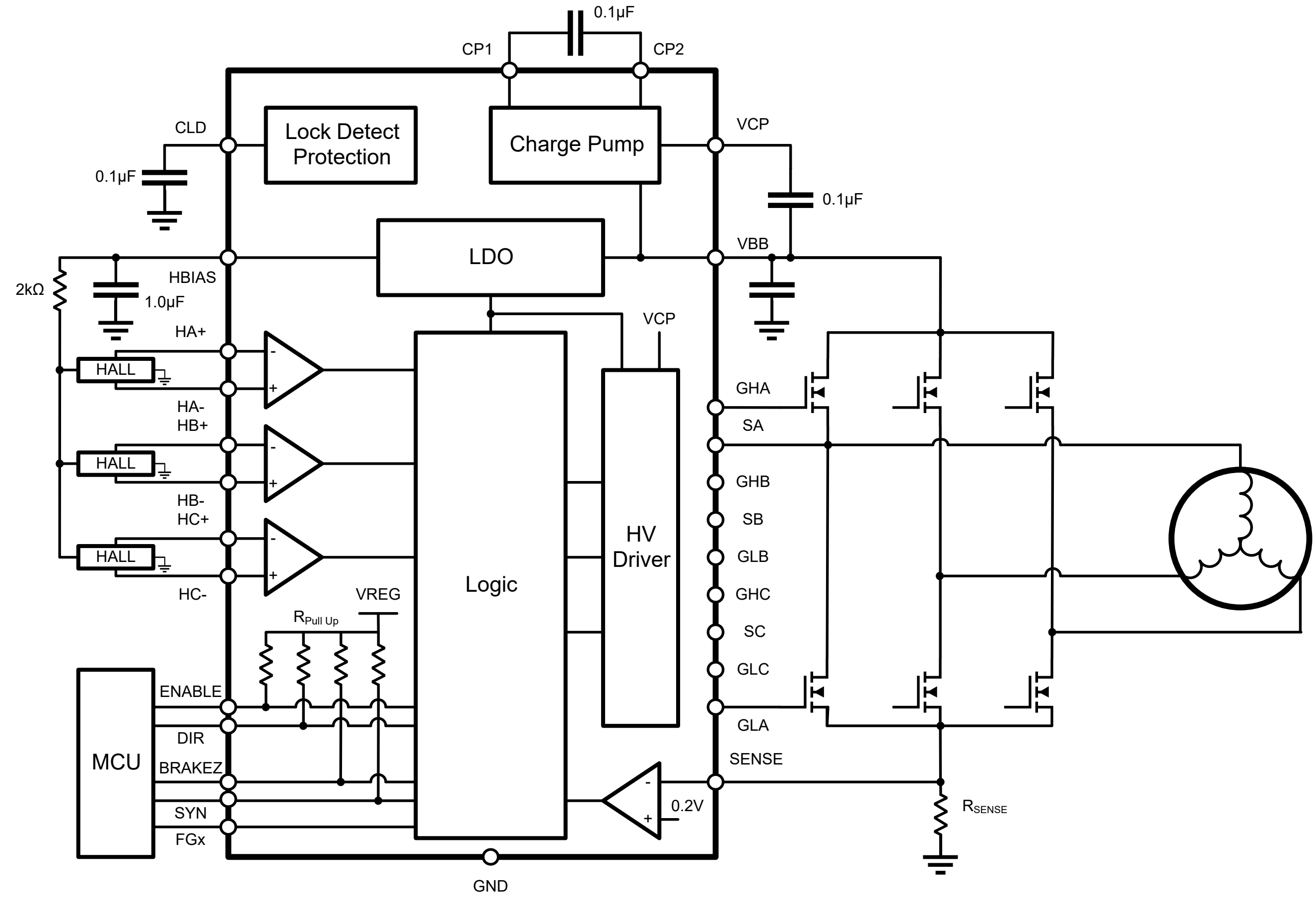
6.5 Electrical Characteristics (continued)

CJDR4938, CJDR4939 (V_{BB} = 24V, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gate Drive						
High-side gate drive output	$V_{GS\ (H)}$	Relative to V_{BB}, I_{GATE} = 2.0mA	-	5.2	-	V
Low-side gate drive output	$V_{GS\ (L)}$	I_{GATE} = 2.0mA	-	5.3	-	V
Gate drive current (Sourcing)	I_{GATE}	GH = GL = 4.0V	20	30	-	mA
Gate drive pull down resistance	R_{GATE}	-	10	28	40	Ω
Dead time	t_{DEAD}	-	700	1000	1300	ns
Current limit input threshold	V_{REF}	-	-	200	-	mV
Fixed off-time	t_{OFF}	-	18	25	37	μs
Protection						
Thermal shutdown temperature	T_{SD}	-	155	170	185	°C
Thermal shutdown hysteresis	ΔT_{SD}	-	-	20	-	°C
VBB UVLO threshold	$V_{BB\ UVLO}$	-	6.9	7.1	7.4	V
VBB UVLO hysteresis	$\Delta V_{BB\ UVLO}$	-	-	200	-	mV
VCP UVLO	$V_{CP\ UVLO}$	Relative to V_{BB}, I_{GATE} = 2.0mA	4.6	-	6.0	V
Lock detect duration	t_{lock}	C = 0.1μF	1.5	2.0	2.5	s
VBB overvoltage threshold	V_{BBOV}	-	28.5	29.0	29.5	V
VBB overvoltage hysteresis	ΔV_{BBOV}	-	-	2.0	-	V
Hall Logic						
Hall input current	I_{HALL}	V_{IN} = 0.2 ~ 3.5V	-1.0	0	1.0	μA
Common mode input range	V_{CMR}	-	0.2	-	3.5	V
Hall thresholds	V_{TH}	Difference between Hall inputs at transitions	-	±10	-	mV
Hall thresholds hysteresis	ΔV_{TH}	T_J = -40 to 125°C	5	20	40	mV
Pulse reject filter	t_{pulse}	-	-	2.0	-	μs
FG						
FG pin voltage	V_{FG}	-	0	-	6.0	V
FG pin current	I_{FG}	-	-	-	14	mA
FG output saturation voltage	$V_{FG\ (sat)}$	I_{FG} = 2.0mA	-	-	0.5	V
FG leakage current	I_{FGlkg}	V_{FG} = 5.0V	-	-	1.0	μA

7 Detailed Description

7.1 Function Block Diagram



7.2 Logic Table State

CONDITION		Inputs					Resulting Pre-driver outputs						Motor Output		
		HA	HB	HC	BRAKEZ	ENB	GHA	GLA	GHB	GLB	GHC	GLC	A	B	C
DIR = 1 (Forward)	A	+	-	+	HI	LO	HI	LO	LO	HI	LO	LO	HI	LO	Z
	B	+	-	-	HI	LO	HI	LO	LO	LO	LO	HI	HI	Z	LO
	C	+	+	-	HI	LO	LO	LO	HI	LO	LO	HI	Z	HI	LO
	D	-	+	-	HI	LO	LO	HI	HI	LO	LO	LO	LO	HI	Z
	E	-	+	+	HI	LO	LO	HI	LO	LO	HI	LO	LO	Z	HI
	F	-	-	+	HI	LO	LO	LO	LO	HI	HI	LO	Z	LO	HI
DIR = 0 (Reverse)	A	+	-	+	HI	LO	LO	HI	HI	LO	LO	LO	LO	HI	Z
	F	-	-	+	HI	LO	LO	LO	HI	LO	LO	HI	Z	HI	LO
	E	-	+	+	HI	LO	HI	LO	LO	LO	LO	HI	HI	Z	LO
	D	-	+	-	HI	LO	HI	LO	LO	HI	LO	LO	HI	LO	Z
	C	+	+	-	HI	LO	LO	LO	LO	HI	HI	LO	Z	LO	HI
	B	+	-	-	HI	LO	LO	HI	LO	LO	HI	LO	LO	Z	HI
DIR = X	Fault	+	+	+	HI	X	LO	LO	LO	LO	LO	LO	Z	Z	Z
	Fault	-	-	-	HI	X	LO	LO	LO	LO	LO	LO	Z	Z	Z
	Brake	X	X	X	LO	X	LO	HI	LO	HI	LO	HI	LO	LO	LO

7 Detailed Description

7.2 Logic Table State (continued)

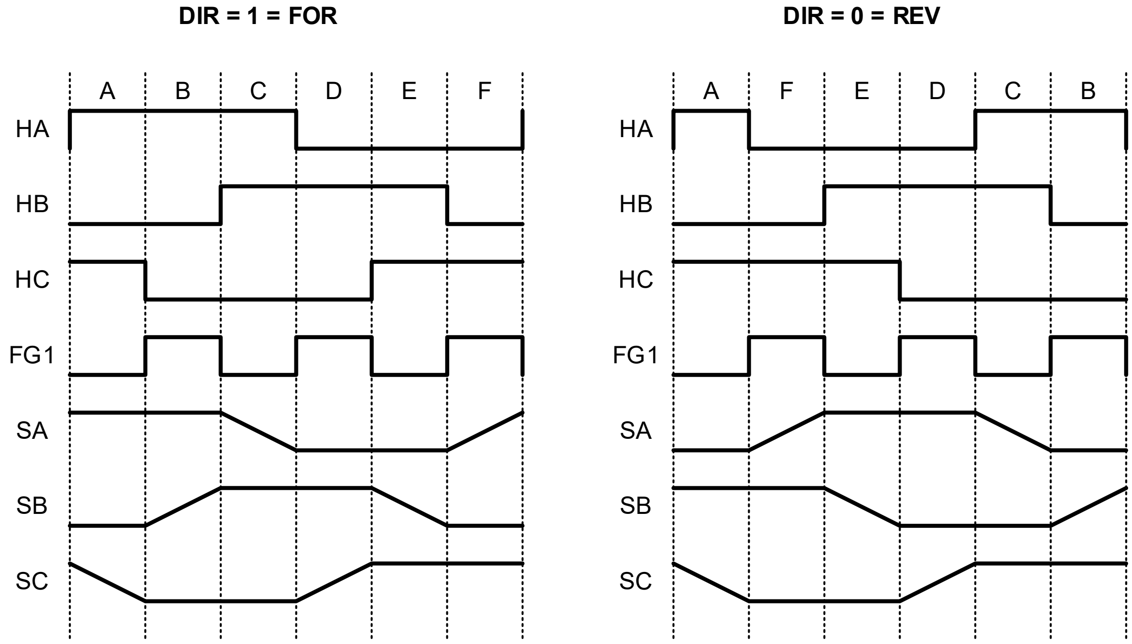


Figure 7-1. CJDR4938 Logic Table State

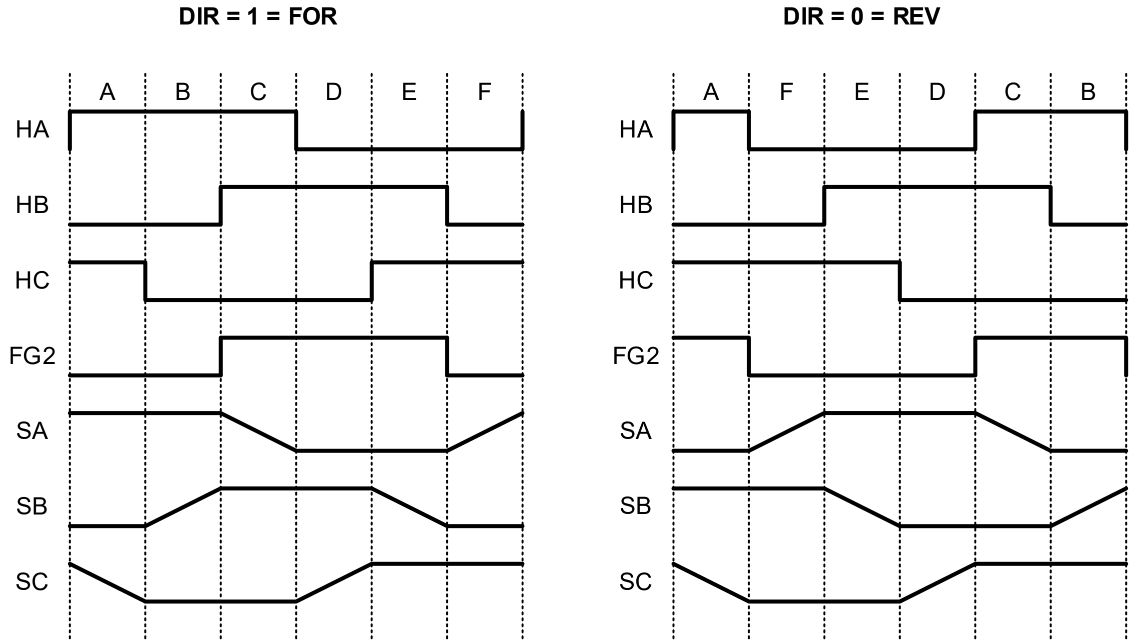


Figure 7-2. CJDR4939 Logic Table State

7 Detailed Description

7.3 Power-up and Standby Modes Timing Diagram

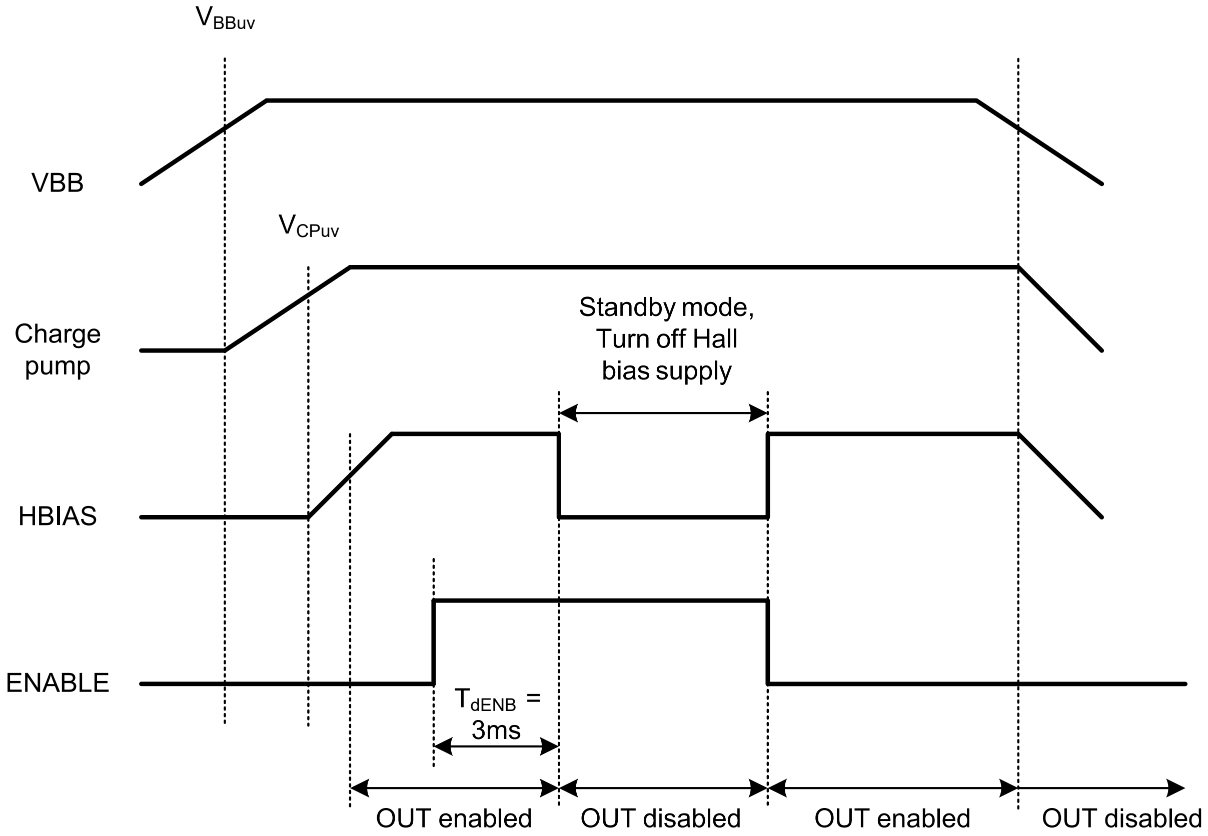


Figure 7-3. CJDR4938, CJDR4939 Power-up and Standby Modes Timing Diagram

7 Detailed Description

7.4 Feature Description

Current Regulation

The load current is controlled by an internal pulse width modulation (PWM) control circuit with a fixed off-time. When the output of the full bridge is switched on, the current in the motor winding increases until a rectified value, I_{TRIP}, is reached, at which point the sensing comparator resets the source pole to enable the latch, closes the source driver, and the load inductor causes the current to decay for a fixed period of time.
The value of I_{TRIP} can be obtained from the following formula:

$$I_{TRIP} = \frac{200mV}{R_{SENSE}}$$

Fixed Off-Time

The typical fixed off-time is set to 25μs.

PWM Blank Timer

When the source driver is switched on, current spikes occur in R_{SENSE} due to the reverse recovery current of the clamp diode and the switching transient associated with the distributed capacitance in the load. To prevent this current spike from incorrectly resetting the source ENABLE latch, the sensor comparator will remain blank and not work for some time. A blank time timer runs after the shutdown time counter is complete, leaving the sensor comparator supply blank. When using external PWM control, a DIR change or an ENBALE on triggers the function of blank timer counting. The typical value for the duration of a blank count is a fixed 1.5μs.

Enable Logic

ENABLE pin can allow external PWM control signal input. When ENABLE is at low level, the corresponding sink source pair will be connected and the load current will gradually increase. When ENABLE is at high level, the corresponding drive will be turned off and the load current will gradually decrease. If ENABLE remains low for a long time, the load current will gradually increase until it reaches the level set by the internal current control circuit. The typical frequency of PWM control is in the range of 20 ~ 30kHz. If the high level pulse width of ENABLE exceeds 3ms (typical), the gate output will be disabled. The control logic of ENBALE can be viewed in the following table.

Table 7-1. Enable Control Logic

ENABLE PIN SETTING	OUTPUTS	OUTPUTS STATE
0	On	Drive
1	Source chopped	Slow decay with synchronous rectification
1 for >3ms typical	Off	Disable

7 Detailed Description

7.4 Feature Description (continued)

Synchronous Rectifier

When the attenuation period of PWM control (external control of ENB pin or internal fixed attenuation period) comes, the motor current circulates inside the motor and H-bridge. Synchronous rectification opens the corresponding MOS tube to short-circuit the freewheeling diode during current attenuation. Due to the low on resistance of MOS tube, this operation can greatly reduce the system power consumption.

Brake Mode

A logic low on the BRAKEZ pin activates Brake mode. A logic high allows normal operation. Braking turns on all three sink drivers, effectively shorting out the motor-generated BEMF. The BRAKEZ input overrides the ENB input and also the Lock Detect function. It is important to note that the internal PWM current control circuit does not limit the current when braking, because the current does not flow through the sense resistor. The maximum current can be approximated by dividing the reverse electromotive force V_{BEMF} by the load resistance R_{SENSE}.
Care should be taken to insure that the maximum ratings of the CJDR4398 and CJDR4939 are not exceeded in the worse case braking situation, high speed and high inertial load.

Noise Reduction Function

The SYN pin is noise reduction function pin. When SYN is suspended or connected to high level, the noise reduction mode will not be turned on. When SYN is pulled down to the ground through resistance, the noise reduction function will be turned on. The noise reduction function can help to improve the phenomenon that the motor may generate squealing at low speed.
It should be noted that the noise reduction function is applicable to motors with small inductance (less than 1mH) and average working current not exceeding 4A. It is not recommended to turn on the noise reduction function when using motors with large inductance or large working current.

HBIAS Function

This function provides a output voltage of 5.2V, current-limited to 30mA. This reference voltage is used to power the logic sections of the IC and also to power the external Hall elements.

Standby Mode

To prevent excessive power dissipation due to the current draw of the external Hall elements, Standby mode turns off the HBIAS output voltage. Standby mode is triggered by holding ENB high for longer than 3 ms. Note that Brake mode overrides Standby mode, so hold the BRAKEZ pin at high level to enter standby mode.

Charge Pump

The internal charge pump is used to generate a supply above VBB to drive the high-side MOSFETs. The voltage on the VCP pin is internally monitored, and in case of a fault condition, the outputs of the device are disabled.

Fault Shutdown

In the event of a fault due to excessive junction temperature or due to low voltage on VCP or VBB, the outputs of the device are disabled until the fault condition is removed. At power-up the UVLO circuit disables the drivers.

7 Detailed Description

7.4 Feature Description (continued)

Overvoltage Protection

VBB is monitored to determine if a hazardous voltage is present due to the motor generator pumping up the supply bus. When the voltage exceeds V_{BBOV}, the synchronous rectification feature is disabled.

Thermal Shutdown

If junction temperature exceeds approximately 170°C (typical), the thermal shutdown function will disable the outputs until the internal temperature falls below the 20°C hysteresis (typical).

Hall State Reporting

The FG1 and FG2 pins are the open drain outputs that change state at each transition of an external Hall element.

Lock Detect Function

The IC will evaluate a locked rotor condition under either of these two different conditions:

1. The FGx signal is not consistently changing;
2. The proper commutation sequence is not being followed. The motor can be locked in a condition in which it toggles between two specific Hall device states.

Both of these fault conditions are allowed to persist for period of time, t_{lock}. t_{lock} is set by capacitor connected to CLD pin. C_{LD} produces a triangle waveform (1.67V_{PP}) with frequency linearly related to the capacitor value. t_{lock} is defined as 127 cycles of this triangle waveform, or:

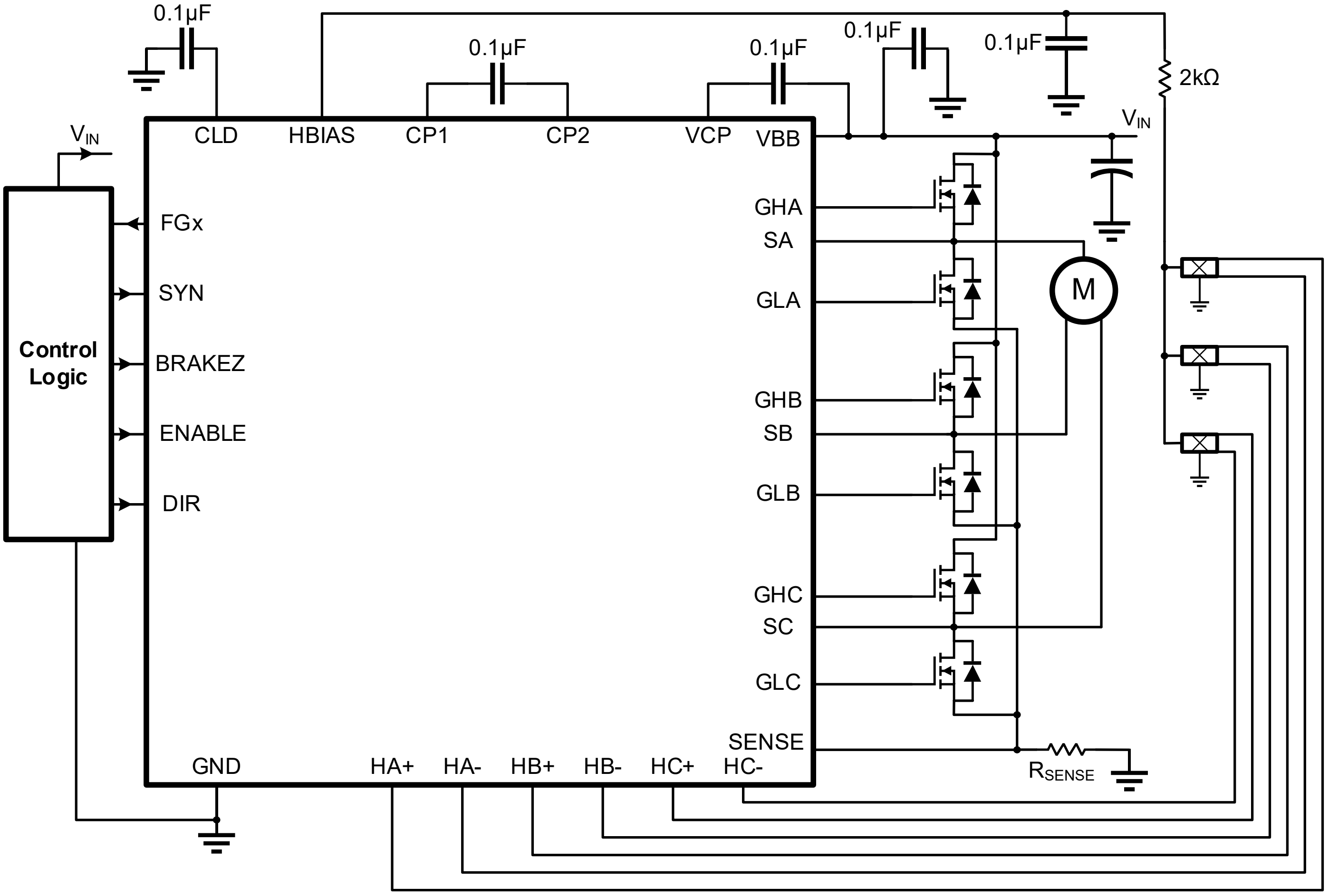
$$t_{lock} = C_{LD} \times 20\ s/\mu F$$

After the wait time, t_{lock}, has expired, the outputs are disabled, and the fault is latched. These fault conditions can only be cleared by any one of the following actions:

1. Rising or falling edge on the DIR pin;
2. $V_{BB\ UVLO}$ threshold exceeded (during power-up cycle);
3. ENB pin held high for > (t_{lock} / 2). The Lock Detect function can be disabled by connecting CLD to GND.

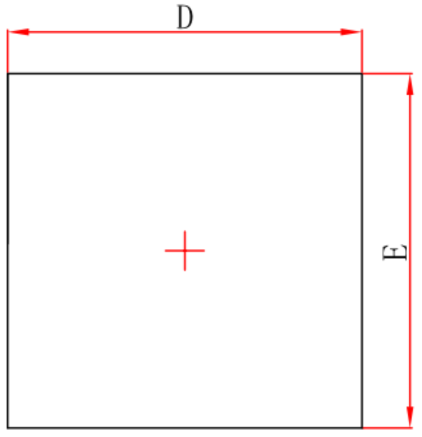
When the device is in Brake mode, the Lock Detect counter is disabled.

8 Typical Application Circuit

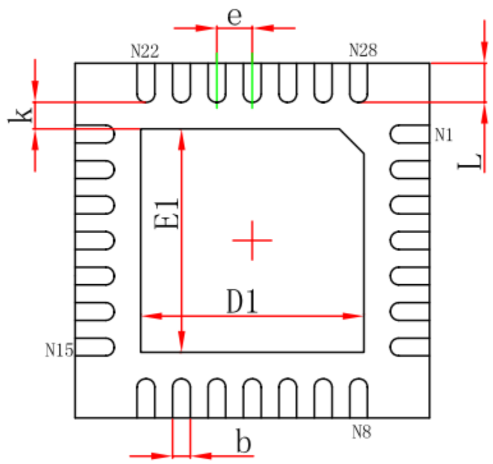


9 Mechanical Information

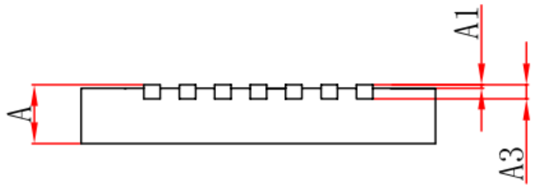
QFNWB5×5-28L Package



Top View



Bottom View



Side View

SYMBOL	DISMENSIONS IN MILLIMETERS			DISMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	-	0.900	0.028	-	0.035
A1	0.000	-	0.050	0.000	-	0.002
A3	0.203 REF.			0.008 REF.		
D	4.900	-	5.100	0.193	-	0.201
E	4.900	-	5.100	0.193	-	0.201
D1	3.050	-	3.250	0.120	-	0.128
E1	3.050	-	3.250	0.120	-	0.128
k	0.200 MIN.			0.008 MIN.		
b	0.180	-	0.300	0.007	-	0.012
e	0.500 TYP.			0.200 TYP.		
L	0.450	-	0.650	0.018	-	0.026

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, please click the official website of JSCJ -- ***https: www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

January, 2023: released CJDR4938, CJDR4939 rev - 1.0.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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