JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

Dual Channel 5V 256 u-step STM Motor Driver IC

CJDR6208 Motor Driver

1 Introduction

The CJDR6208 is a lens motor driver IC for camcorder and security-camera. This device integrates a DC motor driver for Iris which controlled by PID system, and also has two channels STM motor drivers for zoom and focus control.

2 Available Package

PART NUMBER	PACKAGE
CJDR6208	QFNWB6×6-44L

Note: For more detailed packaging information, see the part *Pin Configuration and Function*.

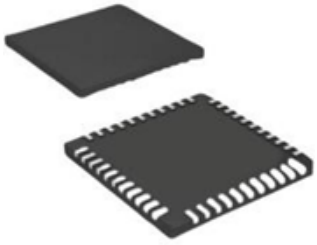


Figure 2-1. QFNWB6×6-44L Package

3 Features

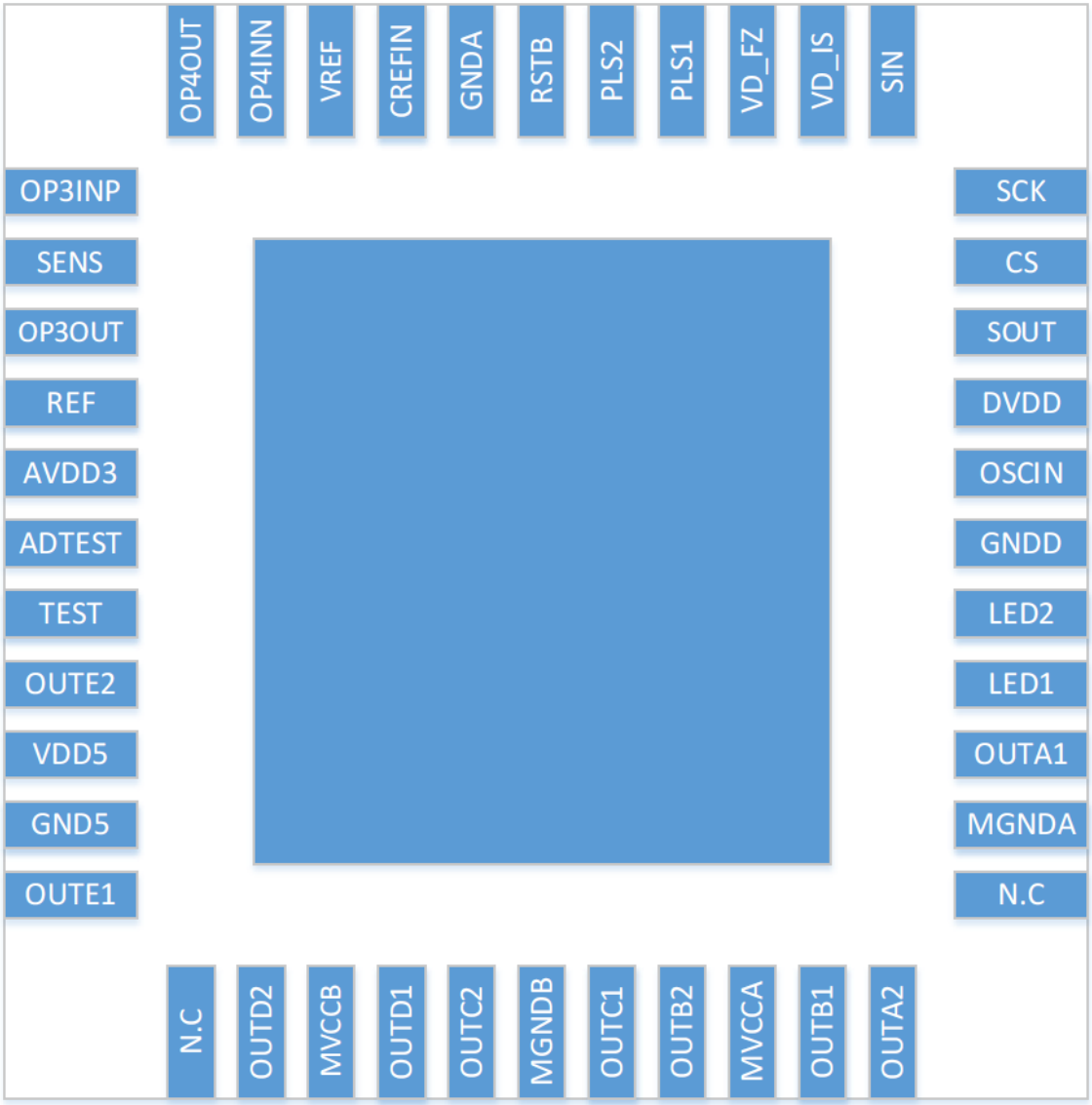
- Built in DC motor driver for Iris controller
- Built in 2 STM driver for zoom and focus
- 256 u-step driving technology for STM, features supper low noise
- 2 systems of open-drain for driving LED
- Over temperature protection
- Under voltage lockout

4 Applications

- Camcorder
- Security-camera
- Consumer Products
- Robotics
- Medical Devices

5 Pin Configuration and Function

Figure 5-1. CJDR6208 Pin Map



5 Pin Configuration and Function

PIN NAME	CJDR6208 QFNWB6×6-44L	I / O	DESCRIPTION
OP3INP	1	I	Hall signal amplifier non-inverting input.
SENS	2	O	Hall current bias.
OP3OUT	3	O	Hall signal amplifier output.
REF	4	I / O	Hall current reference setting by resistor connection.
AVDD3	5	Power	3.3V analog power.
ADTEST	6	I	ADC test input.
TEST	7	I	Test mode input.
OUTE2	8	O	Motor output E2
VDD5	9	Power	Motor power supply.
GND5	10	Ground	Motor E ground.
OUTE1	11	O	Motor output E1.
N.C	12	-	No connection inside.
OUTD2	13	O	Motor output D2.
MVCCB	14	Power	Motor B supply.
OUTD1	15	O	Motor output D1.
OUTC2	16	O	Motor output C2.
MGNDB	17	Ground	Motor B ground.
OUTC1	18	O	Motor output C1.
OUTB2	19	O	Motor output B2.
MVCCA	20	Ground	Motor A ground.
OUTB1	21	O	Motor output B1.
OUTA2	22	O	Motor output A2.

5 Pin Configuration and Function

PIN NAME	CJDR6208 QFNWB6×6-44L	I / O	DESCRIPTION
N.C	23	-	No connection inside.
MGNDA	24	Ground	Motor A ground.
OUTA1	25	O	Motor output A1.
LED1	26	O	LED1 OUT (open drain).
LED2	27	O	LED2 OUT (open drain).
GNDD	28	Ground	Ground pin for digital circuit.
OSCIN	29	I	System clock input.
DVDD	30	Power	Digital power supply.
SOUT	31	O	SPI output.
CS	32	I	SPI chip select.
SCK	33	I	SPI clock input.
SIN	34	I	SPI data in.
VD_IS	35	I	Sync signal input for Iris.
VD_FZ	36	I	Sync signal input for zoom&focus.
PLS1	37	O	Pulse 1 output.
PLS2	38	O	Pulse 2 output.
RSTB	39	I	Reset signal input.
GNDA	40	Ground	Ground pin for analog.
CREFIN	41	I / O	AVDD3/2 capacitor connection pin.
VREF	42	O	Reference voltage for Hall sense.
OP4INN	43	I	Amplifier 4 no-inverting input.
OP4OUT	44	O	Amplifier 4 output.

6 Specifications

6.1 Absolute Maximum Ratings(1)

(over operating free-air temperature range, unless otherwise specified)

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Analog supply voltage	AVDD3	-0.3 ~ 4.0	V
Digital supply voltage	DVDD	-0.3 ~ 4.0	
STM motor supply voltage	MVCCA/B	-0.3 ~ 6.0	
DC motor supply voltage	VDD5	-0.3 ~ 6.0	
STM motor current	I_{STM}	0.8	A
DC motor current	I_{DC}	0.3	
LED pull down current	LED	30	mA
Maximum junction temperature	T_J	125	°C
Storage temperature	T_{stg}	-55 ~ 125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

ESD RATINGS		SYMBOL	VALUE	UNIT
Electrostatic discharge(3)	Human body model	$V_{ESD-HBM}$	3000	V

(3) ESD testing is conducted in accordance with the relevant specifications formulated by the Joint Electronic Equipment Engineering Commission (JEDEC). The human body mode (HBM) electrostatic discharge test is based on the JESD22-114D test standard, using a 100pF capacitor and discharging to each pin of the device through a resistance of 1.5kΩ.

6 Specifications

6.3 Recommended Operating Conditions

PARAMETER	PIN	SYMBOL	MIN.	NOM.	MAX.	UNIT
Motor power supply	MVCCA, MVCCB, VDD5	-	3.0	5.0	5.5	V
Analog & logic power supply	AVDD3, DVDD	-	2.7	3.3	3.6	V
Logic input range	TEST, OSCIN, CS, SCK, SIN, VD_IS, VD_FZ, RSTB	$V_{LOGIC\ IN}$	-0.3	-	DVDD+0.3	V
Logic output range	PLS1. PLS2, SOUT	$V_{LOGIC\ OUT}$	-0.3	-	DVDD+0.3	V
Analog output range	OP3OUT, OP4OUT, SENS, VREF	$V_{Analog\ OUT}$	-0.3	-	AVDD+0.3	V
Motor current	OUTA1, OUTA2, OUTB1, OUTB2, OUTC1, OUTC2, OUTD1, OUTD2	I_{STM}	-0.25	-	0.25	A
	OUTE1, OUTE2	I_{DC}	-0.15	-	0.15	A
External constants	-	C_{VREF}	-	0.1	-	μF
		C_{REFIN}	-	0.1	-	
		C_{OP3INP}	-	0.01	-	
		C_{OP4OUT}	-	0.1	-	
		R_{REF}	-	10	-	kΩ
Operating ambient temperature	-	T_A	-40	-	100	°C

(4) It is necessary to ensure that the operating junction temperature of the device does not exceed the rated value of the recommended operating conditions when using the device for design.

6 Specifications

6.4 Electrical Characteristics

CJDR6208 (DVDD = AVDD = 3.3V, MVCC x = VDD5 = 5.0V, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.(6)	MAX.	UNIT
MVCC current on Reset	$I_{V\ RESET}$	No load, no 27MHz inputs, RSTB = 0	-	0	2.0	μA
MVCC current	$I_{VM\ ON}$	Output open	-	0.5	15	mA
DVDD, AVDD standby current	$I_{VDD\ RESET}$	No 27MHz inputs, RSTB = 1	-	0	10	μA
DVDD, AVDD current	$I_{VDD\ ON}$	No load, RSTB = 0	-	7	20	mA
VDD5 standby current	$I_{VDD5\ RESET}$	No 27MHz inputs, RSTB = 1	-	0	10	μA
VDD5 current	$I_{VDD5\ ON}$	No load, RSTB = 0	-	0.3	1.0	mA
STM OUT H-bridge Driver (Focus & Zoom)						
RDS ON, up + down4	$R_{DS\ ON\ 1}$	I_{OUT} = 100mA, T_A = 25°C	-	1.5	2.5	Ω
When off leakage current	$I_{OFF\ 1}$	V_{OUT} = 0V	-10	-	10	μA
Protection Circuits						
Thermal shutdown	T_{SD}	-	155	169	180	°C
Thermal shutdown hysteresis	ΔT_{SD}	-	-	26	-	°C
Under voltage lockout	$V_{UVLO\ 1}$	DVDD, AVDD	-	2.27	-	V
Under voltage lockout hysteresis	$\Delta V_{UVLO\ 1}$	DVDD, AVDD	-	0.2	-	V
Under voltage lockout	$V_{UVLO\ 2}$	MVCCA, MVCCB, VDD5	-	2.20	-	V
Under voltage lockout hysteresis	$\Delta V_{UVLO\ 2}$	MVCCA, MVCCB, VDD5	-	0.2	-	V

6 Specifications

6.4 Electrical Characteristics (continued)

CJDR6208 (DVDD = AVDD = 3.3V, MVCC x = VDD5 = 5.0V, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.(6)	MAX.	UNIT
Logic Inputs / Outputs						
Input logic-low voltage	V_{IL}	TEST, OSCIN, CS, SCK, SIN, VD_IS, VD_FZ, RSTB	-0.3	1.02	0.20 × DVDD	V
Input logic-high voltage	V_{IH}	TEST, OSCIN, CS, SCK, SIN, VD_IS, VD_FZ, RSTB	0.54 × DVDD	1.36	DVDD + 0.3	V
Output logic-low voltage	V_{OL}	PLS1, PLS2, SOUT, 1mA Sink	-	-	0.5	V
Output logic-high voltage	V_{OH}	PLS1, PLS2, SOUT, 1mA Source	0.9 × DVDD	-	-	V
Pulldown resistance	$R_{Pull\ Down}$	RSTB	-	100	-	kΩ
OPAMP3 (HALL Sensor Amplifier for Output Amplifier)						
Input voltage range	$V_{IN\ OP3}$	-	(0.5 × VDD) - 0.5	0.5 × VDD	(0.5 × VDD) + 0.5	V
Input offset voltage	V_{OF3}	-	-15	-	15	mV
Output voltage (low)	V_{OL3}	I_{LOAD} = -100μA	-	0.1	0.2	V
Output voltage (high)	V_{OH3}	I_{LOAD} = 100μA	AVDD - 0.2	AVDD - 0.1	-	V
Output gain voltage	V_{OG}	Gain register set value: 0h	19.7	21.9	24.1	V / V
OP4AMP4 (HALL Sensor Amplifier for Eliminating Common-mode Voltage)						
Input voltage range	$V_{IN\ OP4}$	-	(0.5 × AVDD) - 0.1	0.5 × VDD	(0.5 × VDD) + 0.1	V
Input offset voltage	V_{OF4}	-	-10	-	10	mV
Output voltage (low)	V_{OL4}	I_{LOAD} = -100μA	-	0.1	0.2	V
Output voltage (high)	V_{OH4}	I_{LOAD} = 100μA	AVDD - 0.5	AVDD - 0.2	-	V

6 Specifications

6.4 Electrical Characteristics (continued)

CJDR6208 (DVDD = AVDD = 3.3V, MVCC x = VDD5 = 5.0V, T_A = 25°C, unless otherwise specified)

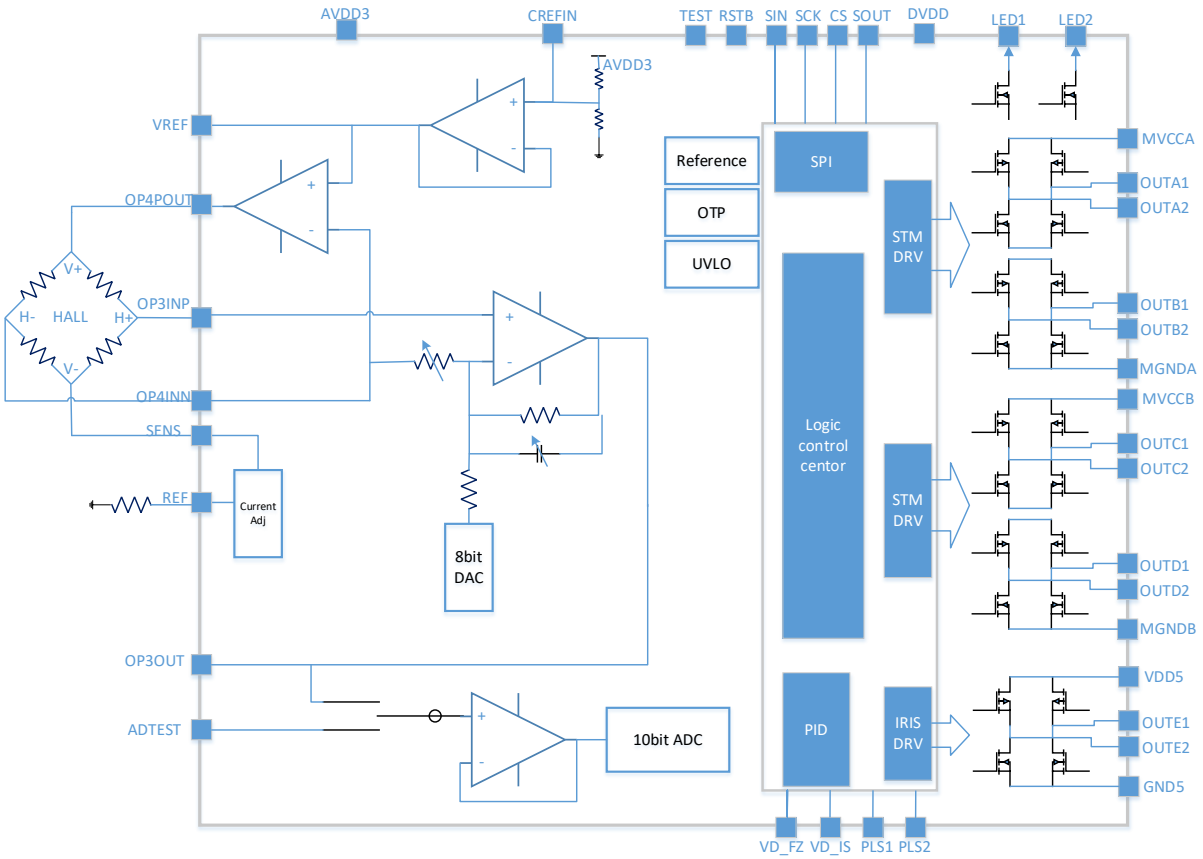
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.(6)	MAX.	UNIT
DC OUT H-bridge driver (Iris)						
RDS ON, up + down	$R_{DS\ ON\ 2}$	I_{OUT} = 100mA, T_A = 25°C	-	2.0	3.0	Ω
When off leakage current	$I_{OFF\ 2}$	V_{OUT} = 0V	-10	-	10	μA
LED Drivers						
Output on resistance	$R_{DS\ ON\ 3}$	-	-	-	5	Ω
When off leakage current	$I_{OFF\ 2}$	-	-10	-	10	μA
Reference Output						
Output voltage 1	V_{REF}	V_{CREF} = 100pF, I_{LOAD} = 0A	(0.5 × AVDD) - 0.1	0.5 × VDD	(0.5 × VDD) + 0.1	V
Output voltage 1 Load	V_{REFL}	VCREF = 100pF, ILOAD = 100μA	V_{REF} - 0.1	V_{REF}	V_{REF} + 0.1	V
Hall Bias Controller (SENS Output)						
Minutes output current	IB_L	R_{REF} = 10kΩ, SENS = 0.7V, set value: 00h	-	0	0.1	mA
Output current accuracy 1	IB_{40H}	R_{REF} = 10kΩ, SENS = 0.7V, set value: 01h	0.90	1.02	1.14	mA
Output current accuracy2	IB_{BEH}	REF=10kΩ，SENS=0.7V，set value: Beh	2.66	3.02	3.38	mA
8bit DAC for Hall Offset Adjustment						
Adjustment range high	DAOUT H	-	-	AVDD3	-	V
Adjustment range low	DAOUT L	-	-	0	-	V

7 Detailed Description

7.1 Description

The CJDR6208 is a lens motor driver IC for camcorder and security-camera. This device integrates a DC motor driver for Iris which controlled by PID system, and also has two channels STM motor drivers for zoom and focus control.

7.2 Functional Block Diagram

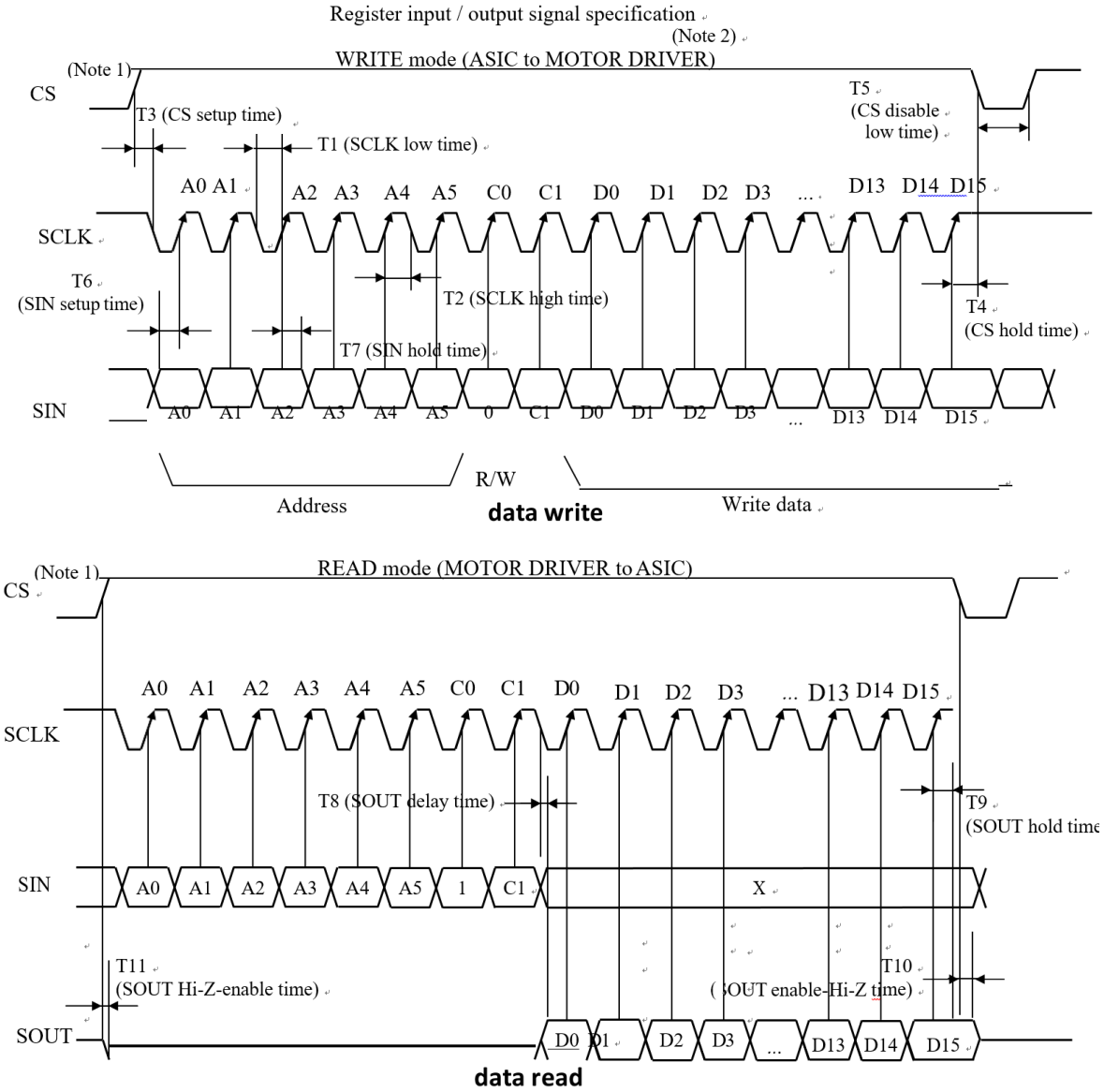


7 Detailed Description

7.3 Function Description

Serial Interface

Timing Chart



7 Detailed Description

7.3 Function Description (continued)

VCC = 5.0V, RL = 20Ω, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITION	RANGE		UNIT
		MIN.	MAX.	
SPI Speed	Serial clock	1	5	MHz
T1	SCLK low time	100	-	ns
T2	SCLK high time	100	-	ns
T3	CS setup time	60	-	ns
T4	CS hold time	60	-	ns
T5	CS disable low time	100	-	ns
T6	SIN setup time	50	-	ns
T7	SIN HOLD time	50	-	ns
T8	SOUT delay time	-	60	μs
T9	SOUT hold time	60	-	ns
T10	SOUT enable-Hiz time	-	60	ns
T11	SOUT Hiz-enable time	-	60	ns
Cload	SOUT Capacitor load	-	40	pF

7 Detailed Description

7.3 Function Description (continued)

Register Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00H							IRS_TGT[9:0]									
01H	DGAIN[6:0]							ASOUNDLPF_FC[2:0]			AS_FLT_OFF	DEC_AVE	OVER_LPF_FC_2ND[1:0]		OVER_LPF_FC_1ST[1:0]	
02H	PID_POLE[3:0]				PID_ZERO[3:0]				IRIS_ROUND[3:0]				IRIS_CALC_NR[3:0]			
03H			DT_ADJ_IRIS[1:0]		PWM_IRIS[2:0]			PWM_LPF_FC[2:0]			PWM_FLTOFF	LMT_ENB	ARW[3:0]			
04H	HALL_OFFSET_DAC[7:0]								HALL_BIAS_DAC[7:0]							
05H				AAF_FC	HALL_GAIN[3:0]						PID_INV	TGT_FLT_OFF	TGT_LPF_FC[3:0]			
06H							START1[9:0]									
07H	P1EN				WIDTH1[11:0]											
08H							START2[9:0]									
09H	P2EN										WIDTH2[5:0]					
0AH						DUTY_TEST	TGT_IN_TEST[9:0]									
0BH	PID_CLIP[3:0]				ADC_TEST	PDWNB	MODESEL_FZ	MODESEL_IRIS	TESTEN1			ASWMODE[1:0]				
0CH							IRSAD[9:0] (Read Only)									
0EH				AVE_SPEED[4:0]					TGT_UPDATE[7:0]							
20H		PWMRES[1:0]		PWMMODE[4:0]					DT1[7:0]							
21H									TESTEN2			FZTEST[4:0]				
22H			PHMODAB[5:0]						DT2A[7:0]							
23H	PPWB[7:0]								PPWA[7:0]							
24H			MICROAB[1:0]		LEDB	ENDISAB	BRAKEAB	CCWCWAB	PSUMAB[7:0]							
25H	INTCTAB[15:0]															
27H			PHMODCD[5:0]						DT2B[7:0]							
28H	PPWD[7:0]								PPWC[7:0]							
29H			MICROCD[1:0]		LEDA	ENDISCD	BRAKECD	CCWCWCD	PSUMCD[7:0]							
2AH	INTCTCD[15:0]															

7 Detailed Description

7.3 Function Description (continued)

Register Description

ADDRESS	REGISTER	FUNCTION
00h	IRS_TGT [9:0]	Iris target position. Expressed in 10 bit digits.
01h	OVER_LRF_FC_1ST [1:0]	ADC feedback filter (1) cut-off frequency.
	OVER_LRF_FC_2ND [1:0]	ADC feedback filter (2) cut-off frequency.
	DEC_AVE	Moving average to Iris target position.
	AS_FLT_OFF	Filter before PID controller enable / disable
	ASOUND_LPF_FC [2:0]	Filter cut-off frequency before PID controller.
	DGAIN [6:0]	PID controller digital gain.
02h	IRIS_CALS_NR [3:0]	PID integral error cumulative prevention level.
	IRIS_ROUND [3:0]	PID differential error cumulative prevention level.
	PID_ZERO [3:0]	PID controller zero point.
	PID_POLE [3:0]	PID controller pole.
03h	ARW [3:0]	Number of bits in PID controller integrator.
	LMT_ENB	PID controller integral stop.
	PWM_FLT_OFF	LPF after PID controller enable / disable.
	PWM_LPF_FC [2:0]	LPF cut-off frequency after PID controller.
	PWM_IRIS [2:0]	PWM frequency of Iris block output.
	DT_ADJ_IRIS [1:0]	Dead time correction of Iris block output.
04h	HALL_BIAS_DAC [7:0]	Drive current value for hall element.
	HALL_OFFSET_DAC [7:0]	Offset adjustment for hall element output amplifier.
05h	TGT_LPF_FC [3:0]	Iris target value LPF cut-off frequency.
	TGT_FLT_OFF	Iris target value LPF function enable / disable.
	PID_INV	PID controller polarity.
	HALL_GAIN [3:0]	Hall element output amplifier gain.
	AAF_FC	Cut-off frequency of hall element output amplifier.
06h	START1 [9:0]	Pulse 1 start time.
07h	WIDTH1 [11:0]	Pulse 1 width.
	P1EN	Pulse 1 output enable.
08h	START2 [9:0]	Pulse 2 start time.
09h	WIDTH2 [5:0]	Pulse 2 width.
	P2EN	Pulse 2 output enable.
0Ah	TGT_IN_TEST [9:0]	Iris output duty direct specified value.
	DUTY_TEST	Iris output duty direct specification enable.

7 Detailed Description

7.3 Function Description (continued)

Register Description (continued)

ADDRESS	REGISTER	FUNCTION
0Bh	ASWMODE [1:0]	ADTESTIN pin connection selection.
	TESTEN1	Test mode enable 1.
	MODESEL_IRIS	VD_IS polarity selection.
	MODESEL_FZ	VD_FZ polarity selection.
	PDWNB	Power down of Iris block.
	ADC_TEST	ADC read value updated timing.
	PID_CLIP [3:0]	Iris output PWM maximum duty.
0Ch	IRSAD [9:0]	ADC output for Iris (read only).
0Eh	TGT_UPDATE [7:0]	IRS_TGT (iris target) update delay time.
	AVE_SPEED [4:0]	Iris target moving average speed.
20h	DT1 [7:0]	Start point wait time.
	PWMMODE [4:0]	Micro step output PWM frequency.
	PWMRES [1:0]	Micro step output PWM resolution.
21h	FZTEST [4:0]	PLS1/2 pin output signal selection.
	TESTEN2	Test mode enable 2.
22h	DT2A [7:0]	α motor start point excitation wait time.
	PHMODAB [5:0]	α motor phase correction.
23h	PPWA [7:0]	Driver A peak pulse width.
	PPWB [7:0]	Driver B peak pulse width.
24h	PSUMAB [7:0]	α motor step count number.
	CCWCWAB	α motor rotation direction.
	BRAKEAB	α motor brake.
	ENDISAB	α motor enable/disable control.
	LEDB	LED B output control.
	MICROAB [1:0]	α motor sine wave division number.
25h	INTCTAB [15:0]	α motor step cycle.
27h	DT2B [7:0]	β motor start point excitation wait time.
	PHMODCD [5:0]	β motor phase correction.
28h	PPWC [7:0]	Driver C peak pulse width.
	PPWD [7:0]	Driver D peak pulse width.

7 Detailed Description

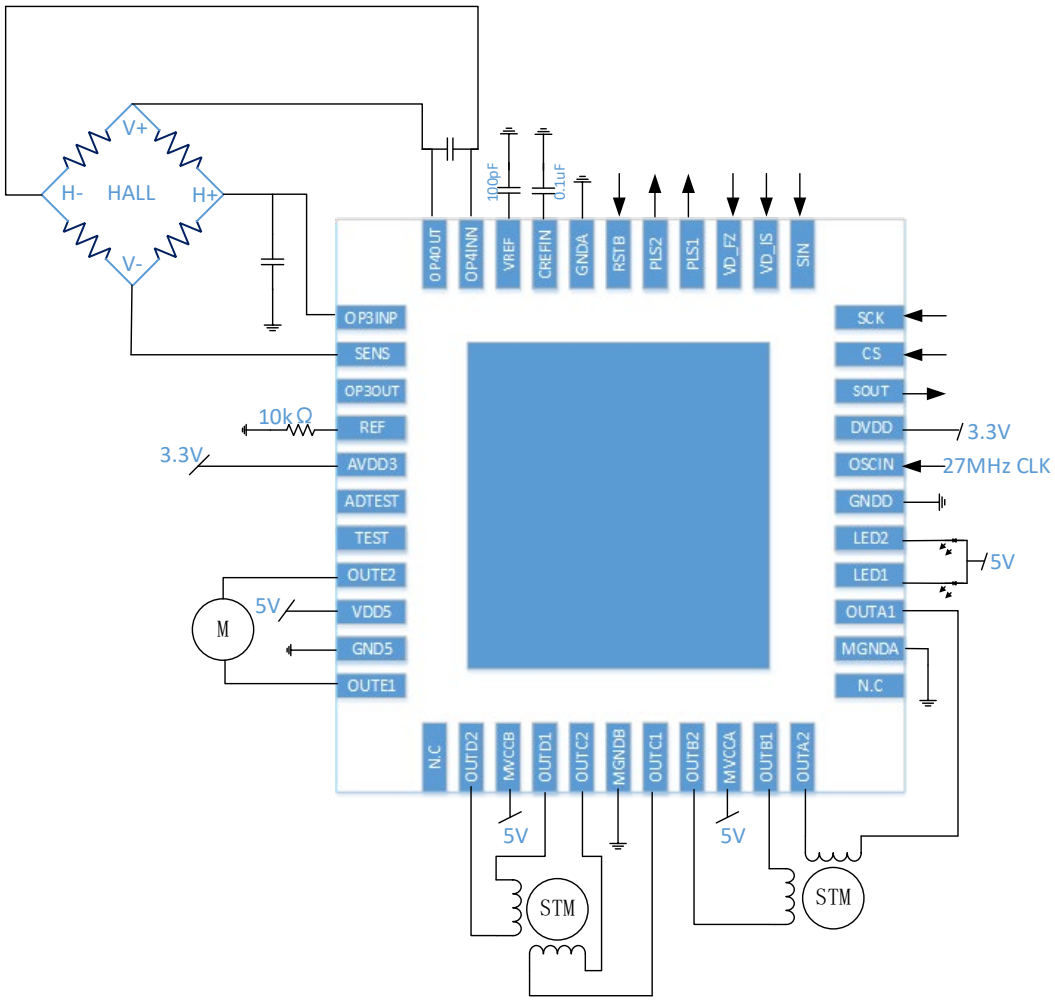
7.3 Function Description (continued)

Register Description (continued)

ADDRESS	REGISTER	FUNCTION
29h	PSUMCD [7:0]	β motor step count number.
	CCWCWCD	β motor rotation direction.
	BRAKECD	β motor brake.
	ENDISCD	β motor enable/disable control.
	LEDA	LED A output control.
	MICROCD [1:0]	β motor sine wave division number.
2Ah	INTCTCD [15:0]	β motor step cycle.

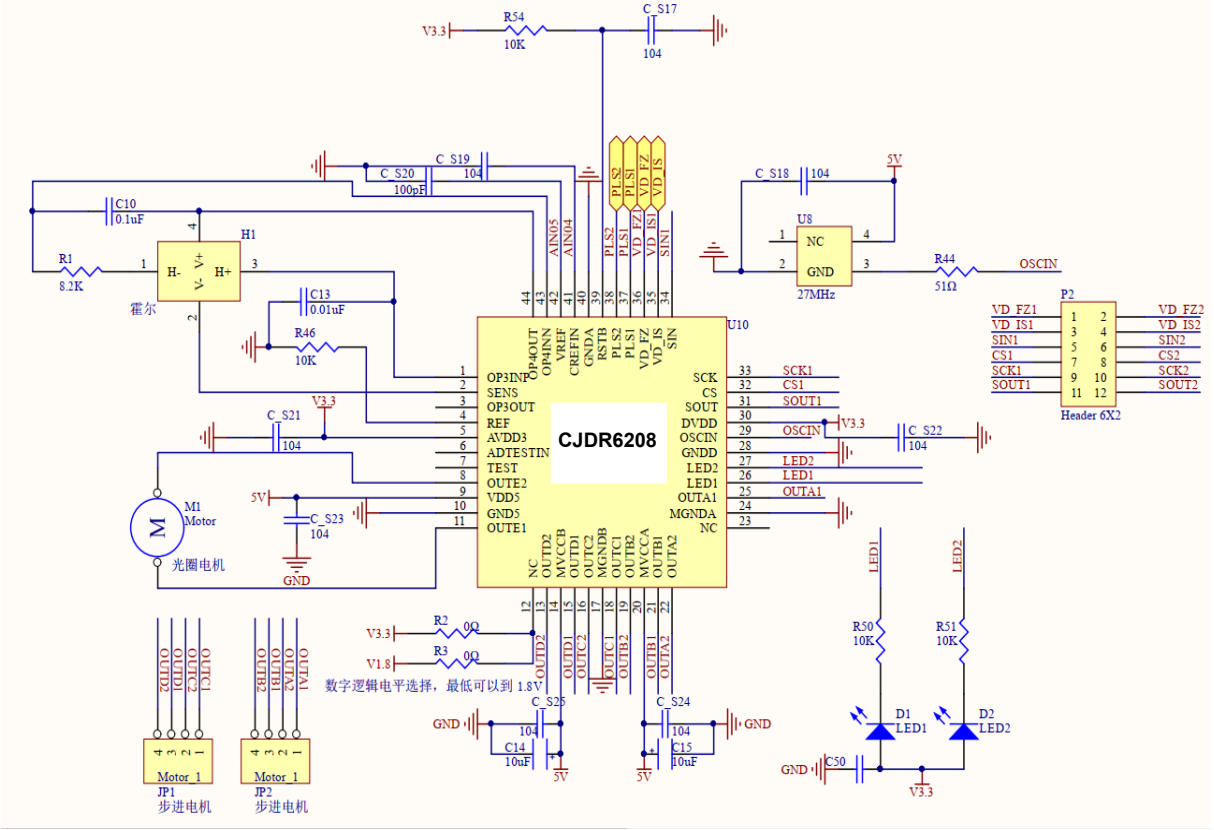
8 Application Information

8.1 Typical Application Circuit



8 Application Information

8.2 PCB Schematic

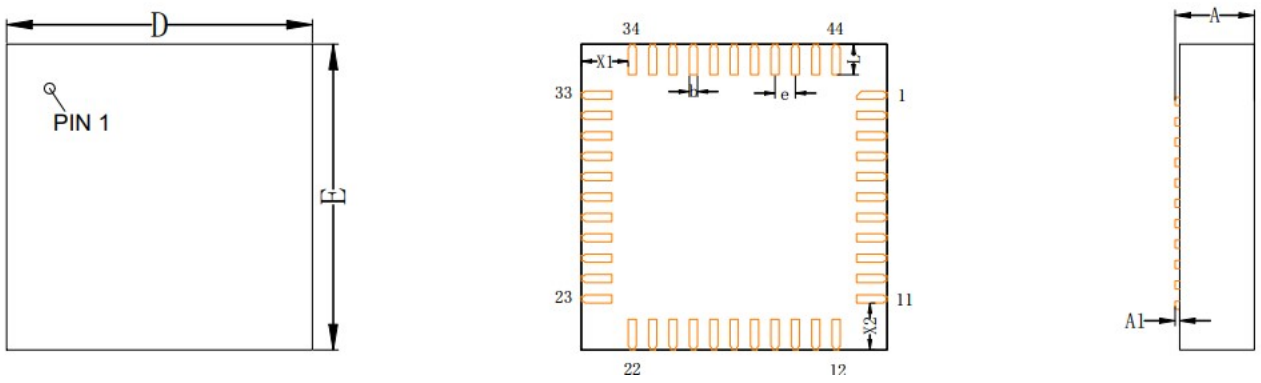


9 Mechanical Information

QFNWB6×6-44L Mechanical Information

Package Information (Unit: mm)

Top View **Bottom View** **Side View**



SYMBOL	DISMENSIONS IN MILLIMETERS			DISMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.007	0.012	0.017	0.000	0.000	0.001
D	5.900	6.000	6.100	0.232	0.236	0.240
E	5.900	6.000	6.100	0.232	0.236	0.240
L	0.550	0.600	0.650	0.022	0.024	0.026
b	0.110	0.160	0.210	0.004	0.006	0.008
e	0.350	0.400	0.450	0.014	0.016	0.018
X1	0.870	0.920	0.970	0.034	0.036	0.038
X2	0.870	0.920	0.970	0.034	0.036	0.038

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- https: ***www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

September, 2023: released CJDR6208 rev - 1.0.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

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Official Website: www.jscj-elec.com