JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

12V Single Channel Full Bridge Motor Driver

CJDR8838 Motor Driver

1 Introduction

CJDR8838 is a 12V, DC, full bridge motor driven IC. It supports 12V power input voltage and can provide continuous output current up to 1.5A. In sleep mode, its power consumption current is less than 1μA. In addition, CJDR8838 also integrates functions such as thermal shutdown, undervoltage protection, output short circuit protection and over-current protection. CJDR8838 has PWM (PH / EN) input interface and is compatible with industry standard equipment. Therefore, CJDR8838 is very suitable for providing integrated motor drive solutions for cameras, consumer goods, toys and other low-voltage or battery powered motion control applications.

2 Available Package

PART NUMBER	PACKAGE
CJDR8838	DFNWB2×2-8L

Note: For more detailed packaging information, see the part *Pin Configuration and Function* and the part *Mechanical Information*.

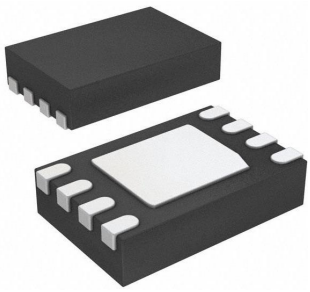


Figure 2-1. DFN2×2-8L Package

3 Features

- H-bridge Motor Driver
- Load Power Supply Voltage: 0 ~ 12V
- Low Conducting Internal Resistance: 350mΩ (Typ., HS + LS)
- Drive Output Current: 1.5A (Continuous)
- PWM (PH / EN) Input Mode
- Compatible with 3.3V, 5.0V Logic Input
- Thermal Shutdown Protection
- Build-in Output Current Limit
- Short Circuit Protection
- Under-voltage Protection
- Low Consumption Current in Sleep Mode: nA level (when nSleep = 0)

4 Applications

- Video Camera
- Digital Single Lens Reflective Lens
- Toys
- Robotics
- Shared Bicycle Lock
- Water Meter Switch
- Medical Equipment

5 Pin Configuration and Function

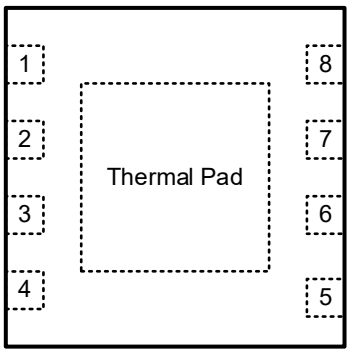


Figure 5-1. Package Pin Map

PIN NAME	CJDR8838 DFNWB2×2-8L	I / O	DESCRIPTION
V_M	1	Power	Load power supply.
OUT 1	2	O	H-bridge output 1.
OUT 2	3	O	H-bridge output 2.
GND	4	Ground	Device ground. Connect to system ground.
EN	5	I	Enable control pin. See Table 7-1 for detailed functions.
PH	6	I	Phase control pin. See Table 7-1 for detailed functions.
nSleep	7	I	Sleep mode control input, active at low level.
V_{CC}	8	Power	Logic power supply.
-	Thermal Pad	-	Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings(1)

(over operating free-air temperature range, unless otherwise specified)

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Load power input voltage range(2)	V_M	0 ~ 16	V
Logic power input voltage range(2)	V_{CC}	-0.3 ~ 7.0	
Logic input voltage range(2)	$V_{IN\ x}$	-0.5 ~ 7.0	
Continuous output current	I_{OUT}	±1.5	A
Peak output current	$I_{OUT\ Max}$	±2.5	
Maximum junction temperature	T_J	150	°C
Storage temperature	T_{stg}	-60 ~ 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

6.2 Recommended Operating Conditions(3)

PARAMETER	SYMBOL	MIN.	NOM.	MAX.	UNIT
Load power input voltage range	V_M	0	-	12	V
Logic power input voltage range	V_{CC}	2.0	-	7.0	V
Continuous output current	I_{OUT}	0	-	1.5	A
External PWM frequency	f_{PWM}	0	-	400	kHz
Operating junction temperature	T_J	-40	-	150	°C
Operating ambient temperature(4)	T_A	-40	-	85	°C

(3) JSCJ recommends that users should not exceed the rated value in the *Recommended Operating Conditions* for the application conditions of the equipment, so as to ensure the stability of normal operation and reliability of long-term operation of the equipment. Operation beyond the recommended rated conditions does not mean that the product will fail. The consumers need to evaluate the risks that may be caused by the operation of the product beyond the recommended rated conditions.

(4) It is necessary to ensure that the operating junction temperature of the equipment does not exceed the rated value of th recommended operating conditions when using the device for design.

6 Specifications

6.3 ESD Ratings

ESD RATINGS		SYMBOL	VALUE	UNIT
Electrostatic discharge(5)	Human body model	$V_{ESD-HBM}$	5000	V

(5) ESD testing is conducted in accordance with the relevant specifications formulated by the Joint Electronic Equipment Engineering Commission (JEDEC). The human body model (HBM) electrostatic discharge test is based on the JESD22-114D test standard, using a 100pF capacitor and discharging to each pin of the device through a resistance of 1.5kΩ.

6.4 Electrical Characteristics

CJDR8838 (V_{CC} = 3.0V, V_M = 12V, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.(6)	MAX.	UNIT
Power Supply						
V_{CC} working current	I_{Vcc}	V_{CC} = 3.0V, no PWM input	-	450	600	μA
		V_{CC} = 3.0V, f_{PWM} = 50kHz	-	700	1500	
V_{CC} standby current	$I_{Vcc\ Q}$	nSleep = 0	-	300	500	nA
V_M working current	I_{VM}	V_{CC} = 3.0V, no PWM input	-	200	550	μA
		V_{CC} = 3.0V, f_{PWM} = 50kHz	-	580	900	
V_M standby current	$I_{VM\ Q}$	nSleep = 0	-	200	300	nA
Output H-bridge						
High side + low side bridge conduction resistance	$R_{DS\ ON}$	I_{OUT} = 500mA, T_J = 25°C	-	350	450	mΩ
		I_{OUT} = 500mA, T_J = 125°C	-	530	700	
Off-state leakage current	I_{OFF}	V_{OUT} = 0V	-10	-	10	μA
Logic Input Pin (IN 1, IN 2, nSleep)						
Logic input low voltage	V_{IL}	High level to low level	-	-	1.30	V
Logic input high voltage	V_{IH}	Low level to high level	1.60	-	-	V
Logic input hysteresis	V_{IHY}	V_{IN} = 3.3V	-	0.3	-	V
Logic input low current	I_{IL}	V_{IN} = 0V	-5	-	5	μA
Logic input high current	I_{IH}	V_{IN} = 3.3V	-	30	-	μA
nSleep low	V_{nSL}	High level to low level	-	-	1.30	V
nSleep high	V_{nSH}	Low level to high level	1.60	-	-	V
nSleep hysteresis	V_{nSHY}	V_{IN} = 3.3V	-	0.3	-	V
nSleep high current	I_{nSH}	V_{IN} = 3.3V	-	100	-	μA
Pull down resistance	R_{PD}	IN x pins	-	100	-	kΩ
		nSleep pin	-	50	-	kΩ

6 Specifications

6.4 Electrical Characteristics (continuned)

CJDR8838 (V_{CC} = 3.0V, V_M = 12V, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.(6)	MAX.	UNIT
Protection Circuits						
Thermal shutdown temperature	T_{SD}	-	155	170	180	°C
Thermal shutdown hysteresis	ΔT_{SD}	-	-	25	-	°C
Undervoltage protection voltage	V_{UVLO}	V_{CC} power supply	-	1.8	-	V
Undervoltage protection hysteresis	ΔV_{UVLO}	V_{CC} power supply	-	0.2	-	V
Output current limit	$I_{OUT\ Limit}$	High side, peak current	-	3.0	-	A
		Low side, peak current	-	3.0	-	
OCP delay time	t_D	-	-	1.5	-	μs
OCP release time	t_R	-	-	1.5		ms

6.5 Time Series Parameters and Curves

CJDR8838 (V_{CC} = 5.0V, R_L = 20Ω, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.(6)	MAX.	UNIT
Phase conversion time	T1	PH high to OUT 1 low	-	-	160	ns
	T2	PH high to OUT 2 high	-	-	200	ns
	T3	PH low to OUT 1 high	-	-	200	ns
	T4	PH low to OUT 2 low	-	-	160	ns
Enable conversion time	T5	EN high to OUT x high	-	-	200	ns
	T6	EN low to OUT x low	-	-	160	ns
OUT x rising	T7	20% to 80%	-	-	200	ns
OUT x falling	T8	80% to 20%	-	-	200	ns
nSleep wake-up time	-	nSleep high to OUT x high	-	-	30	μs

Note:

(6) Typical numbers are at 25°C and represent the most likely norm.

6 Specifications

6.5 Time Series Parameters and Curves (continued)

CJDR8838 (V_{CC} = 5.0V, R_L = 20Ω, T_A = 25°C, unless otherwise specified)

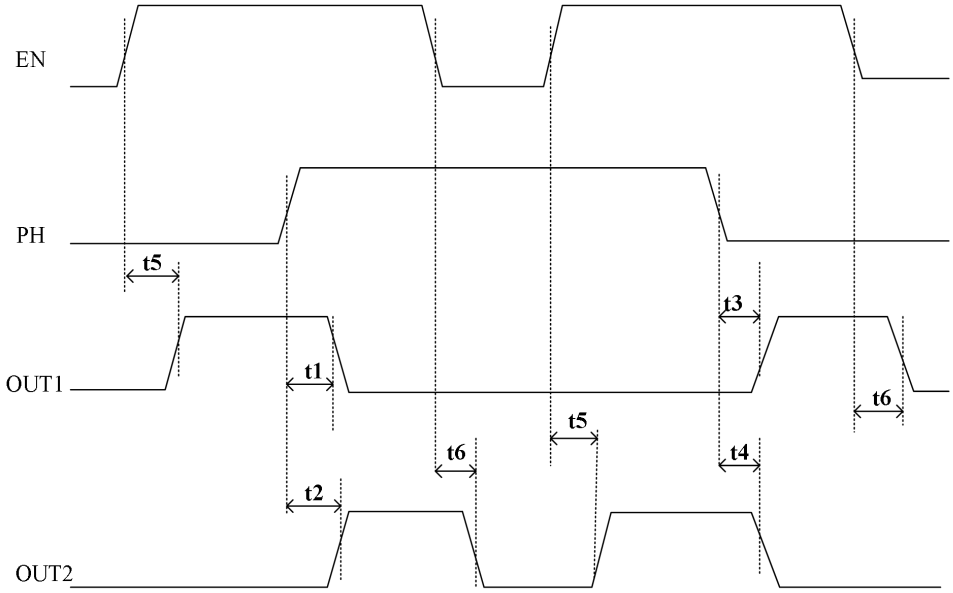


Figure 6-1. Input and Output Parameter Curve 1
(T1, T2, T3, T4, T5, T6)

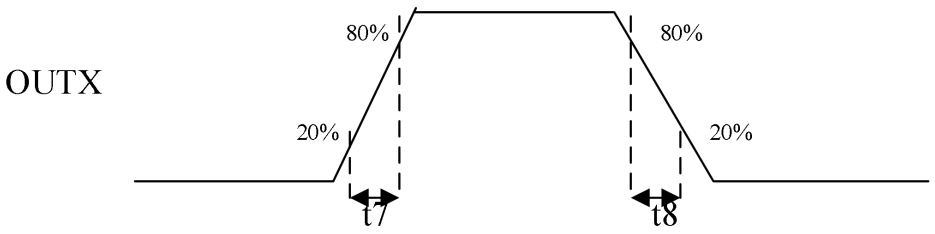


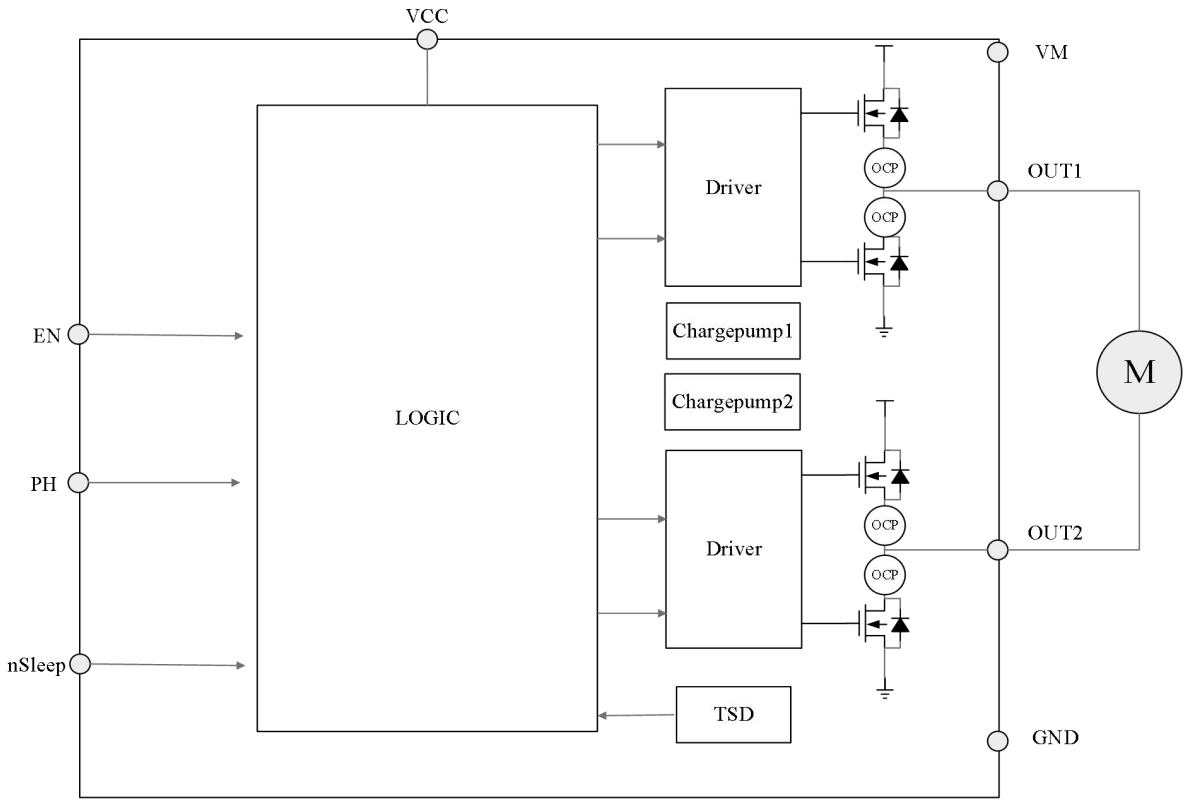
Figure 6-2. Input and Output Parameter Curve 2
(T7, T8)

7 Detailed Description

7.1 Description

CJDR8838 is a 12V DC motor drive integrated circuit, which integrates thermal shutdown, under-voltage protection, output short circuit protection and current limit protection mechanism. It is compatible with industry standard devices and has PWM (PH / EN) interface. A single CJDR8838 can be used as the DC motor drive, or two CJDR8838 can be used as the stepping motor drive.

7.2 Functional Block Diagram



7 Detailed Description

7.3 Feature Description

PWM Control Mode

CJDR8838 is controlled by PWM input interface, also known as PH / EN input mode, the PWM interface (PH / EN) controls the OUT x pins according to the logic table in Table 7-1.

Table 7-1. PWM Control Mode with Automatic Sleep

nSleep	EN	PH	OUT 1	OUT 2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode
1	0	X	L	L	Brake (low-side slow decay)
	1	0	H	L	Forward (OUT 1 → OUT 2)
		1	L	H	Reverse (OUT 2 → OUT 1)

Output Driver

Power NMOS is used for the high side and low side of output drive, and charge pump circuit is built in. The sum of internal resistances of the high side and low side is as low as 350mΩ (typical).

Sleep Mode

When nSleep is high, the device will work normally.
When nSleep is low, the device will enter the sleep mode of low power consumption. In the sleep mode, the power consumption current of the device is at the level of nA, which is suitable for application in systems requiring low power consumption.
The built-in 50kΩ resistor of nSleep is pulled down to GND. When the external input is suspended, it defaults to sleep mode.

Input Pin

There is a 100kΩ (Typ.) resistance pull-down inside the input pin, the default is low-level input.

Thermal Shutdown Protection

When the chip junction temperature exceeds 170°C (Typ.), the thermal shutdown protection circuit is activated and all output tubes are turned off. When the temperature decreases by a hysteresis temperature of 25°C (Typ.), the output tube returns to work.
Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7 Detailed Description

7.3 Feature Description (continued)

Built-in Output Current Limit

Each drive MOS of the H-bridge in CJDR8838 has a built-in current limiting mechanism. When it is detected that the current of any drive MOS exceeds the output current limit $I_{OUT\ Limit}$ in the data sheet and the duration exceeds the delay time T_D, all drive MOS will be closed. After the retry time T_R, the drive tube will automatically attempt to resume normal operation. At this time, if the output current still exceeds the rated range, the device will enter the current limit state again and turn off the output. Therefore, when the device enters the output current limit state because the output current exceeds the rated range, the device will continue the process of "Detection - Shutdown - Release - Detection" until the output current no longer exceeds its rated range. Typical values of output current limit $I_{OUT\ Limit}$, delay time T_D and retry time T_R can be found in *Electrical Characteristics*.

Short Circuit Protection

CJDR8838 has short circuit protection mechanism. When OUT x is short circuited to GND (for example, when the high side of OUT 1 is conductive, OUT 1 is abnormally short circuited to GND), or when OUT x is short circuited to V_M (for example, when the lower side of OUT 1 is conductive, OUT 1 is abnormally short circuited to V_M), the device will turn off the output of all drive MOS to protect the device from being burnt due to large current. The action mechanism of short-circuit protection is the same as that of current limit. See *Build-in Output Current Limit* for more details.

Under-voltage Locking

When the chip power supply voltage is lower than 1.98 (Typ.), the internal detection circuit will turn off the H-bridge output. If the voltage recovers, when the rising hysteresis voltage exceeds 0.2V (Typ.), the output turns on again.

Operation Mode

When nSleep is low level, CJDR8838 enters sleep mode. In sleep mode, all H-bridges are disconnected and output a high resistance state. Most circuits of the chip circuit have been turned off and entered the power saving mode. When nSleep is at high level, the chip will automatically return to the normal operation mode.

Table 7-2. Operation Mode

MODE	CONDITION	H-BRIDGE
Work	nSleep = H	Normal
Sleep mode	nSleep = L	Off
Failure detection	Under-voltage protection	Shutdown
	Thermal shutdown	
	Current limit	Detection - Shutdown - Release - Detection
	Short circuit protection	

8 Application and Implementation

8.1 Typical Application Circuit

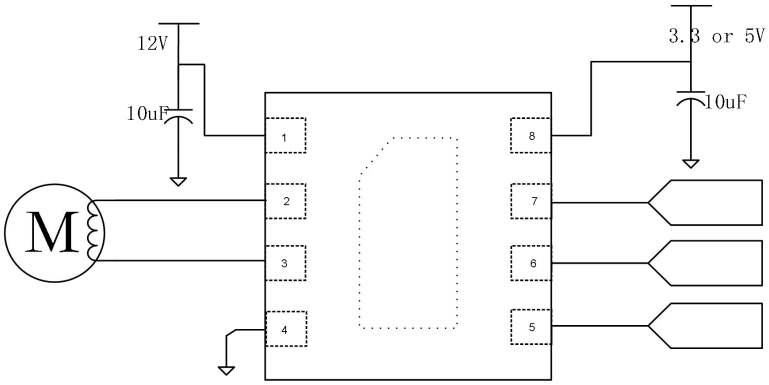


Figure 8-1. Driving DC Motor

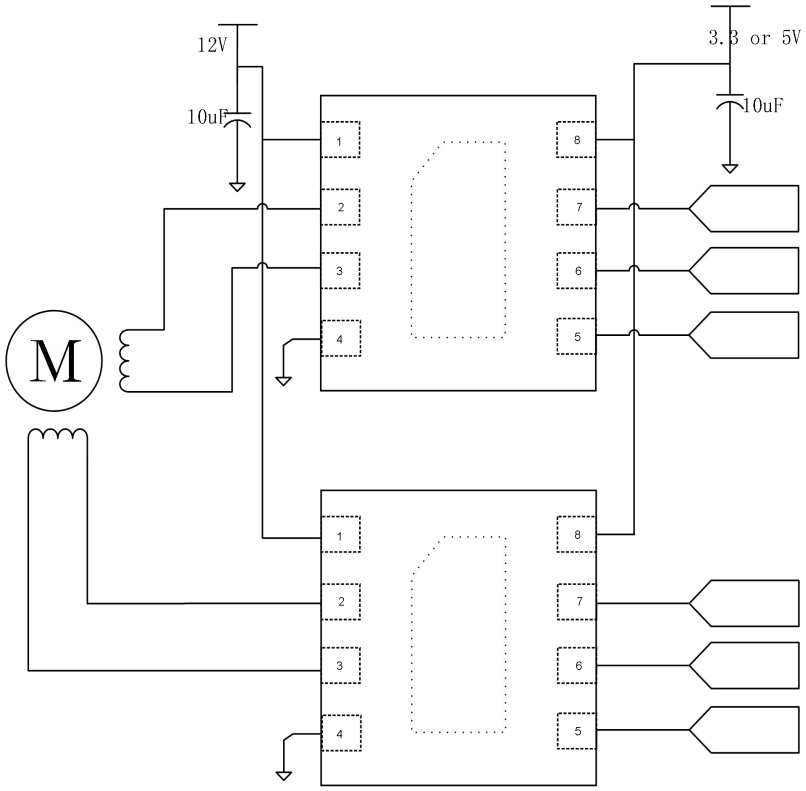


Figure 8-2. Driving Stepper Motor

8.2 Application Information

The bypass capacitor connection of V_{CC} and V_M should be as close as possible to the chip V_{CC} and V_M pin. When the load power supply exceeds 12V, it is recommended to increase the bypass capacitance of V_M to be greater than 56μF. The ground wire connecting the motor needs to be isolated in layout design.

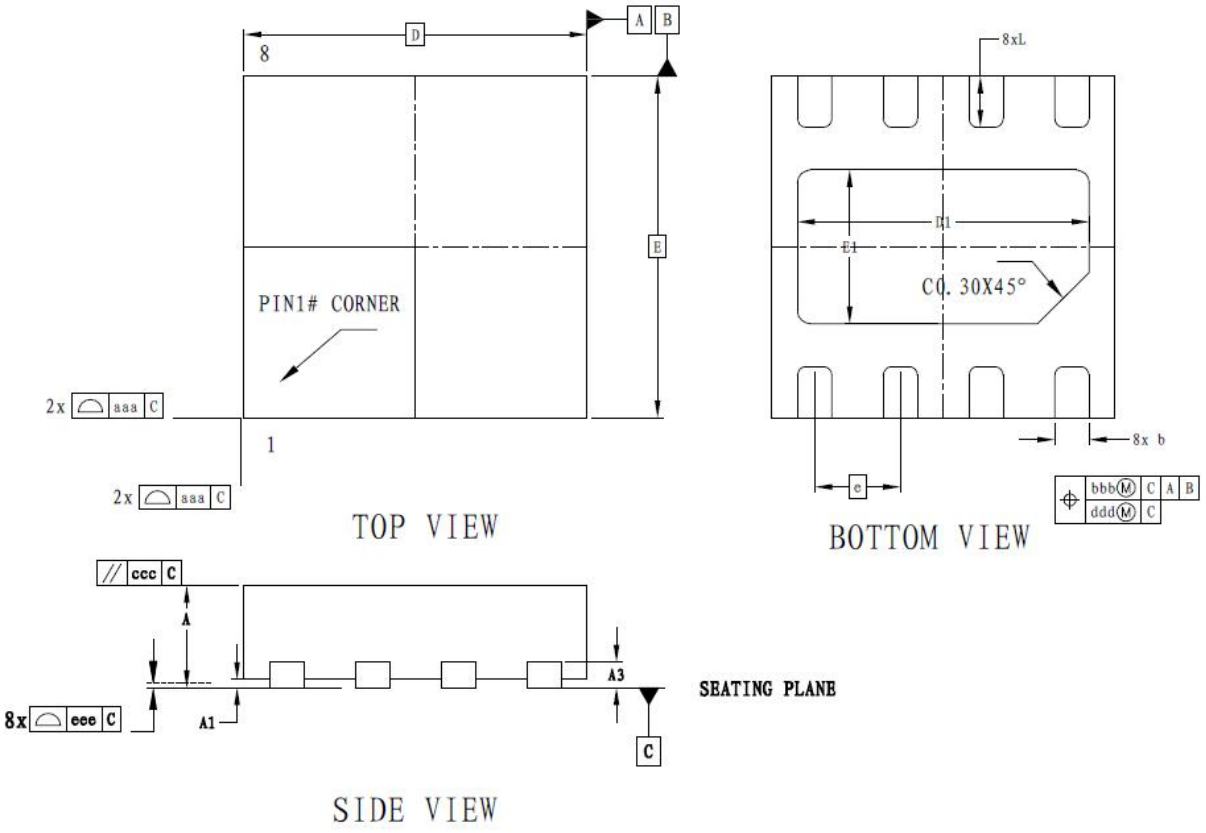
NOTE

The application information in this section is not part of the data sheet component specification, and JSCJ makes no commitment or statement to guarantee its accuracy or completeness. Customers are responsible for determining the rationality of corresponding components in their circuit design and making tests and verifications to ensure the normal realization of their circuit design.

9 Mechanical Information

DFNWB2×2-8L Mechanical Information

DFNWB2×2-8L Outline Dimensions (Unit: mm)



SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.500	0.550	0.600	0.020	0.022	0.024
A1	0.000	0.020	0.050	0.000	0.001	0.002
A3	0.152 REF			0.006 REF		
D	1.924	2.000	2.076	0.076	0.079	0.082
E	1.924	2.000	2.076	0.076	0.079	0.082
D1	1.600	1.700	1.800	0.063	0.067	0.071
E1	0.800	0.900	1.000	0.031	0.035	0.039
b	0.150	0.200	0.250	0.006	0.008	0.010
e	0.500 TYP			0.020 TYP		
L	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.150			0.006		
bbb	0.100			0.004		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- https: ***www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

October, 2022: released CJDR8838 rev - 1.0.

DISCLAIMER

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