



Low Input Voltage Single Channel Full Bridge Driver

CJDR9111 Motor Driver

1 Introduction

CJDR9111 is a low-voltage 5V full-bridge motor drive integrated circuit, providing integrated motor driven solutions for camcorders, consumer products, toys and other low-voltage or battery-powered motion control applications. CJDR9111 can provide up to 1.1A continuous output current. It can operate at 2.0 ~ 6.0V power supply voltage. CJDR9111 has a PWM (IN / IN) input interface, is compatible with industry standard devices, and has over temperature protection.

2 Available Package

PART NUMBER	PACKAGE
CJDR9111	SOT-23-6L

Note: For more detailed packaging information, see the part *Pin Configuration and Function* and the part *Mechanical Information*.

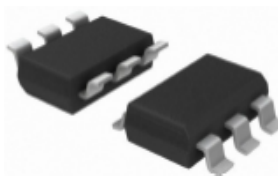


Figure 2-1. SOT-23-6L Package

3 Features

- H-Bridge Motor Driver
- Power Supply Voltage: 2.0 ~ 6.0V
- Low Conductivity Impedance: 480mΩ (HS + LS)
- Drives Output Current: 1.1A (Continuously)
- PWM (IN 1 / IN 2) Input Mode
- Built-in Over Temperature Protection
- Low Current Sleep Mode: (nA level, IN 1= IN 2 = 0)

4 Applications

- Digital Single Lens Reflex (DSLR) Lens
- Electric Toothbrush
- Medical Equipment
- Robotics
- Shared Bicycle Lock
- Toys
- Video Camera
- Water Gas Meter Switch

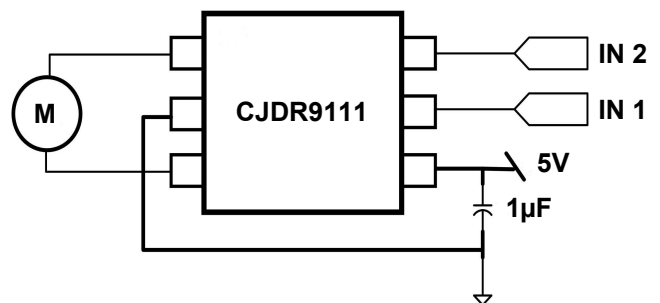


Figure 4-1. Typical Application Circuit

5 Pin Configuration and Function

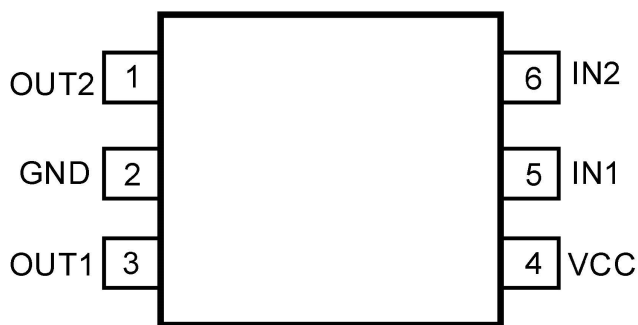


Figure 5-1. Package Top View

PIN NAME	CJDR9111	I / O	DESCRIPTION
	SOT-23-6L		
OUT 2	1	O	H-bridge output 2.
GND	2	-	Device ground. Connect to system ground.
OUT 1	3	O	H-bridge output 1.
VCC	4	-	Logic power supply.
IN 1	5	I	H-bridge control input 1.
IN 2	6	I	H-bridge control input 2.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

(over operating free-air temperature range, unless otherwise specified)

CHARACTERISTIC			SYMBOL	VALUE	UNIT
Power supply input voltage ⁽²⁾			V_{CC}	-0.3 ~ 7	V
Logic pin input voltage ⁽²⁾			V_{IN}	-0.5 ~ 7	
Maximum peak current			$I_{OUT\ MAX}$	2.2	A
Maximum power dissipation	CJDR9111	SOT-23-6L	$P_{D\ Max}$	Internally Limited ⁽³⁾	W
Maximum junction temperature			$T_{J\ Max}$	150	°C
Storage temperature			T_{stg}	-60 ~ 150	°C
Soldering temperature & time			T_{solder}	260°C, 10s	-

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) Refer to *Thermal Information* for details.

6.2 Recommended Operating Conditions⁽⁴⁾

PARAMETER	SYMBOL	MIN.	NOM.	MAX.	UNIT
Power supply input voltage	V_{CC}	2.0	-	6.0	V
Logic input voltage	V_{IN}	0	-	7.0	V
Continuous output current	I_{OUT}	0	-	1.1	A
PWM frequency	f_{PWM}	0	-	250	kHz
Operating junction temperature	T_J	-40	-	150	°C
Operating ambient temperature	T_A	-40 ⁽⁵⁾	-	100 ⁽⁵⁾	°C

(4) JSCJ recommends that users should not exceed the rated value in the *Recommended Operating Conditions* for the application conditions of the device, so as to ensure the stability of normal operation and the reliability of long-term operation. Operation beyond the recommended rated conditions does not mean that the device will fail. The consumers need to evaluate the risks that may be caused by the operation of the device beyond the recommended rated conditions.

(5) It is necessary to ensure that the operating junction temperature of the equipment does not exceed the rated value of the recommended operating conditions when using the device for design.

6 Specifications

6.3 ESD Ratings

ESD RATINGS		SYMBOL	VALUE	UNIT
Electrostatic discharge ⁽⁶⁾	Human body model	$V_{ESD-HBM}$	4000	V

(6) ESD testing is conducted in accordance with the relevant specifications formulated by the Joint Electronic Equipment Engineering Commission (JEDEC). The human body mode (HBM) electrostatic discharge test is based on the JESD22-114D test standard, using a 100pF capacitor and discharging to each pin of the device through a resistance of 1.5kΩ.

6.4 Thermal Information

THERMAL METRIC ⁽⁷⁾	SYMBOL	CJDR9111	UNIT
		SOT-23-6L	
Junction-to-ambient thermal resistance	$R_{\theta JA}$	238.1	°C/W
Maximum heat dissipation power for continuous operation	$P_{D Ref}$	0.42	W

(7) $T_A = 25^\circ\text{C}$, all numbers are typical, and apply for packages soldered directly onto a PCB board in still air.

6 Specifications

6.5 Electrical Characteristics

CJDR9111 ($V_{CC} = 5.0V$, $T_A = 25^\circ C$, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP. ⁽⁸⁾	MAX.	UNIT	
Power Supply							
Power supply voltage	V_{CC}	-	2.0	5.0	6.0	V	
Power supply current 1	I_{VCC}	$V_{CC} = 5V$, without PWM	-	200	550	μA	
Power supply current 2	I_{VCCQ}	$V_{CC} = 5V$, $IN\ 1 = IN\ 2 = 0V$, power saving mode	-	0.01	1.0	μA	
Output H-bridge Parameters							
High + Low bridge conduction resistance	$R_{DS\ ON}$	$V_{CC} = 5V$, $I_{OUT} = 500mA$	-	480	600	$m\Omega$	
Off leakage current	I_{OFF}	$V_{OUT} = 0V$	-200	-	200	nA	
Logic Input Pin (IN 1, IN 2)							
Input logic low voltage	V_{IL}	High level to low level	$V_{CC} = 3V$	0	-	0.75	V
			$V_{CC} = 5V$	0	-	1.0	
Input logic high voltage	V_{IH}	Low level to high level	$V_{CC} = 3V$	1.3	-	V_{CC}	V
			$V_{CC} = 5V$	2.1	-	V_{CC}	
Input logic hysteresis	V_{HY}	$V_{CC} = 3V$	-	0.4	-	V	
		$V_{CC} = 5V$	-	0.6	-		
Logic low input current	I_{IL}	$V_{IN\ x} = 0V$	-5	-	5	μA	
Logic high input current	I_{IH}	$V_{IN\ x} = 3.3V$	-	350	-	μA	
Pull down resistance	R_{PD}	-	-	100	-	$k\Omega$	
Thermal Shutdown Protection							
Thermal shutdown	T_{SD}	-	150	170	180	$^\circ C$	
Thermal shutdown hysteresis	ΔT_{SD}	-	-	30	-	$^\circ C$	
Undervoltage Locking							
Undervoltage locking voltage	V_{ULO}	Supply rising	-	2.0	-	V	
Undervoltage locking hysteresis	ΔV_{ULO}	Supply falling	-	200	-	mV	

Note:

(8) Typical numbers are at $25^\circ C$ and represent the most likely norm.

6 Specifications

6.6 Time Series Parameters

CJDR9111 ($V_{CC} = 5.0V$, $R_L = 20\Omega$, $T_A = 25^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP. ⁽⁸⁾	MAX.	UNIT
Start-up time	T1	-	-	600	-	ns
Shutdown time	T2	-	-	180	220	ns
Input high to output high delay	T3	-	-	160	200	ns
Input low to output low delay	T4	-	-	10	100	ns
Output rising edge time	T5	-	-	35	188	ns
Output drop edge time	T6	-	-	10	188	ns

Note:

(8) Typical numbers are at 25°C and represent the most likely norm.

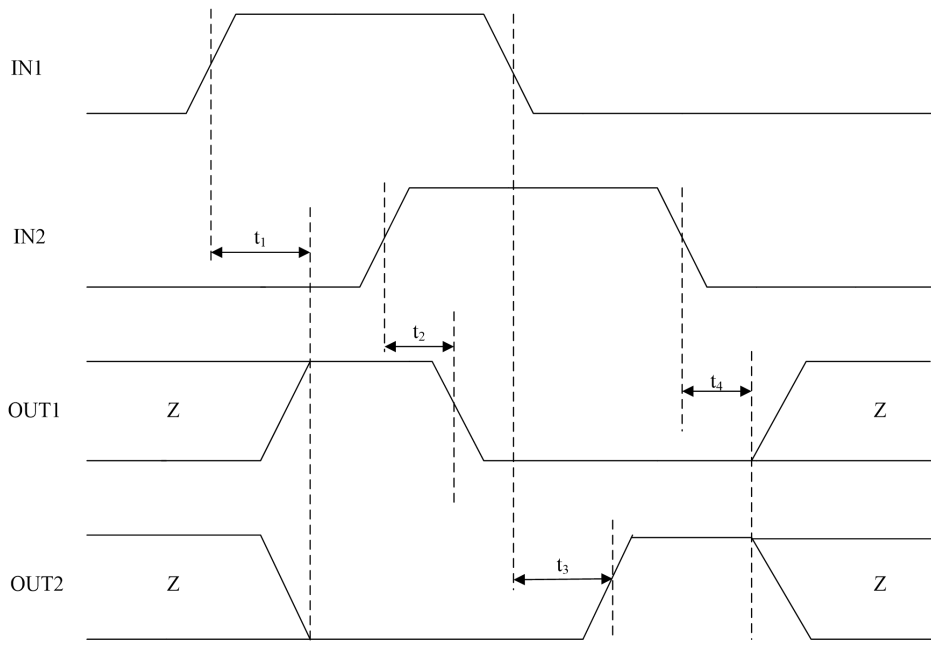


Figure 6-1. Input and Output Parameter Curve 1
(T1, T2, T3, T4)

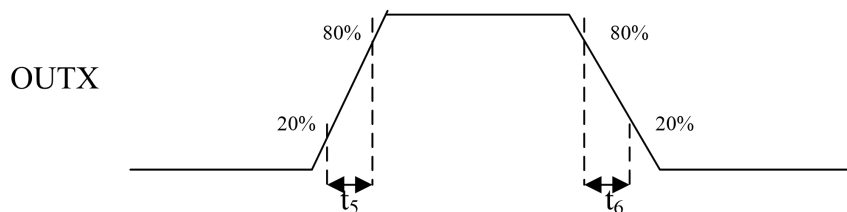


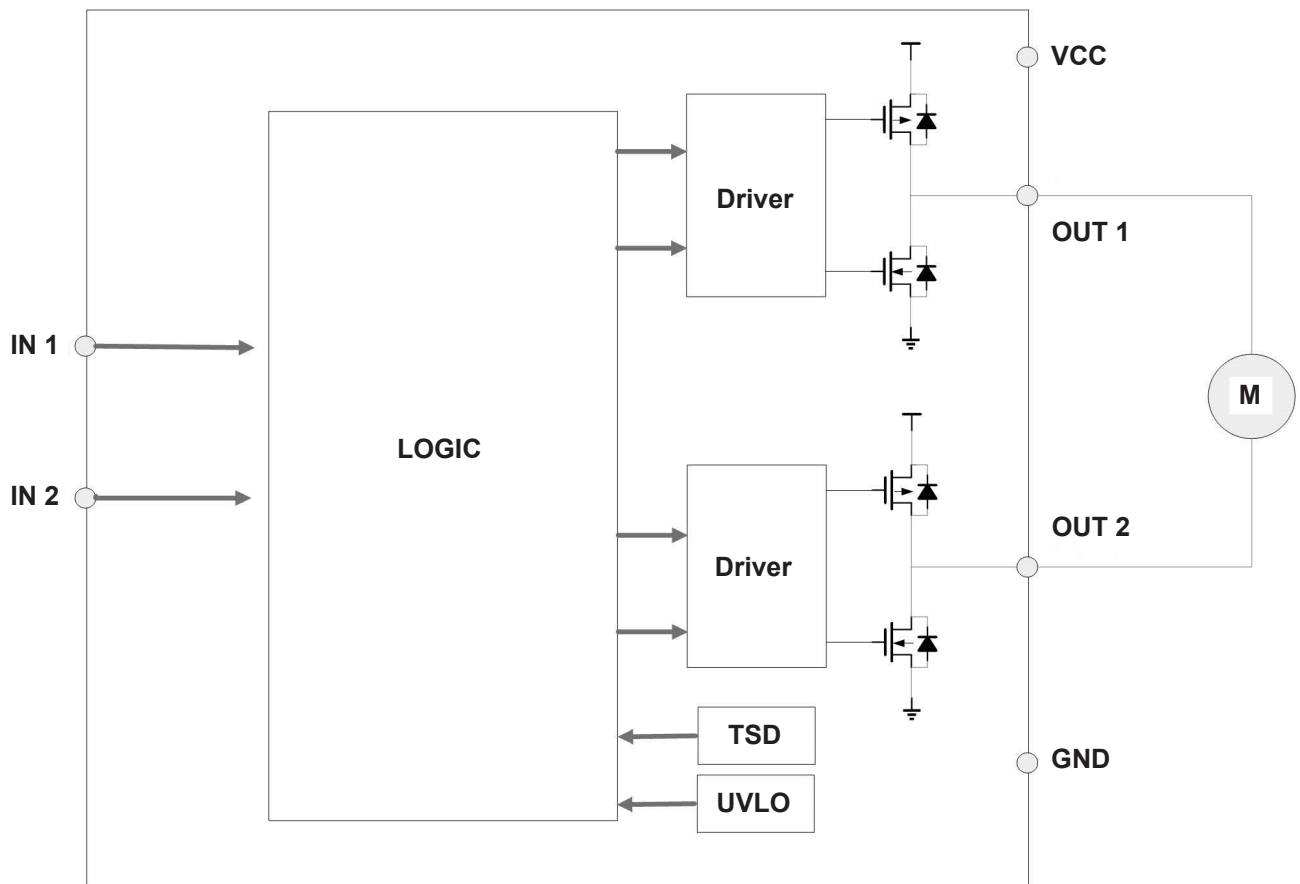
Figure 6-2. Input and Output Parameter Curve 2
(T5, T6)

7 Detailed Description

7.1 Description

CJDR9111 is a single-channel full-bridge driver that provides up to 1.1A continuous output current and can operate at 2.0 ~ 6.0V power supply voltage. CJDR9111 has industry standard compatible PWM (IN / IN) input interface, and has protection functions such as thermal shutdown and under-voltage locking.

7.2 Functional Block Diagram



7 Detailed Description

7.3 Feature Description

PWM Control Mode

CJDR9111 is controlled by PWM input interface, also known as IN / IN input mode, the PWM interface (IN 1 / IN 2) controls the OUT x pins according to the logic table in Table 7-1.

Table 7-1. PWM Control Mode with Automatic Sleep

IN 1	IN 2	OUT 1	OUT 2	DESCRIPTION
0	0	Hi-Z	Hi-Z	Coast (H-bridge Hi-Z) / low-power automatic sleep mode
0	1	L	H	Reverse (OUT 2 → OUT 1)
1	0	H	L	Forward (OUT 1 → OUT 2)
1	1	L	L	Brake (low-side slow decay)

Output Driver

Since the V_{GS} of the driving power supply of the output driver tube is related to the power supply, the H-bridge output conduction resistance of the CJDR9111 decreases with the increase of the voltage, so the current capacity of the chip decreases at low voltage.

Sleep Mode

When IN 1 and IN 2 are low at the same time, the chip works normal.

When IN 1 = IN 2 = 0, the chip enters a low-power sleep mode, the internal circuit stops working, and the total current is less than 1 μ A.

Input Pin

IN 1 and IN 2 input pins have 100k Ω resistance pull-down, and the default is low level.

Over Temperature Protection

When the chip junction temperature exceeds 170 $^{\circ}$ C, the over temperature protection circuit is activated and all output tubes are turned off. When the temperature decreases by a hysteresis temperature of 30 $^{\circ}$ C to 140 $^{\circ}$ C, the output tube returns to work. However, because the over temperature protection is activated only when the chip junction temperature exceeds the set value, it does not guarantee that the product will be protected from damage with this circuit.

Under-voltage Locking

When the chip power supply voltage is lower than 2.0V (Typ.), the internal detection circuit will turn off the H-bridge output. If the voltage recovers, the output turns on again when it rises to 2.2V (Typ.).

7 Detailed Description

7.3 Feature Description (continued)

Operation Mode

CJDR9111 enters the sleep mode when IN 1 = IN 2 is low. In the sleep mode, all h bridges are turned off and output high resistance state. Most circuits of chip circuits are turned off and enter the power saving mode. When IN 1 and IN 2 are not low at the same time, they will automatically resume normal operation.

When the over temperature protection detects failure, it will also close the H-bridge.

Table 7-2. Operation Mode

MODE	CONDITION	H-BRIDGE
Work	0 when IN 1 is different from IN 2	Normal Operation
Sleep mode	IN 1 = IN 2 = 0	Shutdown
Failure detection	IN x = X	Shutdown

8 Application and Implementation

8.1 Typical Application Circuit

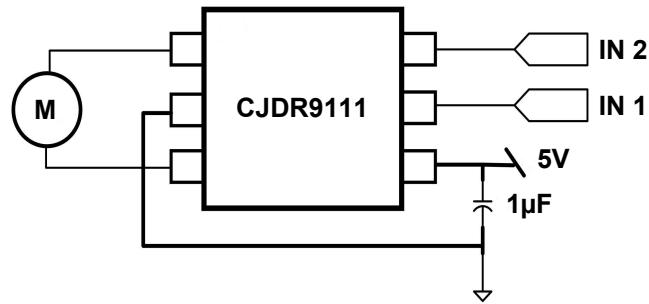


Figure 8-1. Typical Application Circuit

8.2 Application Information

The absolute parameters of the chip cannot be exceeded in any environment.

The bypass capacitor of V_{CC} , especially the connection of ceramic capacitor, should be as close to the V_{CC} pin of the chip as possible.

The ground wire connecting the motor needs to be isolated in layout design.

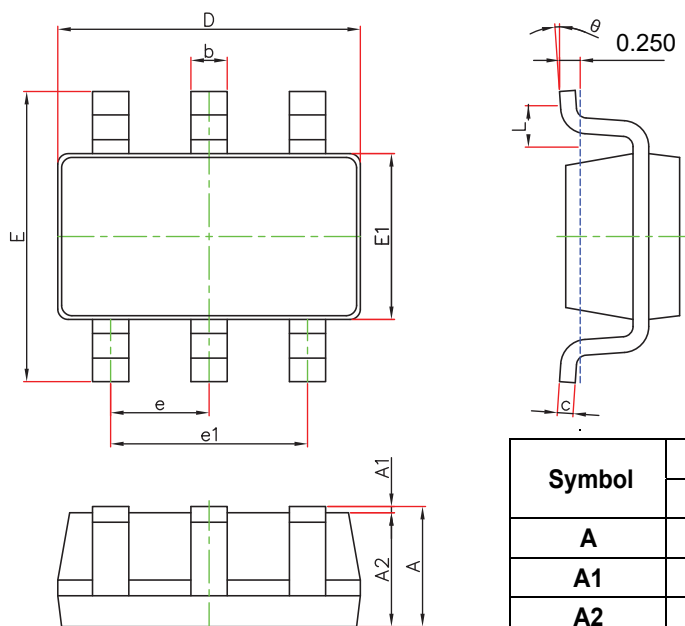
NOTE

The application information in this section is not part of the data sheet component specification, and JSCJ makes no commitment or statement to guarantee its accuracy or completeness. Customers are responsible for determining the rationality of corresponding components in their circuit design and making tests and verifications to ensure the normal realization of their circuit design.

9 Mechanical Information

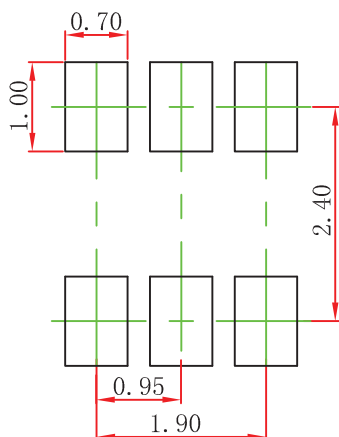
SOT-23-6L Mechanical Information

SOT-23-6L Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.250	-	0.049
A1	0.400	0.100	0.016	0.004
A2	1.000	1.200	0.039	0.047
b	0.330	0.410	0.013	0.016
c	0.150	0.190	0.006	0.007
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.900(BSC)		0.075(BSC)	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-6L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purpose only.

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

August 2022: released CJDR9111 rev - 1.0.

DISCLAIMER

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