2-Channel Auto-bidirectional Multi-voltage Level Translator

CJLSF0102 Logic

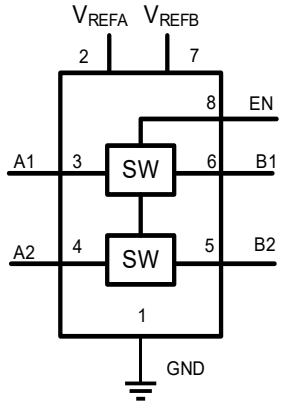
1 Introduction

CJLSF0102 is a voltage level translator. The circuit supports bidirectional multi-voltage level translation in the range of 0.8V to 5V without direction control.

2 Available Packages

PART NUMBER	PACKAGE
CJLSF0102	VSSOP8
	TSSOP8

Note: For all available packages, please refer to the part Orderable Information.



Functional block diagram

3 Features

- 2-channel bidirectional multi-voltage level translation
- Support bidirectional multi-voltage level translation in the range of 0.8V to 5V
  - 0.8V to 1.8/2.5/3.3/5V
  - 1.2V to 1.8/2.5/3.3/5V
  - 1.8V to 2.5/3.3/5V
  - 2.5V to 3.3/5V
  - 3.3V to 5V
- Transmission direction automatically adapted without direction control
- High-speed signal transmission
  - Support up to 100MHz translation at ≤30pF cap load
  - Support up to 40MHz translation at ≤50pF cap load
- Low ON-resistance when the translation channel is ON-state
- IO ports have high impedance characteristics when the translation channel is off (EN=GND)
- No power supply requirement, no latch-up risk
- Low power consumption

4 Applications

- GPIO、MDIO、PMBus、SMBus、SDIO、UART、I^2C and other interfaces in the telecommunications infrastructure
- Enterprise systems
- Communication equipment
- Personal electronics
- Industrial application

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJLSF0102VAN	VSSOP8	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active
CJLSF0102BAN	TSSOP8	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

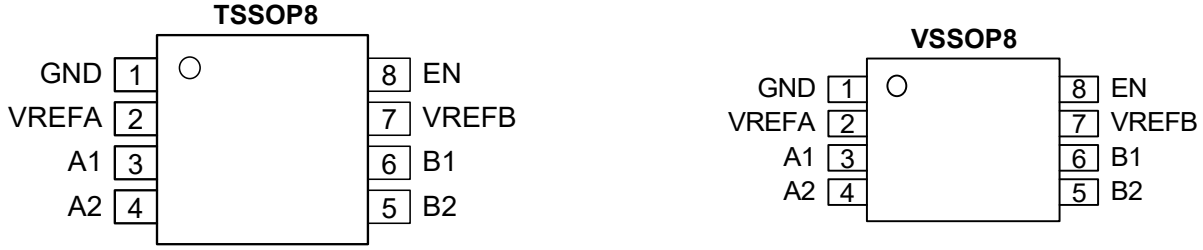


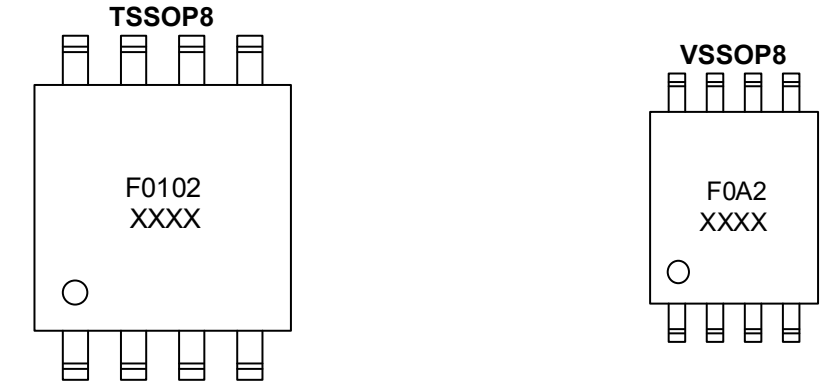
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	GND	G	Ground
2	VREFA	-	A port reference voltage, connected to A port signal power supply
3/4	A1,A2	I/O	Signal transmission port A
5/6	B2,B1	I/O	Signal transmission port B
7	VREFB	-	B port reference voltage, connected to B port signal power supply via 200K resistance
8	EN	I	Enable input, when connected to 0V, transmission channel is closed, and it is short circuited to VREFB and connected to the B port signal power supply through a 200K resistance to achieve automatic adaptation of signal transmission direction

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

T_{amb}=25°C, unless otherwise specified.

SYMBOL	PARAMETER	VALUE	UNIT
VREFA	Reference voltage 1	-0.3 to 7.0	V
VREFB	Reference voltage 2	-0.3 to 7.0	V
EN	Reference voltage 3	-0.3 to 7.0	V
V_{IN}	Input voltage	-0.3 to 7.0	V
T_{amb}	Operating temperature	-40 to 125	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Soldering temperature (10s)	260	°C

Note:

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. These are only partial specified values and do not support functional operations for conditions other than those specified.

(2) All voltage values are based on the ground port as the reference.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{VREFA}	VREFA voltage	0	-	5.5	V
V_{VREFB}	VREFB voltage	0	-	5.5	V
V_{EN}	EN voltage	0	-	5.5	V
V_{IN}	IO input voltage	0	-	5.5	V
I_{SW}	Transmission channel current	-	-	64	mA

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OL}	LOW-level output voltage	See Figure 7-1; VDD1=1.365V, VDD2=3V VBn=0.175V, VAn output or VAn=0.175V, VBn output Ipass=15.2mA	-	-	350	mV
Vclamp	Input clamp voltage	Ii=-18mA, V_{GREF}=0V	-	-	-1.2	V
I_{GREF}	EN input leakage current	V_{EN}=0V	-	-	5	uA
Ron	ON resistance	VREFA=3.3V, VREFB=EN=5V V_I=0V, I_O=64mA	-	8	-	Ω
		VREFA=1.8V, VREFB=EN=5V V_I=0V, I_O=64mA	-	9	-	Ω
		VREFA=1.0V, VREFB=EN=5V V_I=0V, I_O=64mA	-	10	-	Ω
		VREFA=1.8V, VREFB=EN=5V V_I=0V, I_O=32mA	-	10	-	Ω
		VREFA=2.5V, VREFB=EN=5V V_I=0V, I_O=32mA	-	15	-	Ω
		VREFA=3.3V, VREFB=EN=5V V_I=1.8V, I_O=15mA	-	9	-	Ω
		VREFA=1.8V, VREFB=EN=3.3V V_I=1.0V, I_O=10mA	-	18	-	Ω
		VREFA=1.0V, VREFB=EN=3.3V V_I=0V, I_O=10mA	-	20	-	Ω
		VREFA=1.0V, VREFB=EN=1.8V V_I=0V, I_O=10mA	-	30	-	Ω

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OL}	LOW-level output voltage	See Figure 7-1; VDD1=1.365V, VDD2=3V VBn=0.175V, VAn output or VAn=0.175V, VBn output Ipass=15.2mA	-	-	500	mV
Vclamp	Input clamp voltage	Ii=-18mA, V_{GREF}=0V	-	-	-1.2	V
I_{GREF}	EN input leakage current	V_{EN}=0V	-	-	15	uA
Ron	ON resistance	VREFA=3.3V, VREFB=EN=5V V_I=0V, I_O=64mA	-	12	-	Ω
		VREFA=1.8V, VREFB=EN=5V V_I=0V, I_O=64mA	-	14	-	Ω
		VREFA=1.0V, VREFB=EN=5V V_I=0V, I_O=64mA	-	15	-	Ω
		VREFA=1.8V, VREFB=EN=5V V_I=0V, I_O=32mA	-	15	-	Ω
		VREFA=2.5V, VREFB=EN=5V V_I=0V, I_O=32mA	-	23	-	Ω
		VREFA=3.3V, VREFB=EN=5V V_I=1.8V, I_O=15mA	-	14	-	Ω
		VREFA=1.8V, VREFB=EN=3.3V V_I=1.0V, I_O=10mA	-	27	-	Ω
		VREFA=1.0V, VREFB=EN=3.3V V_I=0V, I_O=10mA	-	30	-	Ω
		VREFA=1.0V, VREFB=EN=1.8V V_I=0V, I_O=10mA	-	45	-	Ω

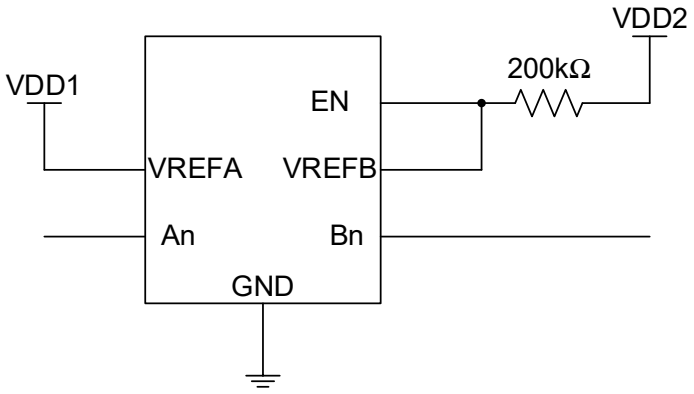


Figure 7-1

7.4.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay 1 (See Figure 7-3)	Test circuit see Figure 7-2 VDD1=1.365V to 1.635V VDD2=3V to 3.6V VDD3=2.36V to 2.63V t_r=t_f≤3ns An input, Bn output	0.5	1.5	5.5	ns

7.4.4 AC Characteristics 2

T_{amb}=-40°C to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay 1 (See Figure 7-3)	Test circuit see Figure 7-2 VDD1=1.365V to 1.635V VDD2=3V to 3.6V VDD3=2.36V to 2.63V t_r=t_f≤3ns An input, Bn output	0.5	3.0	10.0	ns

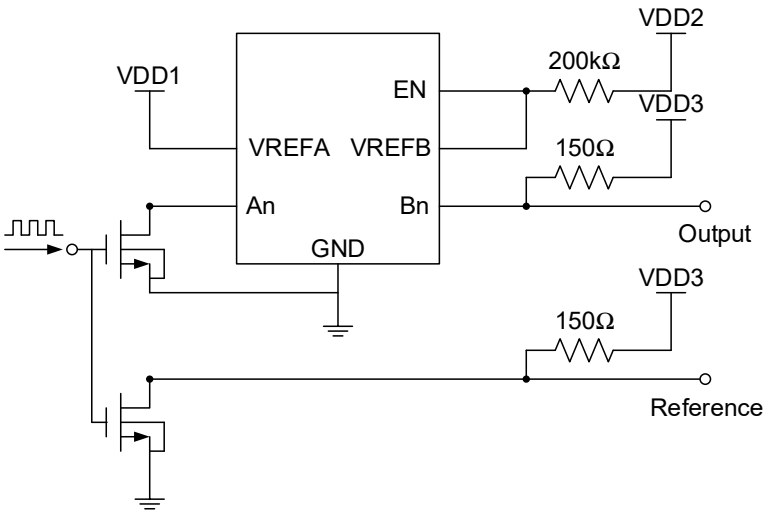


Figure 7-2

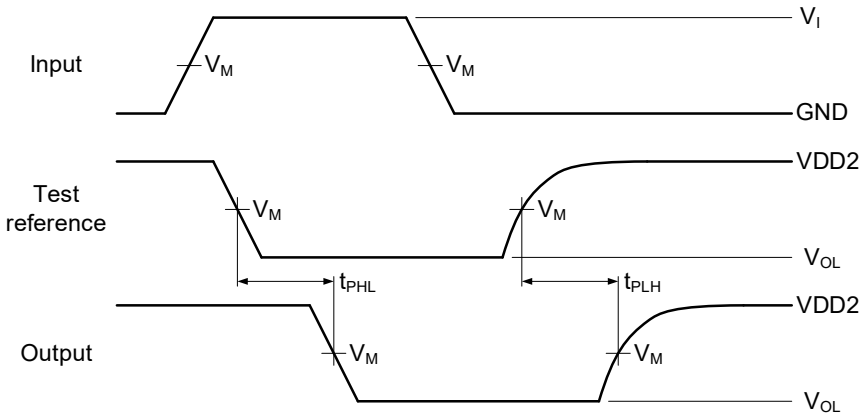


Figure 7-3

7.4.5 AC Characteristics 3

T_{amb}=-40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd}	Propagation delay 2 (See Figure 7-5)	Test circuit see Figure 7-4 V_{EN}=5V±0.5V VREFA, VREFB floating An input, Bn output or Bn input, An output	-	-	250	ps

7.4.6 AC Characteristics 4

T_{amb}=-40°C to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd}	Propagation delay 2 (See Figure 7-5)	Test circuit see Figure 7-4 V_{EN}=5V±0.5V VREFA, VREFB floating An input, Bn output or Bn input, An output	-	-	400	ps

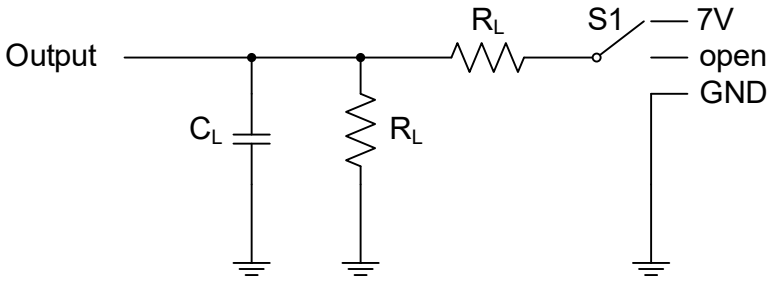


Figure 7-4

C_L=load capacitance including package, PCB and probe parasitic capacitance.

7.4.7 AC Characteristics 5

TEST	C_L	R_L	S1
t_{pd}	50pF	500Ω	Open

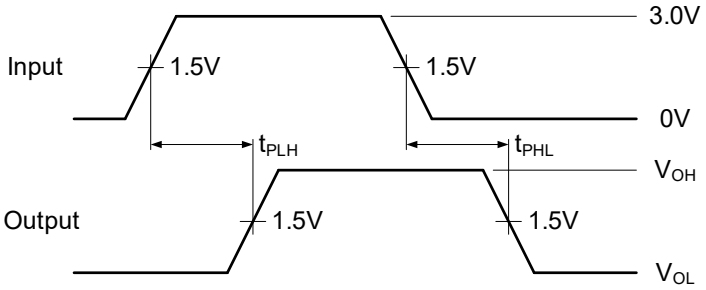


Figure 7-5

7.4.8 AC Characteristics 6

T_{amb}=-40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation delay 3 (See Figure 7-6/7-7)	S1 connected to open EN=3.3V, V_M=1.15V V_{IH}=3.3V, V_{IL}=0V R_L=300	C_L=50pF	-	1.1	-	ns
			C_L=30pF	-	0.7	-	ns
			C_L=15pF	-	0.3	-	ns
t_{PHL}			C_L=50pF	-	1.2	-	ns
			C_L=30pF	-	0.8	-	ns
			C_L=15pF	-	0.4	-	ns
t_{PLH}		S1 connected to open EN=2.5V, V_M=0.75V V_{IH}=2.5V, V_{IL}=0V R_L=300	C_L=50pF	-	1.2	-	ns
			C_L=30pF	-	0.8	-	ns
			C_L=15pF	-	0.35	-	ns
t_{PHL}			C_L=50pF	-	1.3	-	ns
			C_L=30pF	-	1.0	-	ns
			C_L=15pF	-	0.5	-	Ns
t_{PLH}		S1 connected to VH EN=3.3V, V_M=1.15V V_{IH}=2.3V, V_{IL}=0V VH=3.3V R_L=300	C_L=50pF	-	2.1	-	ns
			C_L=30pF	-	1.55	-	ns
			C_L=15pF	-	0.9	-	ns
t_{PHL}			C_L=50pF	-	2.2	-	ns
			C_L=30pF	-	1.65	-	ns
			C_L=15pF	-	1.0	-	ns
t_{PLH}		S1connected to VH EN=2.5V, V_M=0.75V V_{IH}=1.5V, V_{IL}=0V VH=2.5V R_L=300	C_L=50pF	-	1.1	-	ns
			C_L=30pF	-	0.9	-	ns
			C_L=15pF	-	0.45	-	ns
t_{PHL}			C_L=50pF	-	1.3	-	ns
			C_L=30pF	-	1.1	-	ns
			C_L=15pF	-	0.6	-	ns

7.4.9 AC Characteristics 7

T_{amb}=-40°C to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PLH}	Propagation delay 3 (See Figure 7-6/7-7)	S1 connected to open EN=3.3V, V_M=1.15V V_{IH}=3.3V, V_{IL}=0V R_L=300	C_L=50pF	-	1.7	-	ns
			C_L=30pF	-	1.0	-	ns
			C_L=15pF	-	0.5	-	ns
t_{PHL}			C_L=50pF	-	1.8	-	ns
			C_L=30pF	-	1.2	-	ns
			C_L=15pF	-	0.6	-	ns
t_{PLH}		S1 connected to open EN=2.5V, V_M=0.75V V_{IH}=2.5V, V_{IL}=0V R_L=300	C_L=50pF	-	1.8	-	ns
			C_L=30pF	-	1.2	-	ns
			C_L=15pF	-	0.5	-	ns
t_{PHL}			C_L=50pF	-	1.9	-	ns
			C_L=30pF	-	1.5	-	ns
			C_L=15pF	-	0.8	-	Ns
t_{PLH}		S1 connected to VH EN=3.3V, V_M=1.15V V_{IH}=2.3V, V_{IL}=0V VH=3.3V R_L=300	C_L=50pF	-	3.1	-	ns
			C_L=30pF	-	2.3	-	ns
			C_L=15pF	-	1.4	-	ns
t_{PHL}			C_L=50pF	-	3.3	-	ns
			C_L=30pF	-	2.5	-	ns
			C_L=15pF	-	1.5	-	ns
t_{PLH}		S1connected to VH EN=2.5V, V_M=0.75V V_{IH}=1.5V, V_{IL}=0V VH=2.5V R_L=300	C_L=50pF	-	1.7	-	ns
			C_L=30pF	-	1.4	-	ns
			C_L=15pF	-	0.7	-	ns
t_{PHL}			C_L=50pF	-	1.9	-	ns
			C_L=30pF	-	1.7	-	ns
			C_L=15pF	-	0.9	-	ns

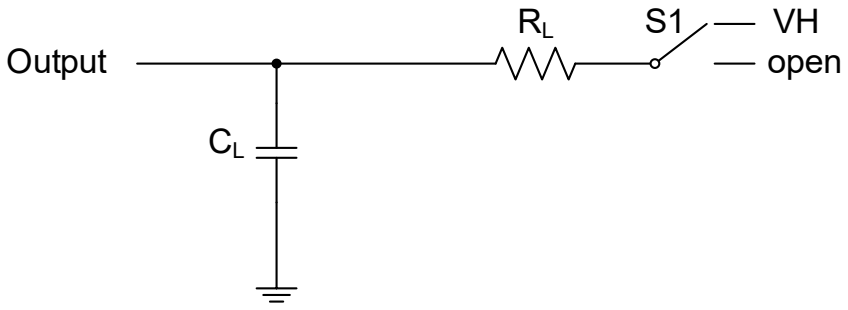


Figure 7-6

C_L=load capacitance including package, PCB and probe parasitic capacitance.

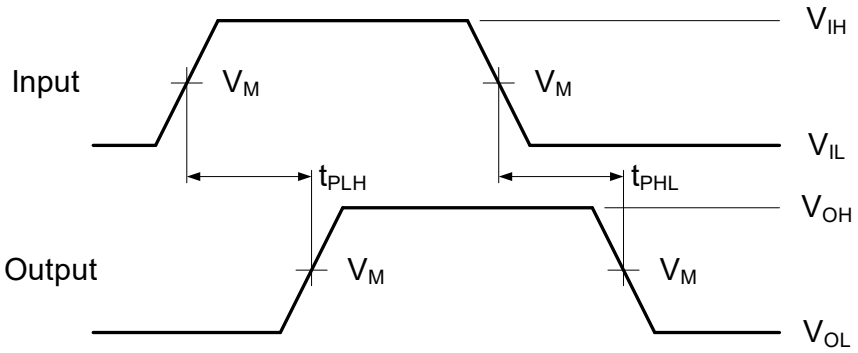


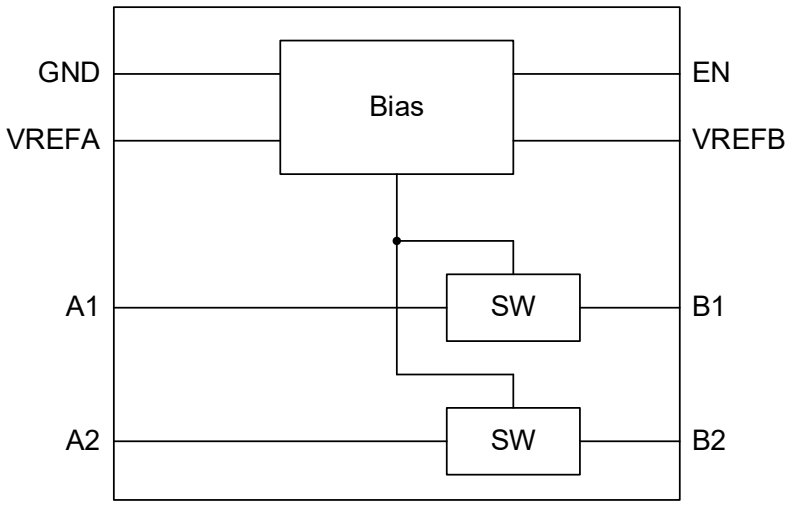
Figure 7-7

8 Detailed Description

8.1 Overview

CJLSF0102 is a voltage level translator. The circuit supports bidirectional multi-voltage level translation in the range of 0.8V to 5V without direction control.

8.2 Functional Block Diagram



8.3 Function Table

EN	VREFB	VREFA	Bn INPUT	An OUTPUT	TRANSMISSION CHANNEL
L	X	X	X	X	OFF
H (V_{EN})	H (V_{VREFB})	H (V_{VREFA})	V_{VREFB}	V_{VREFA}	ON
H (V_{EN})	H (V_{VREFB})	H (V_{VREFA})	L	L	ON

EN	VREFB	VREFA	An INPUT	Bn OUTPUT	TRANSMISSION CHANNEL
L	X	X	X	X	OFF
H (V_{EN})	H (V_{VREFB})	H (V_{VREFA})	V_{VREFA}	VH	ON
H (V_{EN})	H (V_{VREFB})	H (V_{VREFA})	L	L	ON

Note:

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care.

(2) $V_{EN}>V_{VREFA}$, $V_{VREFB}>V_{VREFA}$, $VH>V_{REFA}$ for normal operation

(3) When V_{EN} is 1.5V higher than V_{VREFA}, the circuit has the best signal transmission performance.

(4) When An is the output, An can be pulled up to V_{VREFA} by external resistance or without external pull-up resistance.

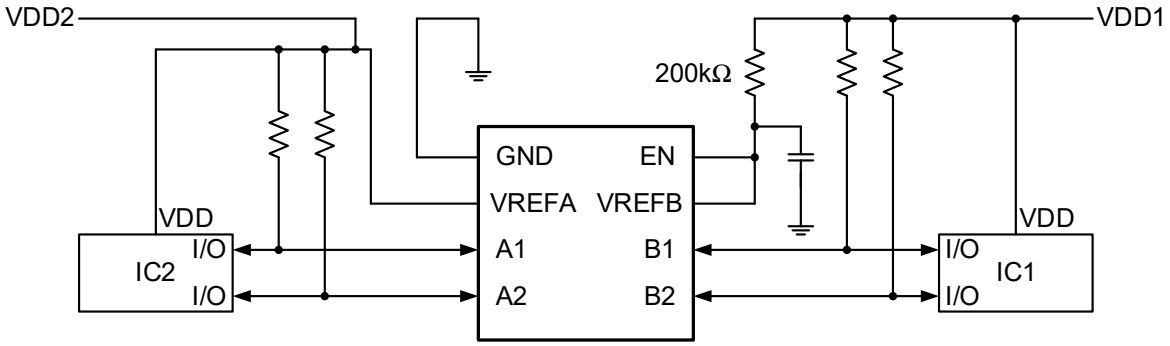
(5) When Bn is the output, Bn must be pulled up through the external resistance to a higher level than V_{VREFA}.

(6) When An/Bn outputs LOW, LOW-level output voltage value is determined by LOW-level input voltage value, not by GND.

8.4 Bidirectional Translation Without Direction Control

When applied to bidirectional signal transmission, and there is no control signal to indicate the direction of signal transmission, the VREFB must be connected to the EN and connected to the higher level by a 200kΩ resistance, and a filter capacitor near the EN port, while the SREF is connected to the lower level.

Both side signals can be push-pull or open-drain. But when signal is open-drain, an external pull-up resistance must be presented.

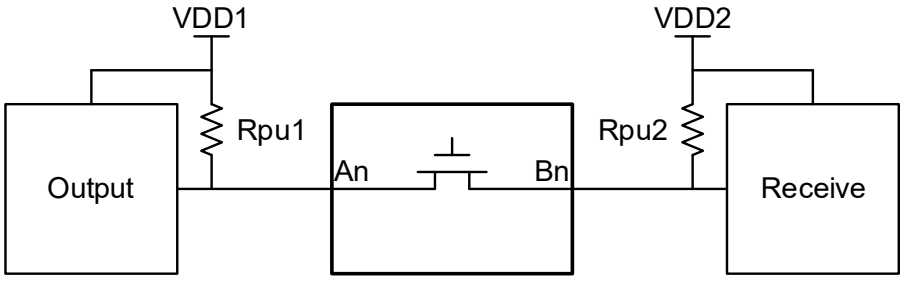


When VDD1≥VDD2+1.0V, the pull-up resistance of IO on the IC2 can be omitted.

8.5 Pull-up Resistor Sizing

Adding the pull-up resistance to IO can effectively improve the signal transmission efficiency and get a more complete waveform. Pull-up resistor value depends on several factors:

1. The low level driving ability of output device and the low level recognition ability of receive device
   When the output device outputs LOW-level, the current generated by the pull-up resistance of the An and Bn port will be absorbed by the low side drive of the output device, LOW-level of transmission will be pulled up. When the low level is pulled up beyond the low level recognition range of the receive device, the signal transmission will be abnormal. Therefore, the pull-up resistor should be selected according to the above factors, and the resistance value should not be set too small.
2. The rate of transmission signal
   When An is input, Bn is output, due to the requirement that VDD2 is higher than VDD1, this time due to the transmission principle of the circuit leads to the high level output of Bn port is to rely on Rpu2 pulled up, at this time the size of Rpu2 determines the rise rate of the signal of Bn, and further determines the highest frequency of the signal at Bn. Therefore, the resistance value cannot be set too large.



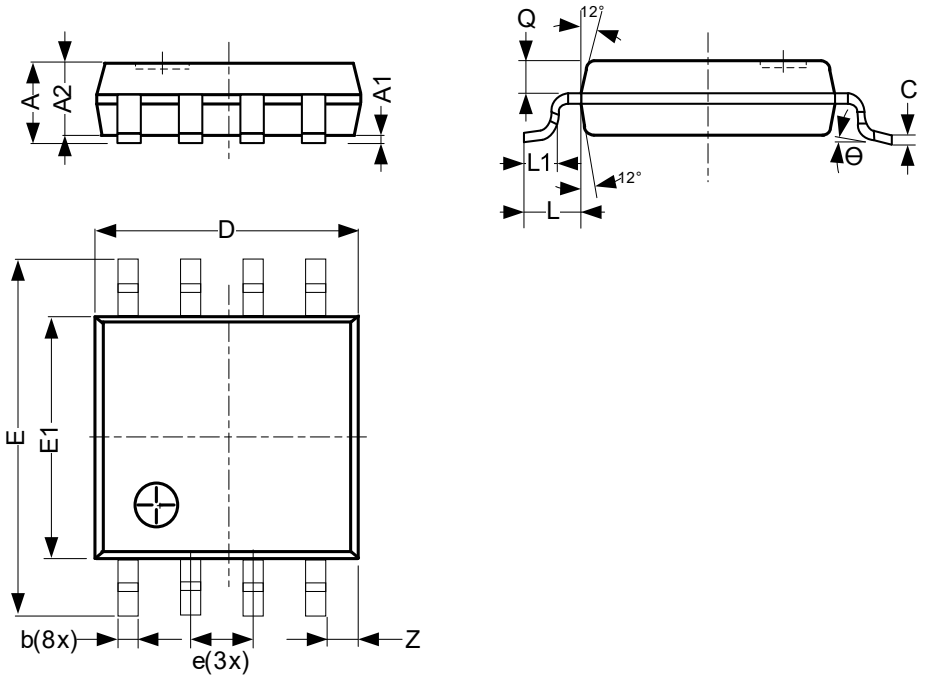
Pull-up resistor values:

LOW-LEVEL OUTPUT CURRENT OF OUTPUT DEVICE V_{OL}=0.2V		15mA		10mA		3mA	
VDD1	VDD2	Rpu1	Rpu2	Rpu1	Rpu2	Rpu1	Rpu2
0.8	1.8	147	147	220	220	733	733
0.8	2.5	193	193	290	290	967	967
0.8	3.3	247	247	370	370	1233	1233
0.8	5.0	360	360	540	540	1800	1800
1.2	1.8	173	173	260	260	867	867
1.2	2.5	220	220	330	330	1100	1100
1.2	3.3	273	273	410	410	1367	1367
1.2	5.0	387	387	580	580	1933	1933
1.5	1.8	193	193	290	290	967	967
1.5	2.5	240	240	360	360	1200	1200
1.5	3.3	293	293	440	440	1467	1467
1.5	5.0	407	407	610	610	2033	2033
1.8	2.5	260	260	390	390	1300	1300
1.8	3.3	313	313	470	470	1567	1567
1.8	5.0	427	427	640	640	2133	2133
2.5	3.3	360	360	540	540	1800	1800
2.5	5.0	473	473	710	710	2367	2367
3.3	5.0	527	527	790	790	2633	2633
<VDD2	1.0	-	53	-	80	-	267
<VDD2	1.2	-	67	-	100	-	333
<VDD2	1.5	-	87	-	130	-	433
<VDD2	1.8	-	107	-	160	-	533
<VDD2	2.5	-	153	-	230	-	767
<VDD2	3.3	-	207	-	310	-	1033
<VDD2	5.0	-	320	-	480	-	1600

9 Mechanical Information

9.1 VSSOP8 Mechanical Information

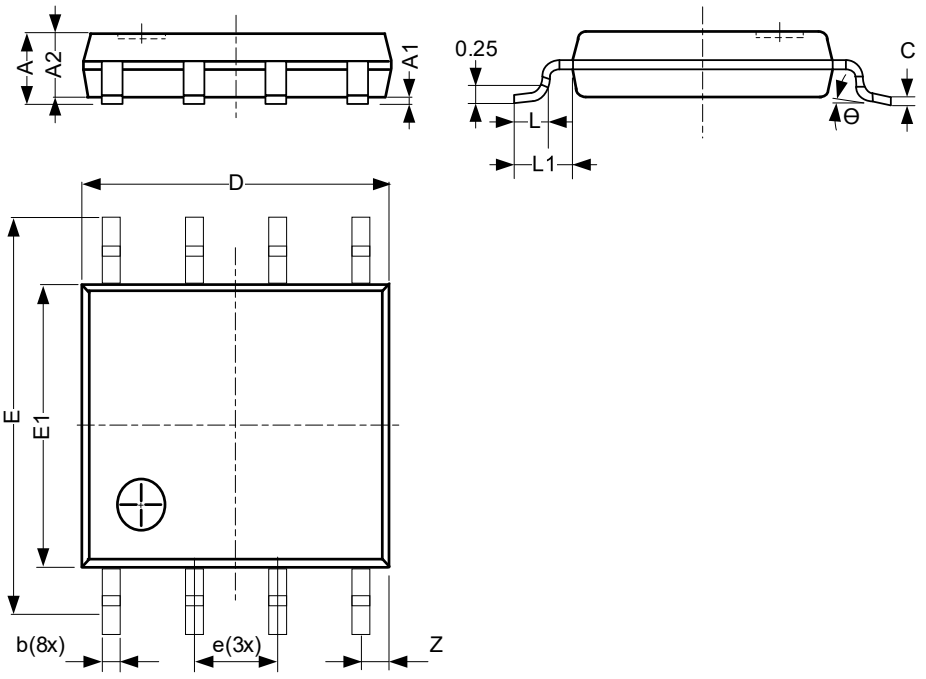
9.1.1 VSSOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.00
A1	0	-	0.15
A2	0.60	-	0.85
Q	0.19	-	0.21
b	0.17	-	0.27
c	0.08	-	0.23
D	1.90	-	2.10
E	3.00	-	3.20
E1	2.20	-	2.40
e	0.50 BSC		
L	-	0.40	-
L1	0.15	-	0.40
Z	0.10	-	0.40
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP8 Mechanical Information

9.2.1 TSSOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.10
A1	0	-	0.15
A2	0.75	-	0.95
b	0.22	-	0.38
c	0.08	-	0.18
D	2.90	-	3.10
E	3.90	-	4.10
E1	2.90	-	3.10
e	0.65 BSC		
L	0.33	-	0.47
L1	-	0.50	-
Z	0.35	-	0.70
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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