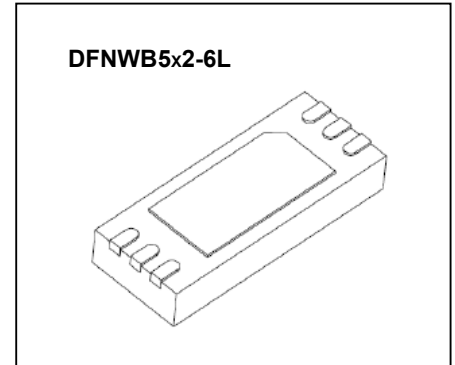




DFNWB5×2-6L Plastic-Encapsulate MOSFETS

CJND2004 Dual N-Channel MOSFET

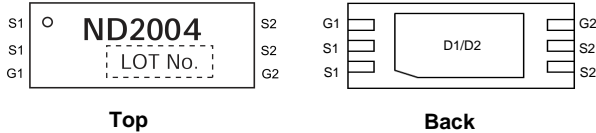
$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
20V	8.0 mΩ@4.5V	10A
	8.2 mΩ@4.0V	
	8.3 mΩ@3.8V	
	8.8 mΩ@3.1V	
	10 mΩ@2.5V	



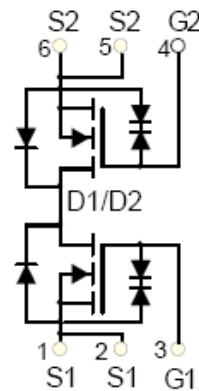
DESCRIPTION

The CJND2004 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.

MARKING:



Equivalent Circuit



MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	10	A
Pulsed Drain Current	I_{DM}^*	50	A
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	71.5	$^\circ\text{C/W}$
Junction Temperature and Storage Temperature Range	T_J, T_{stg}	-55~+150	$^\circ\text{C}$

MOSFET ELECTRICAL CHARACTERISTICS

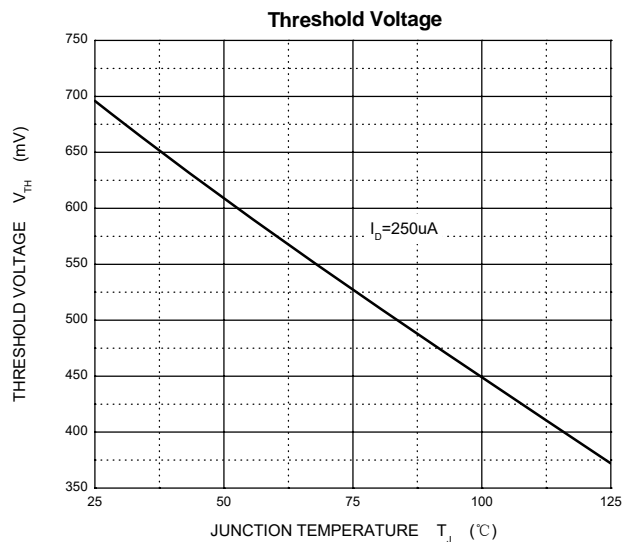
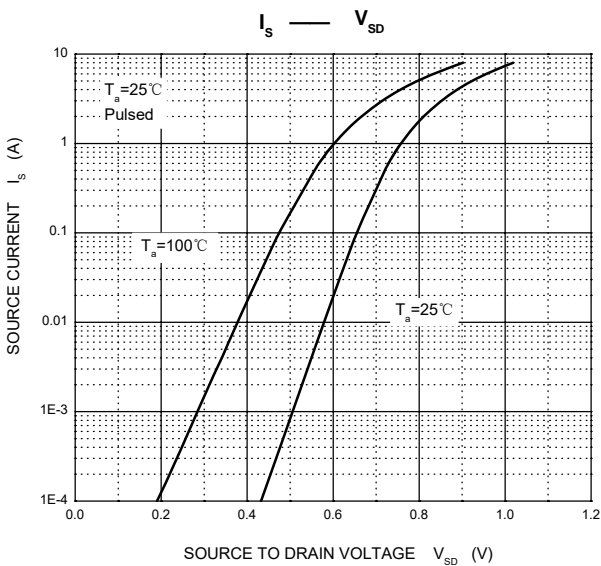
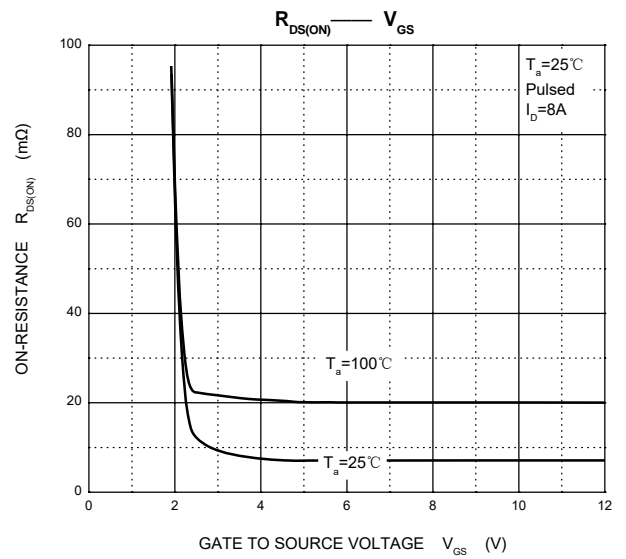
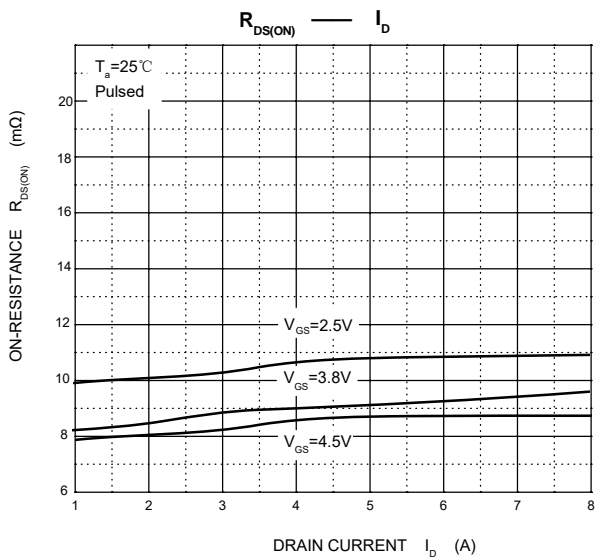
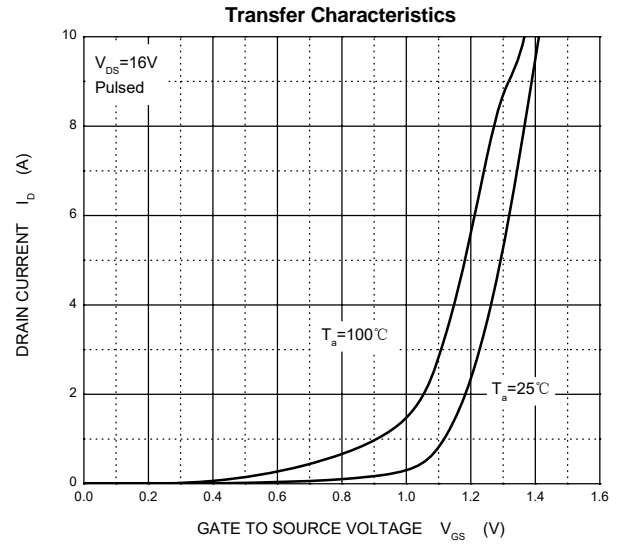
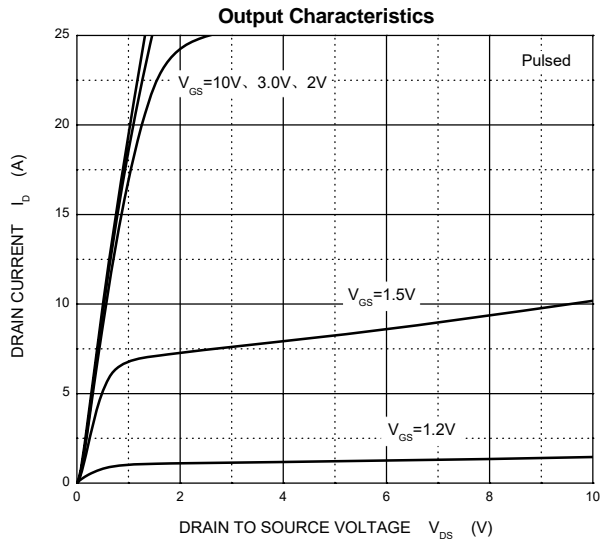
$T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 16V, V_{GS} = 0V$			1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 4.5V, V_{DS} = 0V$			± 1	μA
		$V_{GS} = \pm 8V, V_{DS} = 0V$			± 10	μA
Gate threshold voltage (note 1)	$V_{GS(th)}$	$V_{bs} = V_{GS}, I_D = 250\mu A$	0.4		1	V
Drain-source on-resistance (note 1)	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 3A$	5.6	8.0	10.5	m Ω
		$V_{GS} = 4.0V, I_D = 3A$	5.8	8.2	10.6	m Ω
		$V_{GS} = 3.8V, I_D = 3A$	6.0	8.3	10.7	m Ω
		$V_{GS} = 3.1V, I_D = 3A$	6.2	8.8	11.5	m Ω
		$V_{GS} = 2.5V, I_D = 3A$	7.0	10	13	m Ω
Forward transconductance (note 1)	g_{FS}	$V_{bs} = 5V, I_D = 7A$	9	36		S
Diode forward voltage (note 1)	V_{SD}	$I_S = 1A, V_{GS} = 0V$			1	V
DYNAMIC PARAMETERS (note 2)						
Input Capacitance	C_{iss}	$V_{DS} = 10V, V_{GS} = 0V, f = 1MHz$		1950		pF
Output Capacitance	C_{oss}			250		pF
Reverse Transfer Capacitance	C_{rss}			210		pF
Total gate charge	Q_g	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 7A$		17		nC
Gate-source charge	Q_{gs}			2.0		nC
Gate-drain charge	Q_{gd}			5.1		nC
SWITCHING PARAMETERS (note 2)						
Turn-on delay time	$t_{d(on)}$	$V_{GS} = 5V, V_{DD} = 10V,$ $R_L = 1.35\Omega, R_{GEN} = 3\Omega$		2.2		ns
Turn-on rise time	t_r			5.9		ns
Turn-off delay time	$t_{d(off)}$			40		ns
Turn-off fall time	t_f			90		ns
Drain-Source Diode Characteristics						
Diode Forward Current	I_S		-	-	6.0	A

Notes :

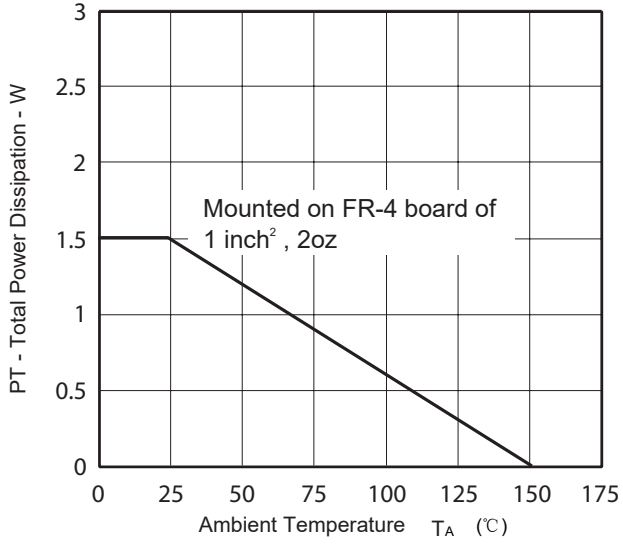
1. Pulse Test : Pulse width $\leq 300\mu s$, duty cycle $\leq 0.5\%$.
2. Guaranteed by design, not subject to production testing.

Typical Characteristics

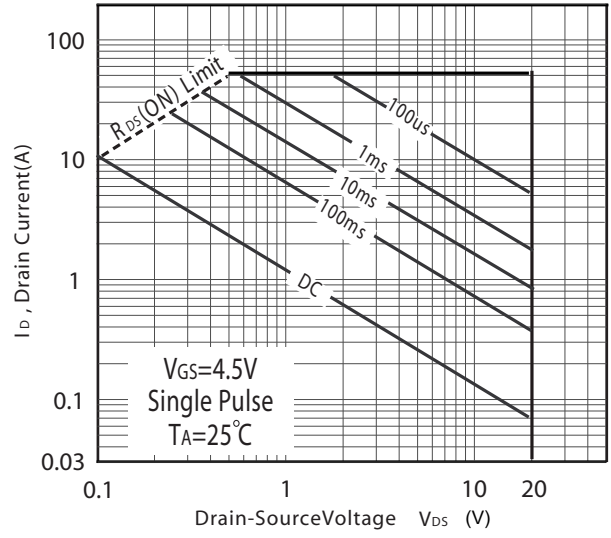


Typical Characteristics

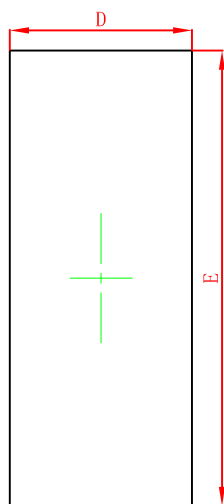
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



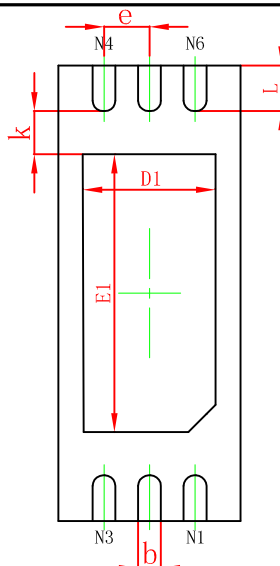
Maximum Safe Operating Area



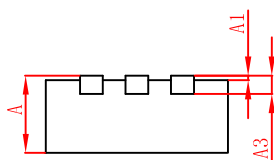
DFNWB5×2-6L-A Package Outline Dimensions(Unit:mm)



Top View



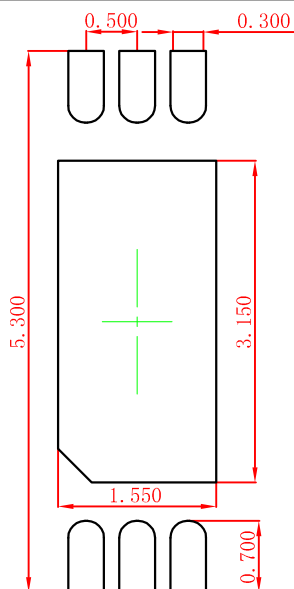
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	4.924	5.076	0.194	0.200
D1	1.350	1.550	0.053	0.061
E1	2.950	3.150	0.116	0.124
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.424	0.576	0.017	0.023

DFNWB5×2-6L-A Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.050 mm.
3. The pad layout is for reference purposes only.

NOTICE

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